

ACPL-M51L

1MBd Low Supply Voltage Digital Optocoupler



Data Sheet



Description

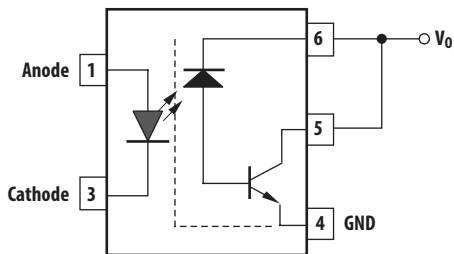
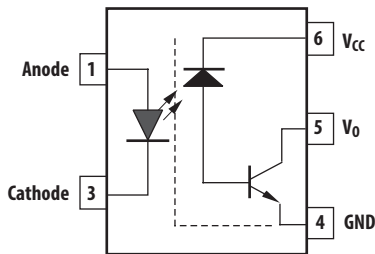
The ACPL-M51L (single-channel in SO-5 footprint), is low power, low supply voltage 1MBd digital optocoupler, configurable as a 4pin device.

This digital optocoupler use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output.

ACPL-M51L has an increased common mode transient immunity of 15kV/μs minimum at $V_{CM} = 1500V$.

The current transfer ratio (CTR) is 140% typical for ACPL-M51L at $I_F = 3.0mA$. This digital optocoupler can be use in any TTL/CMOS, TTL/LSTTL or analog applications.

Functional Diagram



Truth Table

LED	Vo
ON	LOW
OFF	HIGH

A 0.1μF bypass capacitor must be connected between pins V_{CC} and GND.
4-pin configuration : Pins 5 and 6 are externally shorted

Features

- Wide supply voltage V_{CC} : 2.25V to 24V
- Low Drive Current : 3.0mA
- Open-Collector Output
- TTL compatible (5-pin configuration)
- Compact SO-5 package
- 15 kV/μs High Common-Mode Rejection at $V_{CM} = 1500V$
- Guaranteed performance within temperature range: -40°C to +105°C
- Low Propagation Delay: 1μs max at 5V (5pin configuration)
- Worldwide Safety Approval:
 - UL1577 recognized, 3750Vrms/1min
 - CSA Approval
 - IEC/EN/DIN EN 60747-5-5 Approval for Reinforced Insulation

Applications

- Communications Interface
- Digital Signal Isolation
- MCU Interface
- Feedback Elements in Switching Power Supplies
- Digital isolation for A/D, D/A conversion Digital field

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.

Ordering Information

ACPL-M51L is UL Recognized with 3750 V_{rms} for 1 minute per UL1577.

Part Number	Options		Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Package				
ACPL-M51L	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

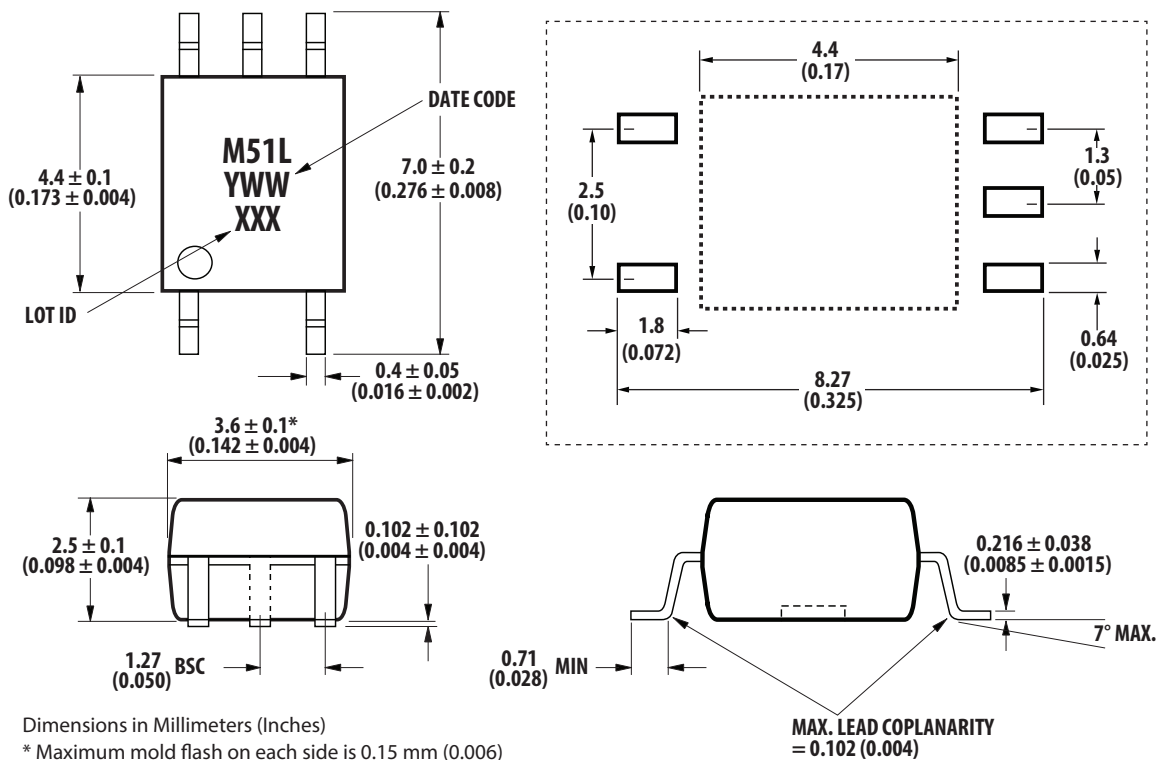
Example 1:

ACPL-M51L-560E to order product of Small Outline SO-5 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

ACPL-M51L Small Outline SO-5 Package (JEDEC MO-155)



Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-M51L is approved by the following organizations:

UL Approval under UL 1577, component recognition program up to $V_{ISO} = 3750 V_{RMS}$ File E55361.

CSA Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5 (Option 060E only)

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M51L	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060E)

Description	Symbol	Characteristic	Unit
	ACPL-M51L		
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 150 V_{RMS}$ for rated mains voltage $\leq 300 V_{RMS}$ for rated mains voltage $\leq 600 V_{RMS}$		I – IV I – III I – II	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V _{peak}
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial discharge < 5 pC	V_{PR}	1050	V _{peak}
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10$ sec, Partial discharge < 5 pC	V_{PR}	896	V _{peak}
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60$ sec)	V_{IOTM}	6000	V _{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	150	°C
Input Current**	$I_{S, INPUT}$	150	mA
Output Power**	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S , $V_{IO} = 500$ V	R_S	$> 10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	105	°C
Lead Soldering Cycle	Temperature		260	°C
	Time		10	s
Average Forward Input Current ^[1]	$I_{F(avg)}$		20	mA
Peak Forward Input Current ^[2] (50% duty cycle, 1ms pulse width)	$I_{F(peak)}$		40	mA
Peak Transient Input Current ($\leq 1\mu s$ pulse width, 300ps)	$I_{F(trans)}$		1	A
Reversed Input Voltage	V_R		5	V
Input Power Dissipation ^[3]	P_{IN}		36	mW
Output Power Dissipation ^[4]	P_O		45	mW
Average Output Current	$I_{O(AVG)}$		8	mA
Peak Output Current	$I_{O(PEAK)}$		16	mA
Supply Voltage	V_{CC}	-0.5	30	V
Output Voltage	V_O	-0.5	24	V
Solder Reflow Temperature Profile	See Package Outline Drawings section			

Notes:

1. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.
2. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.
3. Derate linearly above 85°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 1.2 mW/°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	2.25 ^[1]	24	V
Input Current, High Level ^[1]	I_{FH}	3.0	10	mA
Operating Temperature	T_A	-40	105	°C
Forward Input Voltage (OFF)	$V_{F(OFF)}$		0.8	V

Notes:

1. 5-pin configuration

Electrical Specifications (DC)

Over recommended operating $T_A = -40^\circ\text{C}$ to 105°C , supply voltage ($2.25\text{V} \leq V_{CC} \leq 24\text{V}$) and unless otherwise specified. All typicals are at $T_A = 25^\circ\text{C}$

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions	Fig.
Current Transfer Ratio	CTR ^[1]	80	140	200	%	$T_A = 25^\circ\text{C}$ $V_O = 0.4\text{V}$ $V_{CC} = 2.5\text{V}$ or 3.3V or 5V , $I_F = 3\text{mA}$	2a, 2b, 3
		60			%	$V_O = 0.5\text{V}$	
Logic Low Output Voltage	V_{OL}		0.2	0.4	V	$T_A = 25^\circ\text{C}$ $I_O = 3\text{mA}$ $V_{CC} = 2.5\text{V}$ or 3.3V or 5V , $I_F = 3\text{mA}$	
			0.2	0.5	V	$I_O = 1.6\text{mA}$	
Logic High Output Current	I_{OH}		0.003	0.5	μA	$T_A = 25^\circ\text{C}$ $V_O = V_{CC} = 5.5\text{V}$ $I_F = 0\text{mA}$	4, 5
			0.01	1		$V_O = V_{CC} = 24\text{V}$	
				80		$V_O = V_{CC} = 24\text{V}$	
Logic Low Supply Current per Channel	I_{CCL}		36	100	μA	$I_F = 3\text{mA}$, $V_O = \text{open}$, $V_{CC} = 24\text{V}$	
Logic High Supply Current per Channel	I_{CCH}		0.02	2	μA	$I_F = 0\text{mA}$, $V_O = \text{open}$, $V_{CC} = 24\text{V}$	
Input Forward Voltage	V_F		1.5	1.8	V	$T_A = 25^\circ\text{C}$ $I_F = 3\text{mA}$	1
			1.5	1.95	V	$I_F = 3\text{mA}$	
Input Reversed Breakdown Voltage	BV_R	5			V	$I_R = 10\mu\text{A}$	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		-1.6		$\text{mV}/^\circ\text{C}$	$I_F = 3\text{mA}$	
Input Capacitance	C_{IN}		77		pF	$F = 1\text{MHz}$, $V_F = 0$	

Switching Specifications

Over recommended operating ($T_A = -40^{\circ}\text{C}$ to 105°C), $I_F = 3\text{mA}$, ($2.25\text{V} \leq V_{CC} \leq 24\text{V}$), unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig.
Propagation Delay Time to Logic Low at Output	t_{PHL}	0.2	0.5	0.5	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 2.5\text{V}$, $R_L = 560\Omega$, $V_{\text{THHL}} = 1.5\text{V}$	14
		0.2	1	1	μs		6a, 14
		0.2	0.5	0.5	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 3.3\text{V}$, $R_L = 1.2\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$	14
		0.2	1	1	μs		6b, 14
		0.22	0.5	0.5	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$	14
		0.22	1	1	μs		7, 14
		0.33	0.7	0.7	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 24\text{V}$, $R_L = 10\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$	14
		0.33	1.3	1.3	μs		8, 14
Propagation Delay Time to Logic High at Output	t_{PLH}	0.38	0.8	0.8	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 2.5\text{V}$, $R_L = 560\Omega$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.38	1.2	1.2	μs		6a, 14
		0.38	0.8	0.8	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 3.3\text{V}$, $R_L = 1.2\text{k}\Omega$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.38	1.2	1.2	μs		6b, 14
		0.31	0.7	0.7	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.31	1	1	μs		7, 14
		0.3	0.7	0.7	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 24\text{V}$, $R_L = 10\text{k}\Omega$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.3	1	1	μs		8, 14
Pulse Width Distortion ^[2]	PWD	0.18	0.8	0.8	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 2.5\text{V}$, $R_L = 560\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.18	1.2	1.2	μs		14
		0.18	0.8	0.8	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 3.3\text{V}$, $R_L = 1.2\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.18	1.2	1.2	μs		14
		0.1	0.7	0.7	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.1	1	1	μs		14
		0.1	0.7	0.7	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 24\text{V}$, $R_L = 10\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.1	1	1	μs		14
Propagation Delay Difference Between Any two Parts ^[3]	t_{psk}	0.18	0.7	0.7	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 2.5\text{V}$, $R_L = 560\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.18	0.7	0.7	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 3.3\text{V}$, $R_L = 1.2\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.1	0.6	0.6	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
		0.1	0.6	0.6	μs	$T_A=25^{\circ}\text{C}$ $V_{CC} = 24\text{V}$, $R_L = 10\text{k}\Omega$, $V_{\text{THHL}} = 1.5\text{V}$, $V_{\text{THLH}} = 1.5\text{V}$	14
Common Mode Transient Immunity at Logic High Output ^[4]	$ C_{\text{MH}} $	15	25		$\text{kV}/\mu\text{s}$	$T_A=25^{\circ}\text{C}$ $V_{\text{CM}} = 1500\text{V}$, $I_F = 0\text{mA}$, $R_L = 560\Omega$, $1.2\text{k}\Omega$ or $1.9\text{k}\Omega$, $V_{CC} = 2.5\text{V}$ or 3.3V or 5V	15
Common Mode Transient Immunity at Logic Low Output ^[5]	$ C_{\text{ML}} $	15	20		$\text{kV}/\mu\text{s}$	$T_A=25^{\circ}\text{C}$ $V_{\text{CM}} = 1500\text{V}$, $I_F = 3\text{mA}$, $R_L = 1.2\text{k}\Omega$, $V_{CC} = 5\text{V}$	15
		10	15		$\text{kV}/\mu\text{s}$	$T_A=25^{\circ}\text{C}$ $V_{\text{CM}} = 1500\text{V}$, $I_F = 3\text{mA}$, $R_L = 560\Omega$ or $1.2\text{k}\Omega$, $V_{CC} = 2.5\text{V}$ or 3.3V	15

Notes:

- CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
- Pulse Width Distortion (PWD) is defined as $|t_{\text{PHL}} - t_{\text{PLH}}|$ for any given device.
- The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
- Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0\text{V}$).
- Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{V}$).

Electrical Specifications (DC) for 4-Pin Configuration

Applicable for $V_{CC} = V_O$. Over recommended operating $T_A = -40^{\circ}\text{C}$ to 105°C and unless otherwise specified. All typicals are at $T_A = 25^{\circ}\text{C}$

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions	Fig.
Current Transfer Ratio	CTR ^[1]		140		%	$T_A = 25^{\circ}\text{C}$ $I_F = 3\text{mA}$, $V_O = V_{CC} = 5\text{V}$	20
Current Transfer Ratio	CTR ^[1] (Sat)	20	70		%	$I_F = 10\text{mA}$ $V_O = V_{CC} = 0.5\text{V}$ $I_F = 3\text{mA}$	21
Logic Low Output Voltage	V_{OL}		0.1	0.2	V	$T_A = 25^{\circ}\text{C}$ $I_O = 0.6\text{mA}$ $I_F = 10\text{mA}$	
			0.1	0.2	V		
				0.5	V	$I_O = 2.4\text{mA}$ $I_F = 3\text{mA}$	
Off-State Current	$I_{(CEO)}$		0.0001	5	μA	$I_F = 0\text{mA}$, $V_O = V_{CC} = 15\text{V}$	

Switching Specifications for 4-Pin Configuration

Over recommended operating ($T_A = -40^{\circ}\text{C}$ to 105°C), $I_F = 3\text{mA}$, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig.	
Propagation Delay Time to Logic Low at Output	t_{PHL}		8	50	μs	Pulse: $f = 1\text{kHz}$, $V_{CC} = 5.0\text{V}$, $R_L = 8.2\text{k}\Omega$, $V_{THHL} = 1.5\text{V}$	18	
				5	50	μs		Pulse: $f = 1\text{kHz}$, $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $V_{THHL} = 1.5\text{V}$
				8	50	μs		Pulse: $f = 500\text{Hz}$, $V_{CC} = 24.0\text{V}$, $R_L = 39\text{k}\Omega$, $V_{THHL} = 1.5\text{V}$
Propagation Delay Time to Logic High at Output	t_{PLH}		35	100	μs	Pulse: $f = 1\text{kHz}$, $V_{CC} = 5.0\text{V}$, $R_L = 8.2\text{k}\Omega$, $V_{THLH} = 1.5\text{V}$	18	
				10	50	μs		Pulse: $f = 1\text{kHz}$, $V_{CC} = 5.0\text{V}$, $R_L = 1.9\text{k}\Omega$, $V_{THLH} = 1.5\text{V}$
				35	100	μs		Pulse: $f = 500\text{Hz}$, $V_{CC} = 24.0\text{V}$, $R_L = 39\text{k}\Omega$, $V_{THLH} = 1.5\text{V}$
Common Mode Transient Immunity at Logic High Output ^[2]	$ CM_H $	15	25		$\text{kV}/\mu\text{s}$	$T_A = 25^{\circ}\text{C}$ $V_{CM} = 1500\text{V}$, $I_F = 0\text{mA}$, $R_L = 8.2\text{k}\Omega$, $V_{CC} = 5\text{V}$	19	
Common Mode Transient Immunity at Logic Low Output ^[3]	$ CM_L $	10	15		$\text{kV}/\mu\text{s}$	$T_A = 25^{\circ}\text{C}$ $V_{CM} = 1500\text{V}$, $I_F = 3\text{mA}$, $R_L = 8.2\text{k}\Omega$, $V_{CC} = 5\text{V}$	19	

Notes:

- CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
- Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0\text{V}$).
- Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{V}$).

Package Characteristics

All Typical at $T_A = 25^{\circ}\text{C}$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage ^[1,2]	V_{ISO}	3750			Vrms	$RH \leq 50\%$, $t = 1\text{min.}$, $T_A = 25^{\circ}\text{C}$
Input-Output Resistance ^[1]	R_{I-O}		10^{14}		Ω	$V_{I-O} = 500\text{Vdc}$
Input-Output Capacitance ^[1]	C_{I-O}		0.6		pF	$f = 1\text{MHz}$, $T_A = 25^{\circ}\text{C}$

Notes:

- Device considered a two terminal device: pins 1 and 3 shorted together and pins 4, 5 and 6 shorted together
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 4500 V_{RMS}$ for 1 second. (leakage detection current limit, $I_{I-O} \leq 5\ \mu\text{A}$).

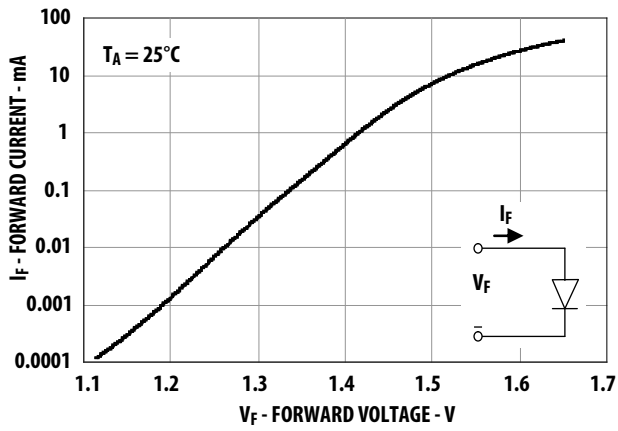


Figure 1. Input Current vs. Forward Voltage

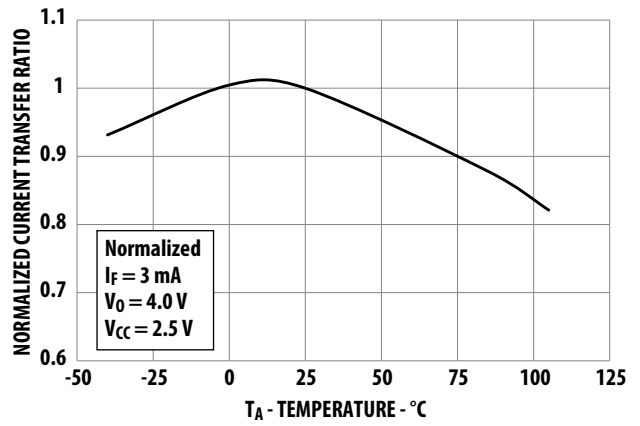


Figure 2a. Typical Current Transfer Ratio vs. Temperature ($V_{CC} = 2.5\text{ V}$)

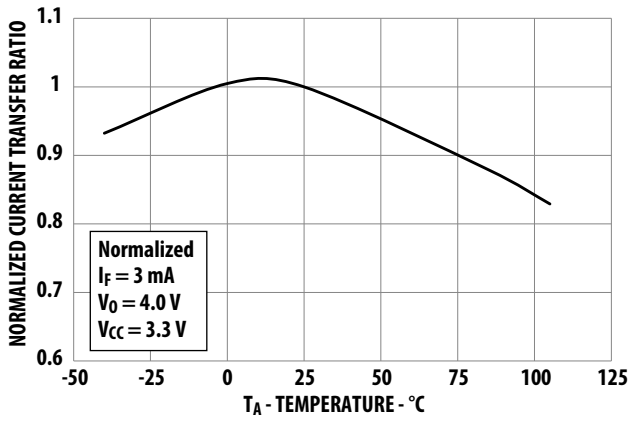


Figure 2b. Typical Current Transfer Ratio vs. Temperature ($V_{CC} = 3.3\text{ V}$)

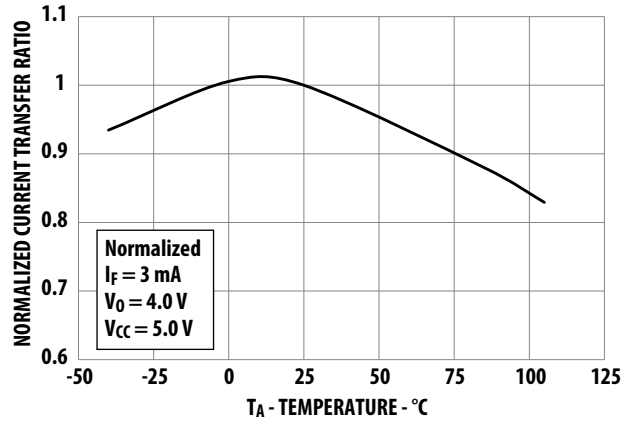


Figure 3. Typical Current Transfer Ratio vs. Temperature ($V_{CC} = 5.0\text{ V}$)

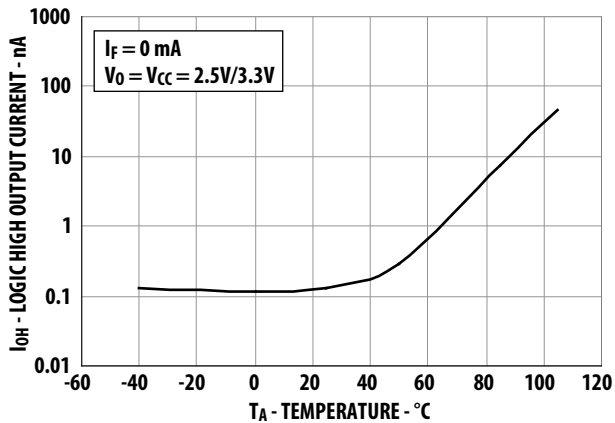


Figure 4 Typical Logic High Output Current vs. Temperature

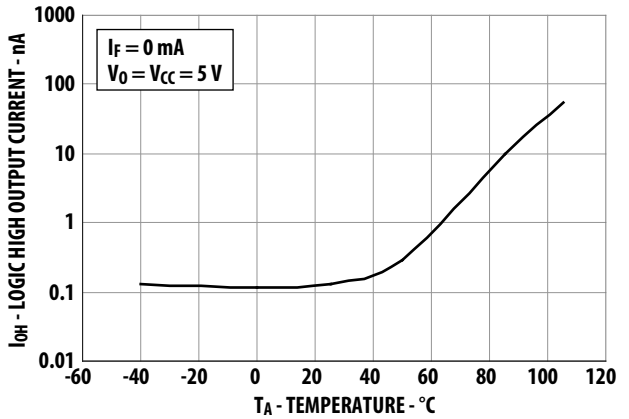


Figure 5. Typical Logic High Output Current vs. Temperature

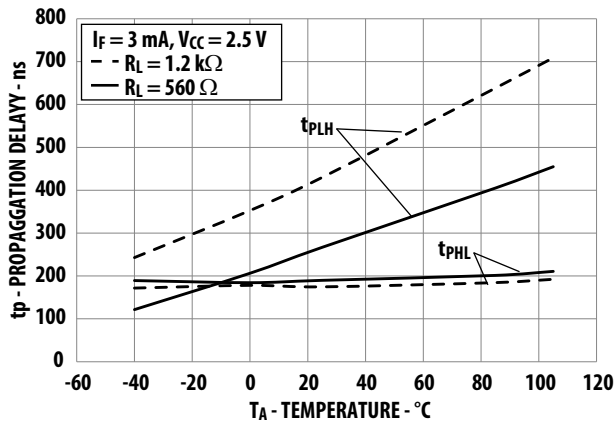


Figure 6a. Typical Propagation Delay vs. Temperature ($V_{CC} = 2.5\text{ V}$)

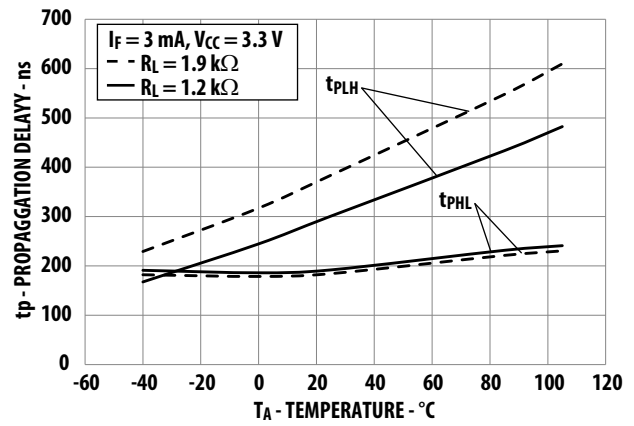


Figure 6b. Typical Propagation Delay vs. Temperature ($V_{CC} = 3.3\text{ V}$)

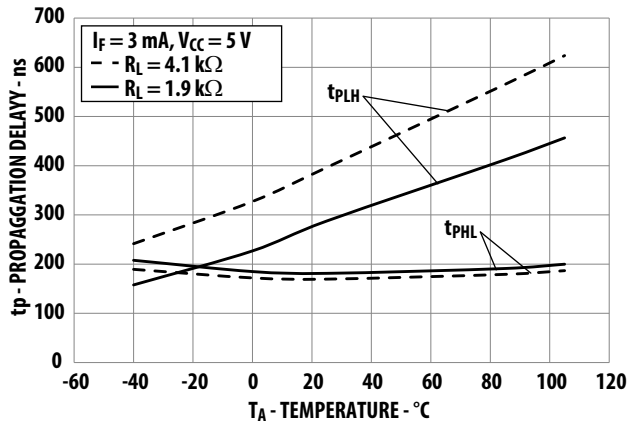


Figure 7. Typical Propagation Delay vs. Temperature ($V_{CC} = 5.0\text{ V}$)

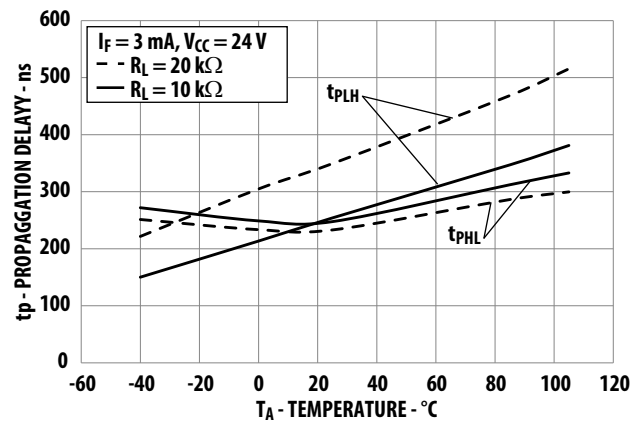


Figure 8. Typical Propagation Delay vs. Temperature ($V_{CC} = 24\text{ V}$)

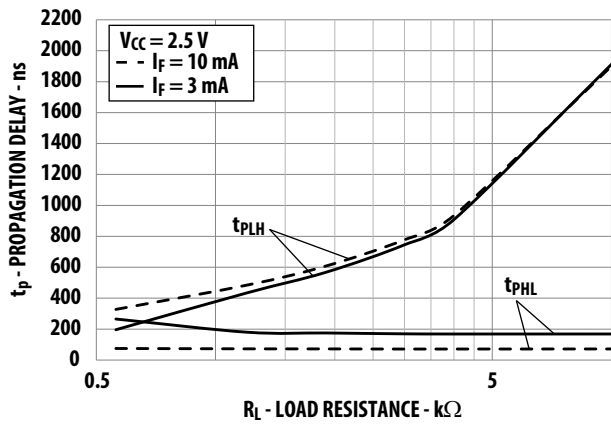


Figure 9a. Typical Propagation Delay vs. Load Resistance ($V_{CC} = 2.5 \text{ V}$)

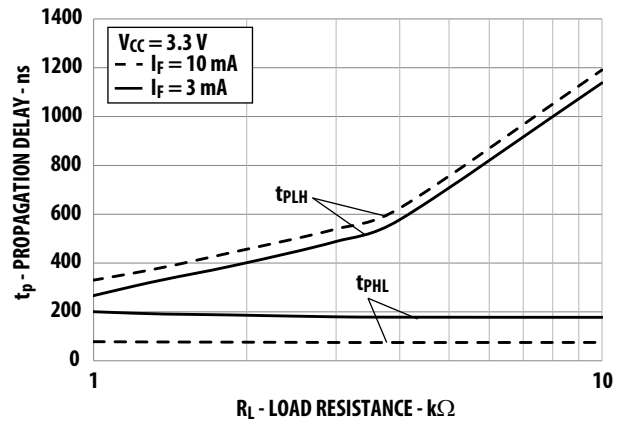


Figure 9b. Typical Propagation Delay vs. Load Resistance ($V_{CC} = 3.3 \text{ V}$)

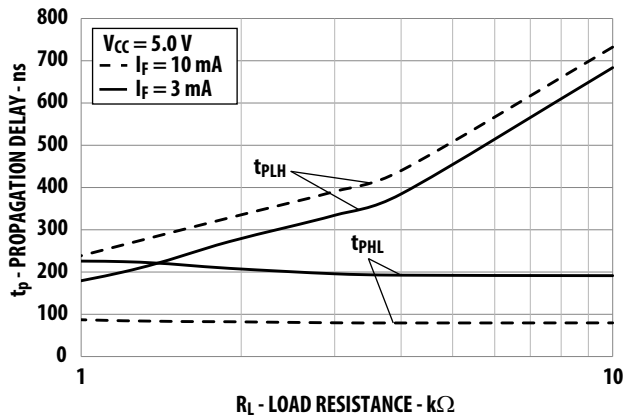


Figure 10. Typical Propagation Delay vs. Load Resistance ($V_{CC} = 5.0 \text{ V}$)

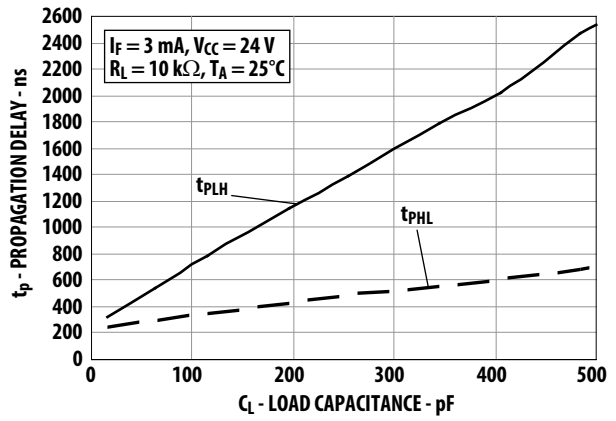


Figure 11. Typical Propagation delay vs. Load Capacitance

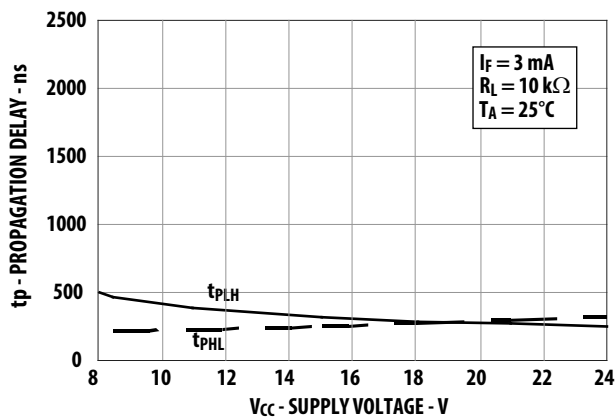


Figure 12. Typical Propagation Delay vs. Supply Voltage

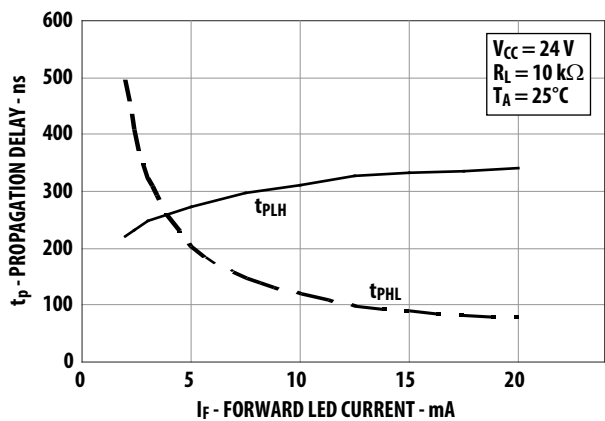


Figure 13. Typical Propagation Delay vs. Supply Current

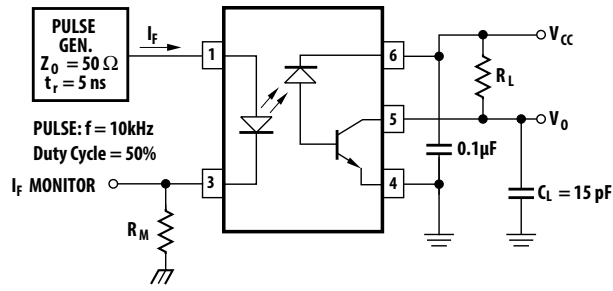
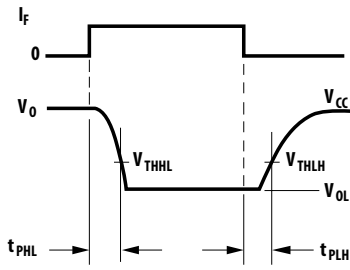


Figure 14. Switching Test Circuits

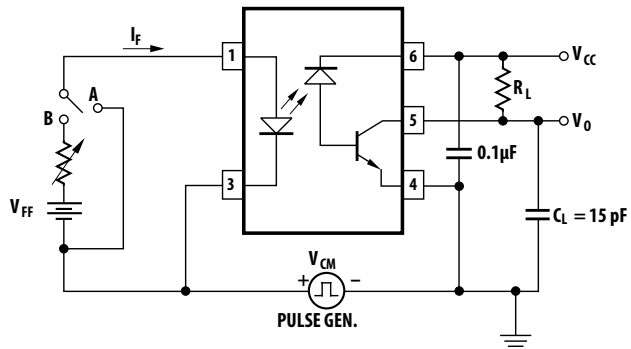
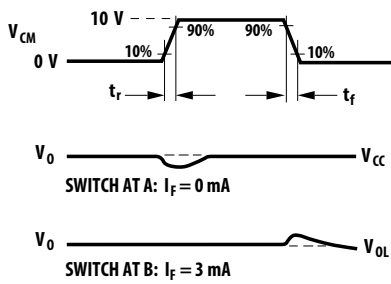


Figure 15. Test Circuit for Transient Immunity and typical waveforms

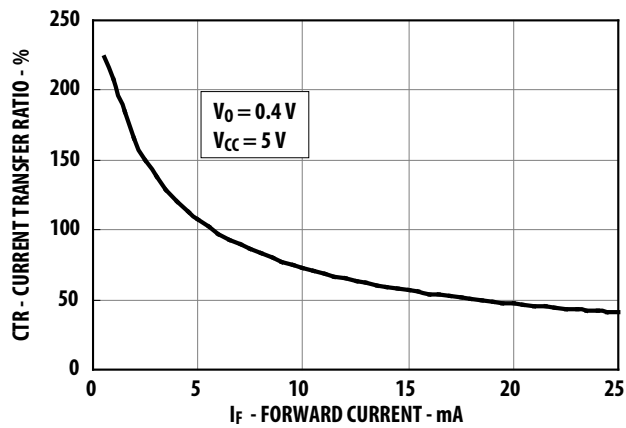


Figure 16. Current Transfer Ratio versus Input Current

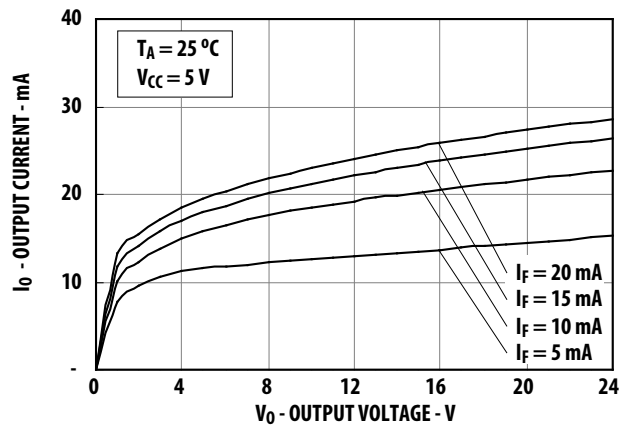


Figure 17. DC Pulse Transfer Characteristic

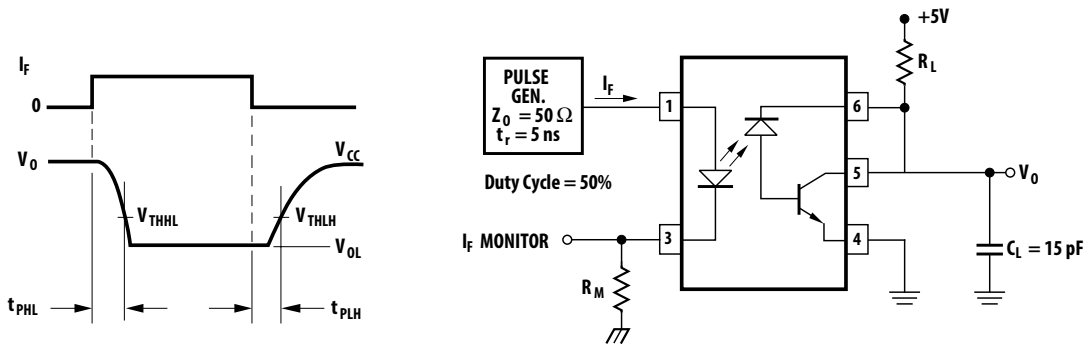


Figure 18. Switching Test Circuits (4-pin configuration)

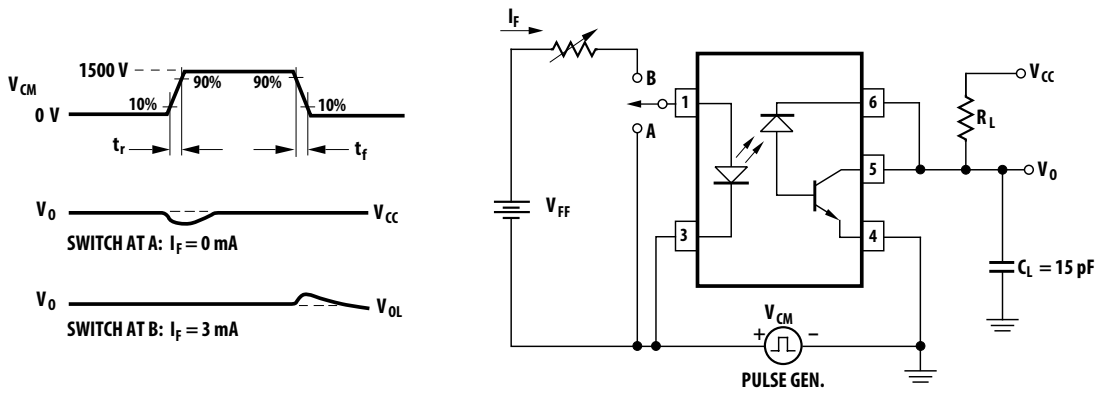


Figure 19. Test Circuit for Transient Immunity and typical waveforms (4-pin configuration)

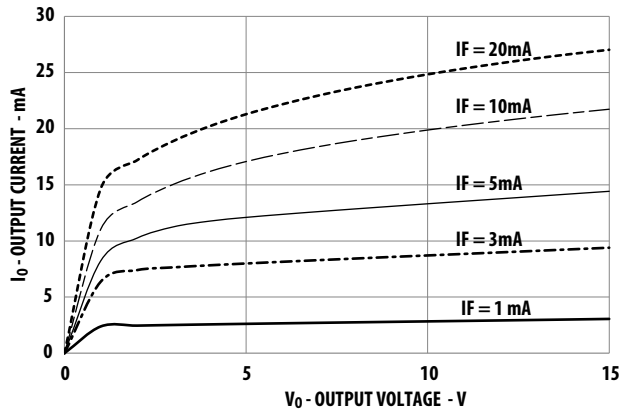


Figure 20. Output Current vs Output Voltage (4-pin configuration)

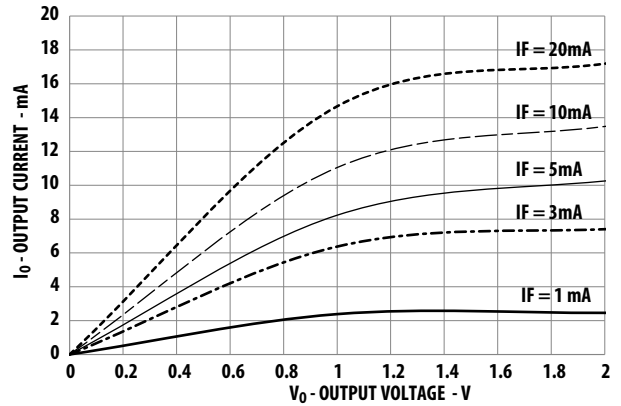


Figure 21. Low level Output Current vs Output Voltage (4-pin configuration)

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