

November 2013

FCP7N60 / FCPF7N60

N-Channel SuperFET® MOSFET

600 V, 7 A, 600 mΩ

Features

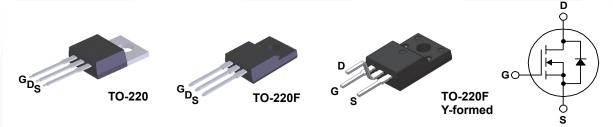
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 530 m Ω
- Ultra Low Gate Charge (Typ. Q_q = 23 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 60 pF)
- 100% Avalanche Tested
- · RoHS Compliant

Application

- LCD/LED/PDP TV
- · Solar Inverter
- · AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low onresistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FCP7N60	FCPF7N60 / FCPF7N60YDTU	Unit
V _{DSS}	Drain-Source Voltage			600		
I _D	Drain Current	- Continuous (T _C = 25 - Continuous (T _C = 10		7 4.4	7* 4.4*	A A
I _{DM}	Drain Current	- Pulsed	(Note 1)	21	21*	Α
V_{GSS}	Gate-Source voltage			± 30		V
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	230		mJ
I _{AR}	Avalanche Current		(Note 1)	7		Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	8.3		mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5		V/ns
P_{D}	Power Dissipation	(T _C = 25°C) - Derate Above 25°C		83 0.67	31 0.25	W/°C
T _{J,} T _{STG}	Operating and Storage Temperature Range		-55 to +150		°C	
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300		

^{*}Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCP7N60	FCP7N60 FCPF7N60 / FCPF7N60YDTU	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.5	4.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP7N60	FCP7N60	TO220	Tube	N/A	N/A	50 units
FCPF7N60	FCPF7N60	TO220F	Tube	N/A	N/A	50 units
FCPF7N60YDTU	FCPF7N60	TO-220F (Y-formed)	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions		Тур.	Max.	Unit
Off Charac	teristics					
BV _{DSS} Drain-Source Breakdown Voltage		$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A, } T_J = 25^{\circ}\text{C}$				V
		$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_J = 150^{\circ}\text{C}$		650		V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.6		V/°C
BV _{DS}	Drain-Source Avalanche Breakdown Voltage	V _{GS} = 0 V, I _D = 7 A		700		V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$			1 10	μ Α μ Α
I _{GSSF}	Gate-Body Leakage Current, Forward $V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
On Charac	teristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3.5 A		0.53	0.6	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 3.5 A		6		S
Dynamic C	Characteristics					
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		710	920	pF
C _{oss}	Output Capacitance			380	500	pF
C _{rss}	Reverse Transfer Capacitance			34		pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1 MHz		22	29	pF
C _{oss(eff.)}	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		60		pF
Switching	Characteristics					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 300 \text{ V}, I_D = 7 \text{ A},$		35	80	ns
t _r	Turn-On Rise Time	V_{GS} = 10 V, R_G = 25 Ω		55	120	ns
$t_{d(off)}$	Turn-Off Delay Time			75	160	ns
t _f	Turn-Off Fall Time	(Note 4)		32	75	ns
Qg	Total Gate Charge	$V_{DS} = 480 \text{ V}, I_{D} = 7 \text{ A},$		23	30	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		4.2	5.5	nC
Q _{gd}	Gate-Drain Charge	(Note 4)		11.5		nC
Drain-Sour	rce Diode Characteristics and Maximur	n Ratings			м	
I _S	Maximum Continuous Drain-Source Diode Forward Current				7	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				21	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 7 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 7 A,		360		ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt =100 A/μs		4.5		μС

Notes

 $^{{\}it 1. Repetitive\ rating: pulse-width\ limited\ by\ maximum\ junction\ temperature.}$

^{2.} I_{AS} = 3.5 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C.

^{3.} $I_{SD} \le 7$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.

^{4.} Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

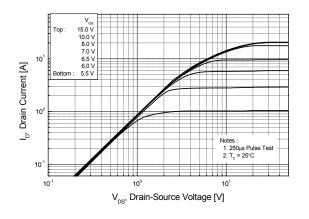


Figure 2. Transfer Characteristics

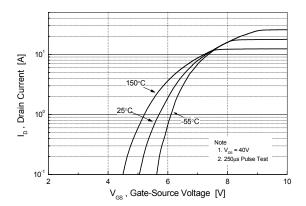


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

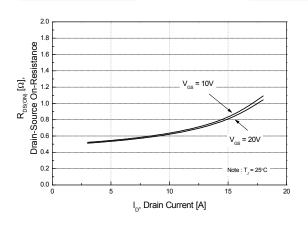


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

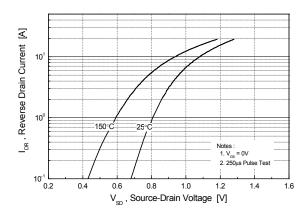


Figure 5. Capacitance Characteristics

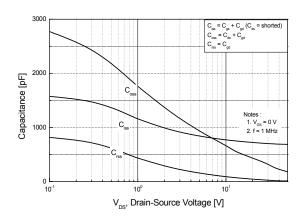
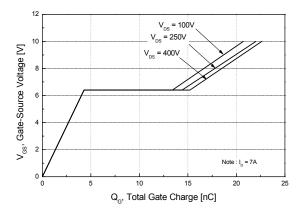


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

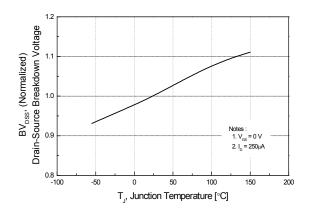


Figure 8. On-Resistance Variation vs. Temperature

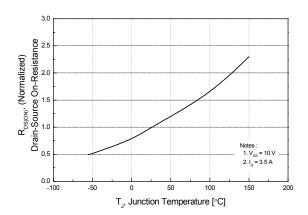


Figure 9-1. Maximum Safe Operating Area for FCP7N60

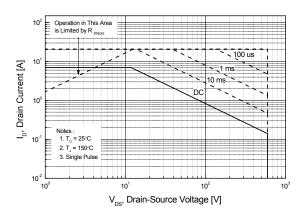


Figure 9-2. Maximum Safe Operating Area for FCPF7N60

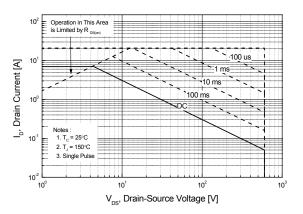
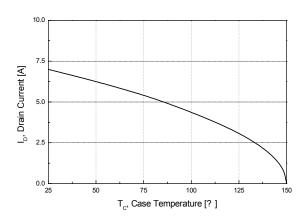


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve for FCP7N60

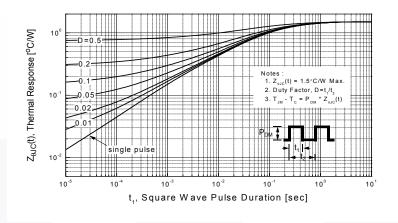
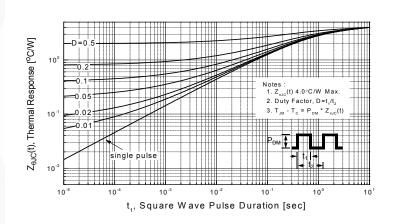


Figure 11-2. Transient Thermal Response Curve for FCPF7N60



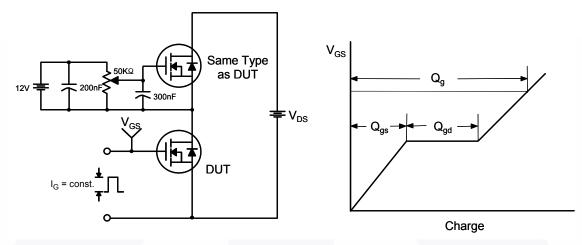


Figure 12. Gate Charge Test Circuit & Waveform

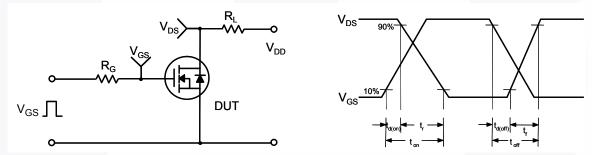


Figure 13. Resistive Switching Test Circuit & Waveforms

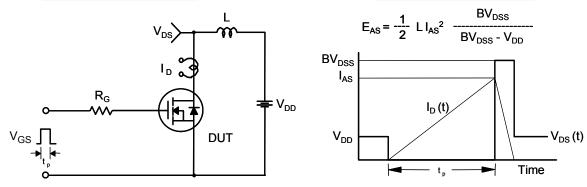


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

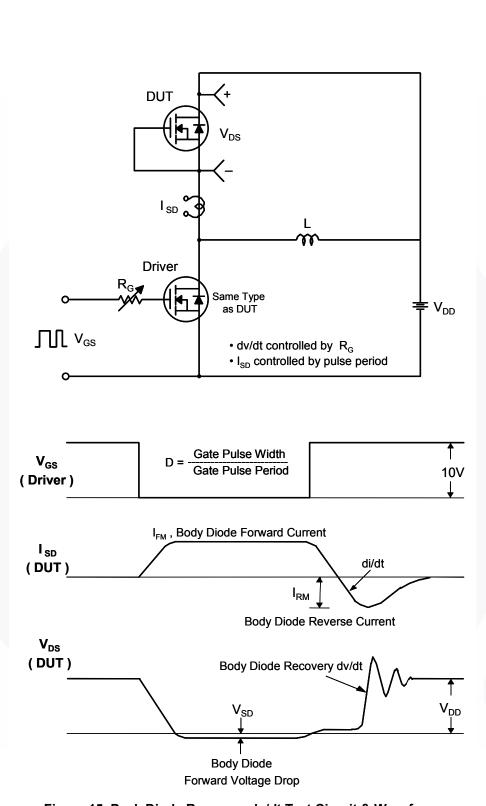
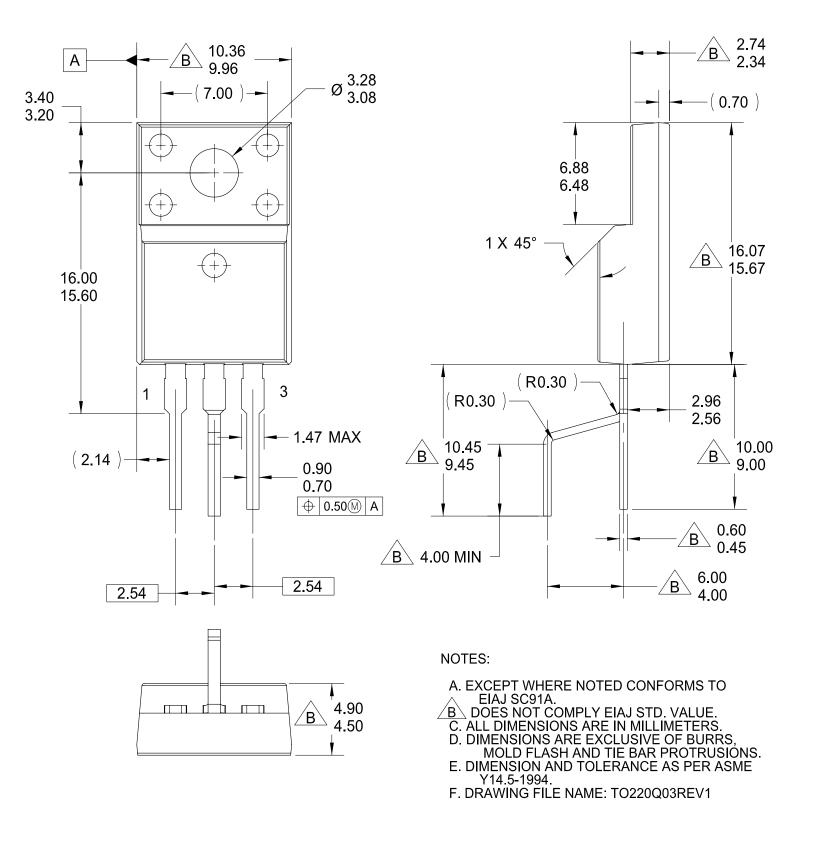
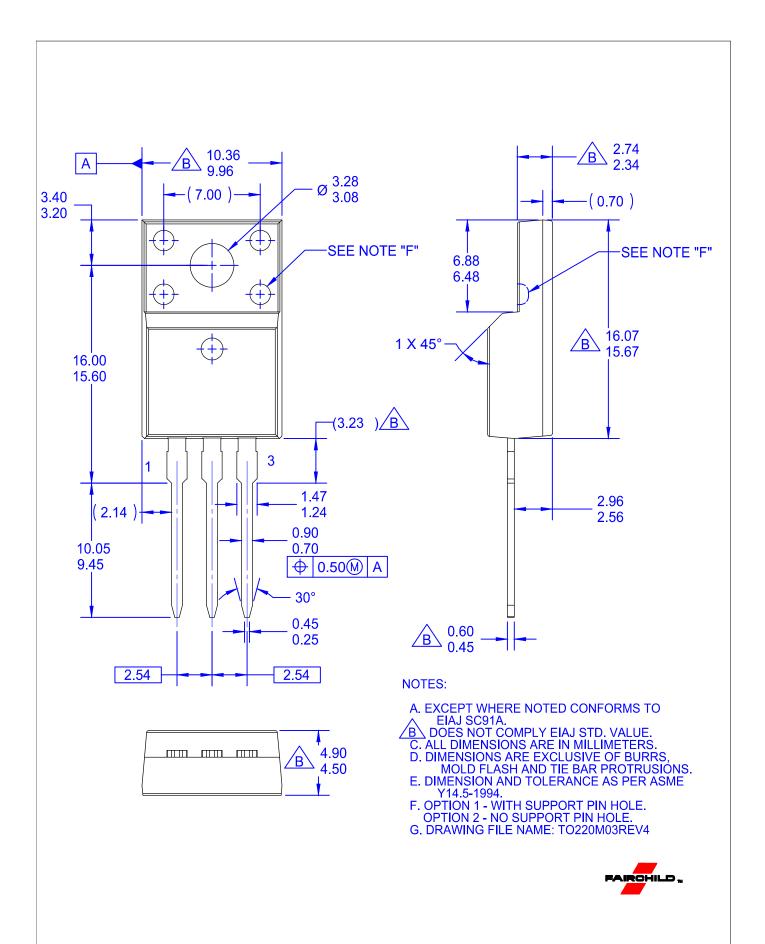


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms











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Definition of Terms				
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