

June 2014

FDMC8854

N-Channel Power Trench® MOSFET

30V, **15A**, **5.7m** Ω

Features

- Max $r_{DS(on)} = 5.7 m\Omega$ at $V_{GS} = 10 V$, $I_D = 15 A$
- Max $r_{DS(on)} = 7.6 \text{m}\Omega$ at $V_{GS} = 4.5 \text{V}$, $I_D = 13 \text{A}$
- Low Profile 1mm max in Power 33
- RoHS Compliant

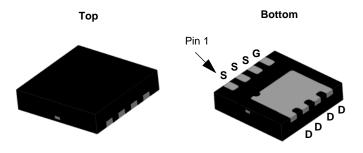


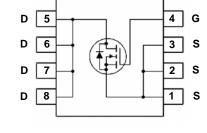
General Description

This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

Application

■ DC - DC Conversion





MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Paramete		Ratings	Units	
V _{DS}	Drain to Source Voltage			30	V
V _{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25°C		15	
I _D	-Continuous	T _A = 25°C	(Note 1a)	15	Α
	-Pulsed			100	
D	Power Dissipation	T _C = 25°C		41	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.0	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8854	FDMC8854	MLP 3.3x3.3	7"	8mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV_DSS	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		21		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24V$, $V_{GS} = 0V$			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{GS} = 0V$			±100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.9	3	٧
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-6		mV/°C
		$V_{GS} = 10V, I_D = 15A$		4.4	5.7	
r _{DS(on)}	r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 13A$		5.6	7.6	mΩ
` '	$V_{GS} = 10V, I_D = 15A, T_J = 125^{\circ}C$		6.6	9.0		
g _{FS}	Forward Transconductance	$V_{DS} = 5V, I_{D} = 15A$		60		S

Dynamic Characteristics

C _{iss}	Input Capacitance	101/1/	2560	3405	pF
Coss	Output Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1MHz	515	685	pF
C _{rss}	Reverse Transfer Capacitance	1 – 1111112	290	435	pF
R_{q}	Gate Resistance	f = 1MHz	1.3		Ω

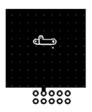
Switching Characteristics

t _{d(on)}	Turn-On Delay Time	.,		13	23	ns
t _r	Rise Time	$V_{DD} = 10V, I_{D} = 15A$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		5	10	ns
t _{d(off)}	Turn-Off Delay Time	V _{GS} = 10V, K _{GEN} = 652		31	50	ns
t _f	Fall Time			5	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V 40V L 45A		41	57	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 10V, I_D = 15A,$ $V_{GS} = 10V$		7		nC
Q_{gd}	Gate to Drain "Miller" Charge	VGS = 10 V		7		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0V, I _S = 15A (Note 2)		0.8	1.3	V
t _{rr}	Reverse Recovery Time	I _F = 15A, di/dt = 100A/μs		33	50	ns
Q _{rr}	Reverse Recovery Charge	I _F = 15A, αl/αt = 100A/μs		28	42	nC

^{1:} R_{BJA} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a. 60°C/W when mounted on a 1 in² pad of 2 oz copper

b. 135°C/W when mounted on a minimum pad of 2 oz copper



2: Pulse Test: Pulse Width < 300μ s, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

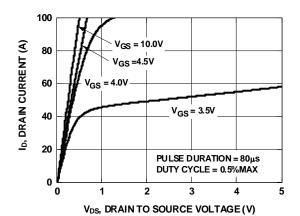


Figure 1. On-Region Characteristics

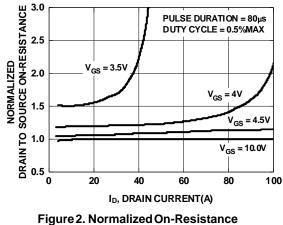


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

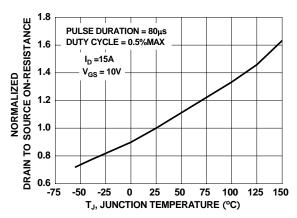


Figure 3. Normalized On-Resistance vs. Junction Temperature

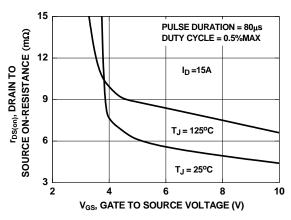


Figure 4. On-Resistance vs. Gate to Source Voltage

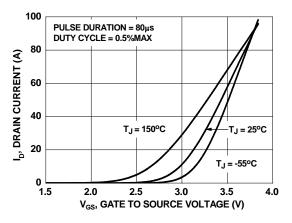


Figure 5. Transfer Characteristics

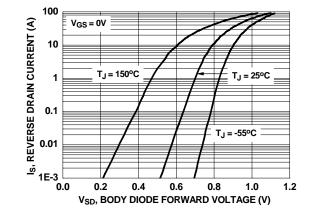


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

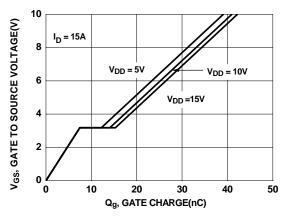


Figure 7. Gate Charge Characteristics

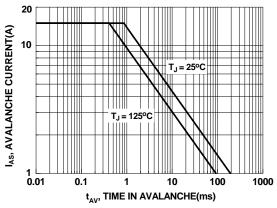


Figure 9. Unclamped Inductive Switching Capability

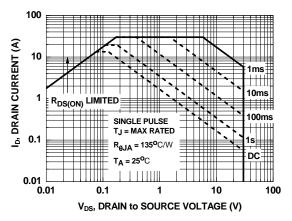


Figure 11. Forward Bias Safe Operating Area

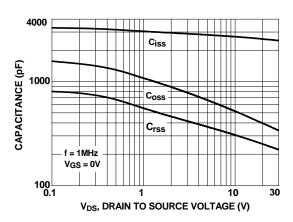


Figure 8. Capacitance vs. Drain to Source Voltage

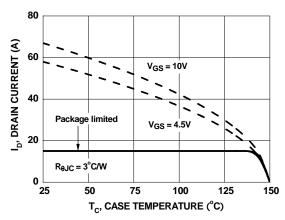


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

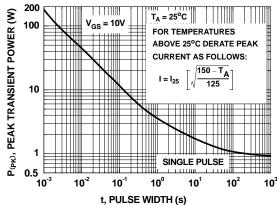


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

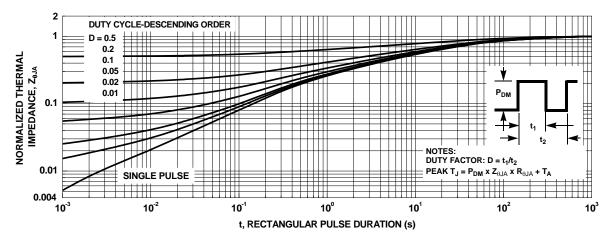
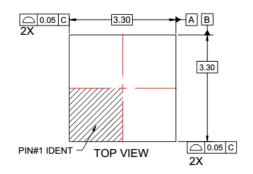
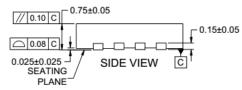
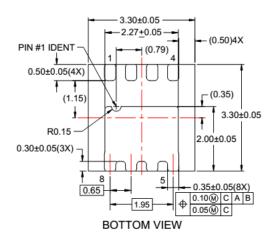


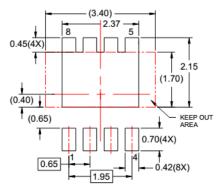
Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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