

January 2016

### FDMD8240L

# Dual N-Channel Power Trench<sup>®</sup> MOSFET 40 V, 98 A, 2.6 m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 2.6 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 23 A
- Max  $r_{DS(on)}$  = 3.95 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 19 A
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- Termination is Lead-free and RoHS Compliant

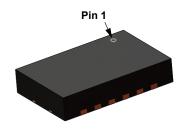


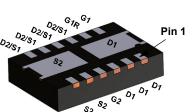
#### **General Description**

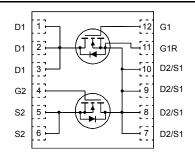
This device includes two 40V N-Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain are internally connected for half/full bridge, low source inductance package, low  $r_{DS(on)}/Qg$  FOM silicon.

#### **Applications**

- Synchronous Buck : Primary Switch of Half / Full Bridge Converter for Telecom
- Motor Bridge: Primary Switch of Half / Full bridge Converter for BLDC Motor
- MV POL: Synchronous Buck Switch







Power 3.3 x 5

### **MOSFET Maximum Ratings** T<sub>A</sub> = 25 °C unless otherwise noted.

Symbol	Param	eter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			40	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C	(Note 5)	98	
	-Continuous	T <sub>C</sub> = 100 °C	(Note 5)	62	
ID	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	23	A
	-Pulsed		(Note 4)	464	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	216	mJ
Б	Power Dissipation	T <sub>C</sub> = 25 °C		42	10/
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.1	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8240L	FDMD8240L	Power 3.3 x 5	13 "	12 mm	3000 units

Max. Units

### **Electrical Characteristics** $T_J$ = 25 $^{\circ}$ C unless otherwise noted.

Parameter

Off Characteristics							
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	40			V	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		23		mV/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V			1	μΑ	
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA	

**Test Conditions** 

#### On Characteristics

Symbol

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 μA, referenced to 25 °C		-6		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 23 A		2.0	2.6	
r <sub>DS(on)</sub>		$V_{GS} = 4.5 \text{ V}, I_D = 19 \text{ A}$		3.2	3.95	mΩ
		$V_{GS}$ = 10 V, $I_D$ = 23 A, $T_J$ = 125 °C		3.0	3.9	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 5 V, I <sub>D</sub> = 23 A		107		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V = 20 V V = 0 V		3020	4230	pF
Coss	Output Capacitance	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V f = 1 MHz		876	1230	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12		33	52	pF
$R_q$	Gate Resistance		0.1	2.8	6	Ω

#### **Switching Characteristics**

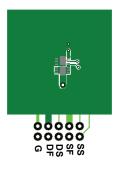
$t_{d(on)}$	Turn-On Delay Time			12	22	ns
t <sub>r</sub>	Rise Time	$V_{DD}$ = 20 V, $I_{D}$ = 23 A $V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$		8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
t <sub>f</sub>	Fall Time			9	18	ns
0	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$		40	56	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 V to 5 V$	V <sub>DD</sub> = 20 V	21	30	nC
$Q_{gs}$	Gate to Source Charge		I <sub>D</sub> = 23 A	9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	1		5		nC

#### **Drain-Source Diode Characteristics**

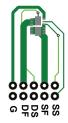
	V <sub>SD</sub>	Source to Drain Dioge Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 23 \text{ A}$ (Note 2)	8.0	1.3	V
			$V_{GS} = 0 \text{ V}, I_S = 1.6 \text{ A}$ (Note 2)	0.7	1.2	
Ī	t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 23 A. di/dt = 100 A/μs	41	65	ns
Ī	Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>F</sub> = 23 A, di/dt = 100 A/μS	21	32	nC

#### NOTES

<sup>1.</sup> R<sub>0,1A</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0,1C</sub> is guaranteed by design while R<sub>0,CA</sub> is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 130 °C/W when mounted on a minimum pad of 2 oz copper

<sup>2.</sup> Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0 %.

<sup>3.</sup> E<sub>AS</sub> of 216 mJ is based on starting T<sub>J</sub> = 25  $^{\rm o}$ C, L = 3 mH, I<sub>AS</sub> = 12 A, V<sub>DD</sub> = 40 V, V<sub>GS</sub> = 10 V. 100% tested at L = 0.1 mH, I<sub>AS</sub> = 37 A.

<sup>4.</sup> Pulsed Id please refer to Fig 11 SOA graph for more details.

<sup>5.</sup> Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

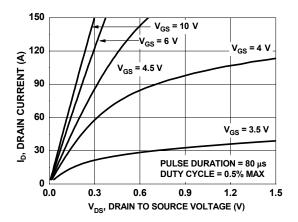


Figure 1. On-Region Characteristics

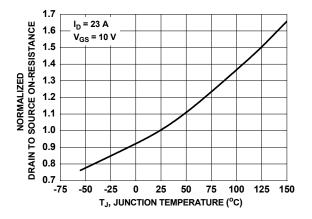


Figure 3. Normalized On Resistance vs. Junction Temperature

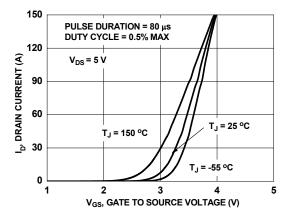


Figure 5. Transfer Characteristics

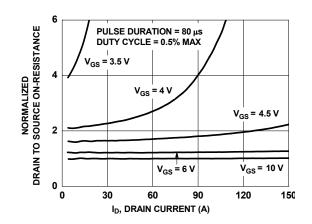


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

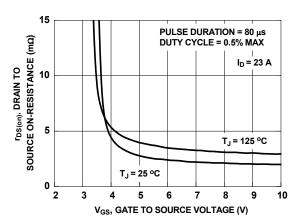


Figure 4. On Resistance vs. Gate to Source Voltage

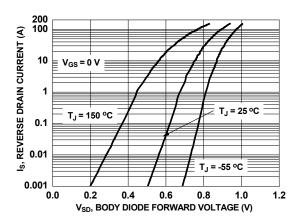


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

### **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

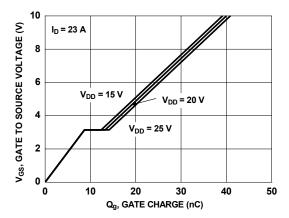


Figure 7. Gate Charge Characteristics

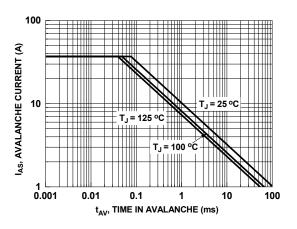


Figure 9. Unclamped Inductive Switching Capability

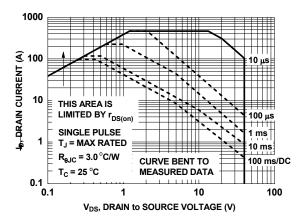


Figure 11. Forward Bias Safe Operating Area

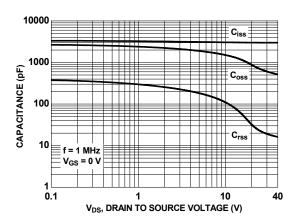


Figure 8. Capacitance vs. Drain to Source Voltage

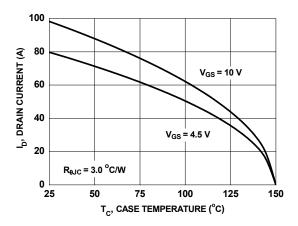


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

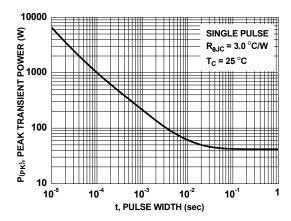


Figure 12. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** T<sub>J</sub> = 25 °C unless otherwise noted.

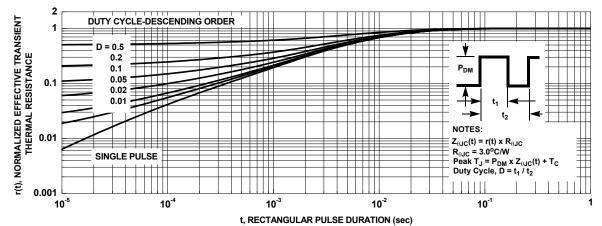
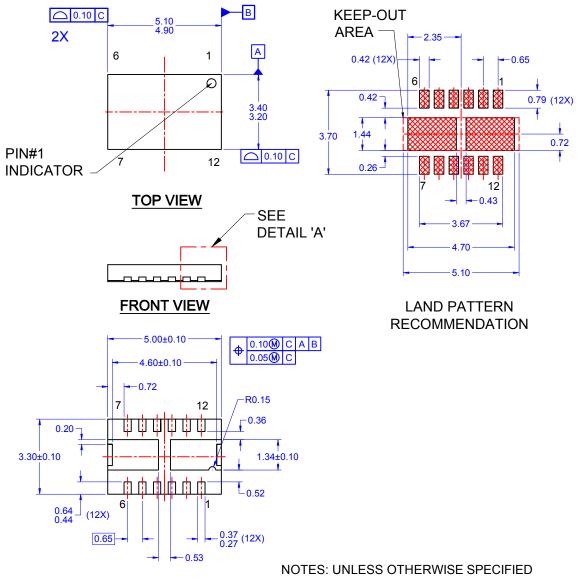


Figure 13. Junction-to-Case Transient Thermal Response Curve



#### **BOTTOM VIEW**

0.80 0.70

| 0.10 | C | E |
| 0.25 | 0.05 | SEATING
| DETAIL 'A' | SCALE: 2:1

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229 DATED 8/2012
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F) DRAWING FILE NAME: MKT-PQFN12BREV1





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