

October 2014

# **FDMS3500**

# N-Channel Power Trench<sup>®</sup> MOSFET 75V, 49A, 14.5m $\Omega$

### **Features**

- Max  $r_{DS(on)}$  = 14.5m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 11.5A
- Max  $r_{DS(on)}$  = 16.3m $\Omega$  at  $V_{GS}$  = 4.5V,  $I_D$  = 10A
- Advanced Package and Silicon combination for low r<sub>DS(on)</sub>
- MSL1 robust package design
- 100% UIL Tested
- RoHS Compliant

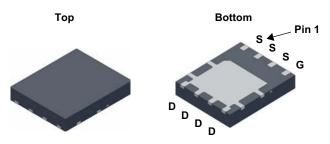


### **General Description**

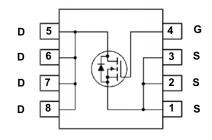
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### **Application**

■ DC - DC Conversion



Power 56



### MOSFET Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units	
$V_{DS}$	Drain to Source Voltage			75	V
V <sub>GS</sub>	Gate to Source Voltage			±20	V
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25°C		49	
	-Continuous (Silicon limited)	T <sub>C</sub> = 25°C		57	1 ,
<sup>I</sup> D	-Continuous	T <sub>A</sub> = 25°C	(Note 1a)	9.2	Α Α
	-Pulsed			100	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	384	mJ
В	Power Dissipation	T <sub>C</sub> = 25°C		96	w
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> = 25°C	(Note 1a)	2.5	] vv
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			-55 to +150	°C

### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	C/VV

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS3500	FDMS3500	Power 56	13"	12mm	3000 units

# **Electrical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter Test Conditions		Min	Тур	Max	Units
Off Chara	octeristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	75			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		71		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 60V,			1	μА
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		-6.8		mV/°C
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 11.5A		11.1	14.5	
r <sub>DS(on)</sub>	()	$V_{GS} = 4.5V, I_{D} = 10A$		12.8	16.3	mΩ
		$V_{GS} = 10V$ , $I_D = 11.5A$ , $T_J = 125$ °C		17.6	23.0	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 5V, I <sub>D</sub> = 11.5A		56		S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	\\ - 40\\ \\ - 0\\	3580	4765	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 40V, V_{GS} = 0V,$ f = 1MHz	225	300	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1101112	120	175	pF
$R_g$	Gate Resistance	f = 1MHz	1.2		Ω

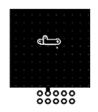
### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time				16	29	ns
t <sub>r</sub>	Rise Time		$V_{DD}$ = 40V, $I_{D}$ = 11.5A, $V_{GS}$ = 10V, $R_{GEN}$ = 6 $\Omega$		9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10V, $R_{GEN}$			48	77	ns
t <sub>f</sub>	Fall Time				6	11	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0V to 10V			65	91	nC
Qg	Total Gate Charge	$V_{GS} = 0V \text{ to } 5V$	V <sub>DD</sub> = 40V,		34	48	nC
Q <sub>gs</sub>	Gate to Source Charge		I <sub>D</sub> = 11.5A		9.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				11.6		nC

### **Drain-Source Diode Characteristics**

Ved Source to Drain Dioge Forward Voltage	Source to Drain Diade Forward Voltage	$V_{GS} = 0V, I_{S} = 11.5A$ (Note 2)	(	8.0	1.3	V
	$V_{GS} = 0V, I_S = 2.1A$ (Note 2)	(	0.7	1.2	, <b>v</b>	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 11.5A, di/dt = 100A/μs		38	60	ns
Q <sub>rr</sub>	Reverse Recovery Charge	-1F - 11.5A, α/αι - 100A/μs		45	72	nC

<sup>1.</sup> R<sub>0,1A</sub> is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0,1C</sub> is guaranteed by design while R<sub>0,0C</sub> is determined by the user's board design.



a. 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

<sup>2.</sup> Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

<sup>3.</sup> Starting  $T_J$  = 25°C, L = 3mH,  $I_{AS}$  = 16A,  $V_{DD}$  = 75V,  $V_{GS}$  = 10V

### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

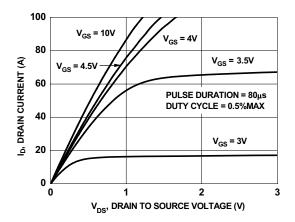


Figure 1. On-Region Characteristics

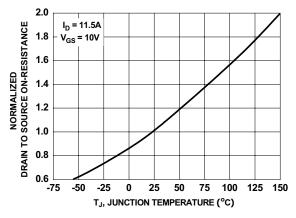


Figure 3. Normalized On-Resistance vs Junction Temperature

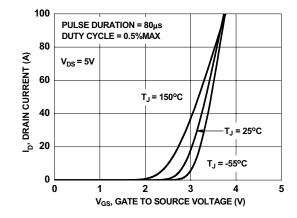


Figure 5. Transfer Characteristics

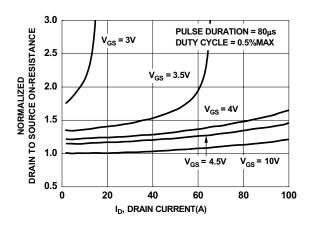


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

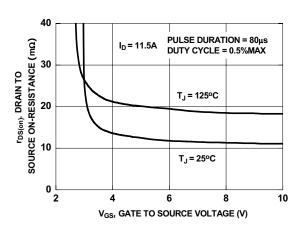


Figure 4. On-Resistance vs Gate to Source Voltage

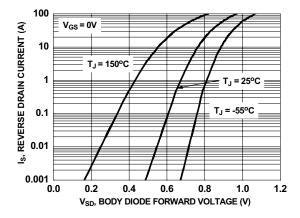


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

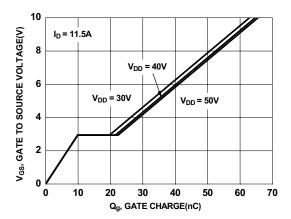


Figure 7. Gate Charge Characteristics

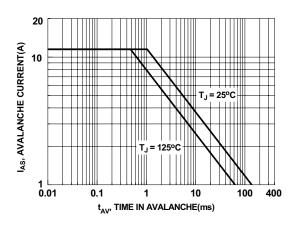


Figure 9. Unclamped Inductive Switching Capability

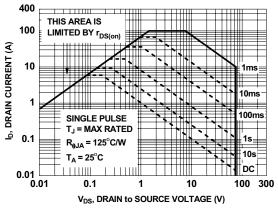


Figure 11. Forward Bias Safe Operating Area

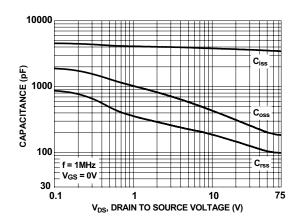


Figure 8. Capacitance vs Drain to Source Voltage

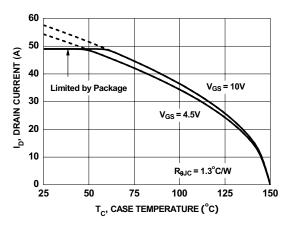


Figure 10. Maximum Continuous Drain Current vs Case Temperature

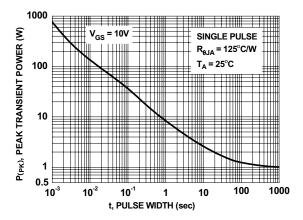


Figure 12. Single Pulse Maximum Power Dissipation

## Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

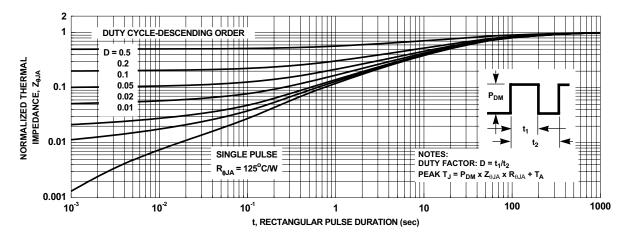


Figure 13. Transient Thermal Response Curve







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