

March 2015

FDMS8350L

N-Channel PowerTrench[®] MOSFET 40 V, 290 A, 0.85 m Ω

Features

- Max $r_{DS(on)} = 0.85 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 47 \text{ A}$
- Max $r_{DS(on)} = 1.2 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 38 \text{ A}$
- Advanced Package and Silicon combination for low r_{DS(on)} and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

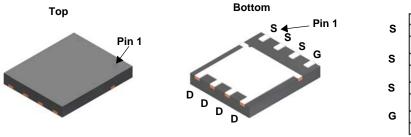


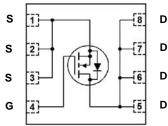
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch





Power 56

MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parame	ter		Ratings	Units
V_{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage			±20	V
I _D	Drain Current -Continuous	T _C = 25 °C	(Note 5)	290	
	-Continuous	T _C = 100 °C	(Note 5)	183	A
	-Continuous	T _A = 25 °C	(Note 1a)	47	_ A
	-Pulsed		(Note 4)	1737	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	800	mJ
В	Power Dissipation	T _C = 25 °C		113	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.7	VV
T_J , T_{STG}	Operating and Storage Junction Temperat	ture Range		-55 to + 150	°C

Thermal Characteristics

Г				
	$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.1	°C/W
	$R_{\theta,IA}$	Thermal Resistance, Junction to Ambient (Note 1a	45	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8350L	FDMS8350L	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		25		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-6		mV/°C
r _{DS(on)}		V _{GS} = 10 V, I _D = 47 A		0.71	0.85	
	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 38 \text{ A}$		0.91	1.2	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 47 \text{ A}, T_J = 125 ^{\circ}\text{C}$		0.94	1.2	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 47 A		260		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 00 V V 0 V		12500	17500	pF
C _{oss}	Output Capacitance	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		3430	4800	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12		136	190	pF
R_{α}	Gate Resistance		0.1	1	3	Ω

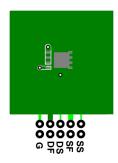
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		29	47	ns
t _r	Rise Time	V _{DD} = 20 V, I _D = 47 A,	22	36	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	83	133	ns
t _f	Fall Time		18	33	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V	173	242	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V} V_{DD} = 20 \text{ V},$	80	113	nC
Q _{gs}	Gate to Source Charge	I _D = 47 A	30		nC
Q_{gd}	Gate to Drain "Miller" Charge		18		nC

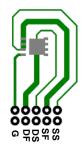
Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2.1 \text{ A}$ (Note 2)	C).65	1.2	V
	Source to Drain blode 1 of ward voltage	$V_{GS} = 0 \text{ V}, I_{S} = 47 \text{ A}$ (Note 2)	C	0.76	1.3	\ \
t _{rr}	Reverse Recovery Time	-I _F = 47 A, di/dt = 100 A/μs		72	116	ns
Q _{rr}	Reverse Recovery Charge			64	103	nC
Mataa						

Notes:
1. R_{8JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{8CA} is determined by the user's board design.



a. 45 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 115 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. E_{AS} of 800 mJ is based on starting $T_J = 25$ °C, L = 1 mH, $I_{AS} = 40$ A, $V_{DD} = 36$ V, $V_{GS} = 10$ V. 100% test at L = 0.1 mH, $I_{AS} = 86$ A.
- 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted

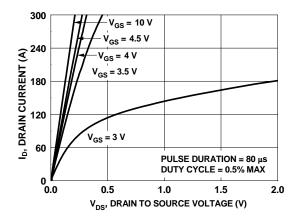


Figure 1. On Region Characteristics

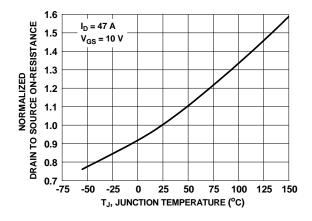


Figure 3. Normalized On Resistance vs Junction Temperature

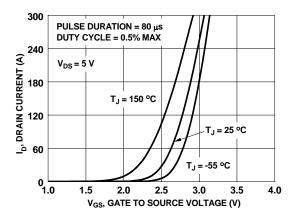


Figure 5. Transfer Characteristics

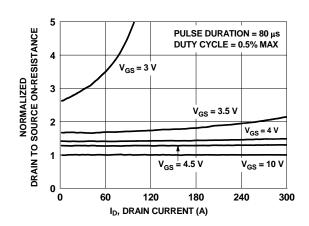


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

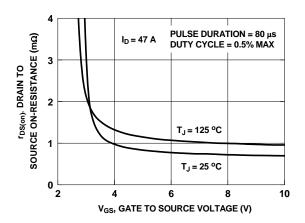


Figure 4. On-Resistance vs Gate to Source Voltage

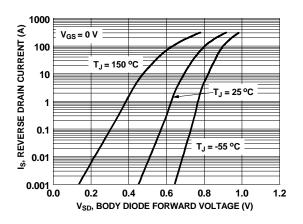


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

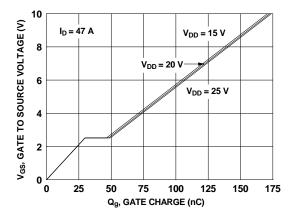


Figure 7. Gate Charge Characteristics

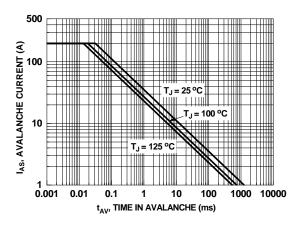


Figure 9. Unclamped Inductive Switching Capability

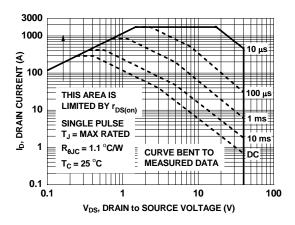


Figure 11. Forward Bias Safe Operating Area

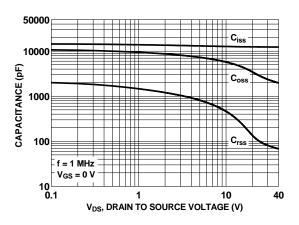


Figure 8. Capacitance vs Drain to Source Voltage

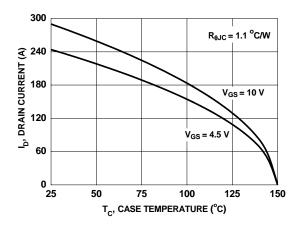


Figure 10. Maximum Continuous Drain Current vs Case Temperature

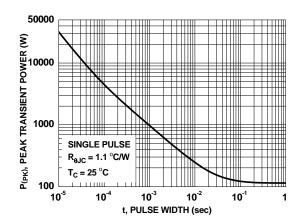


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

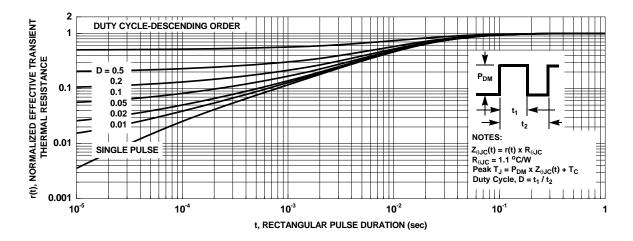
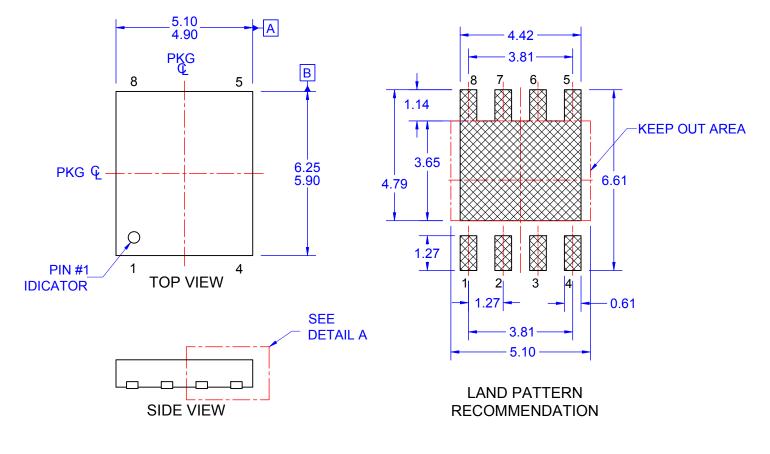
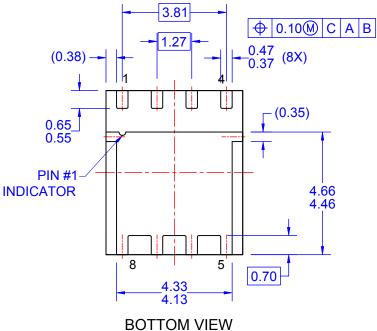
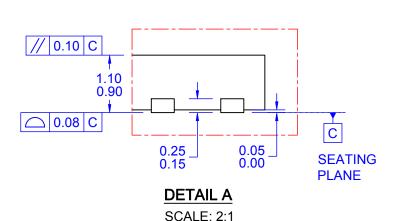


Figure 13. Junction-to-Case Transient Thermal Response Curve







NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F) DRAWING FILE NAME: PQFN08JREV3.







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Definition of Terms

Definition of Terms		
Datasheet Identification		Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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