

October 2013

# FDP55N06 / FDPF55N06

# N-Channel UniFET<sup>™</sup> MOSFET 60 V, 55 A, 22 mΩ

#### **Features**

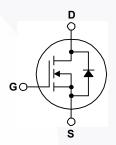
- $R_{DS(on)}$  = 22  $m\Omega$  @ $V_{GS}$  = 10 V,  $I_D$  = 27.5 A
- Low Gate Charge (Typ. 30 nC)
- Low Crss (Typ. 60 pF)
- · 100% Avalanche Tested

# **Description**

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter		FDP55N06	FDPF55N06	Unit
V <sub>DSS</sub>	Drain-Source Voltage		60		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C	)	55	55 *	Α
	- Continuous (T <sub>C</sub> = 100°C)		34.8	34.8 *	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	220	220 *	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 25		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		480		mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	55		Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		11.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
$P_{D}$	Power Dissipation (T <sub>C</sub> = 25°C)		114	48	W
	- Derate above 25°C		0.9	0.4	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150		°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

<sup>\*</sup> Drain current limited by maximum junction temperature

#### **Thermal Characteristics**

Symbol	Parameter	FDP55N06	FDPF55N06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.1	2.58	°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max,	62.5	62.5	°C/W

# **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP55N06	FDP55N06	TO-220	Tube	N/A	50 units
FDPF55N06	FDPF55N06	TO-220F	Tube	N/A	50 units

# **Electrical Characteristics** $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Charac	teristics				ı	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V, } I_D = 250  \mu\text{A}$	60			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		0.05		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μА
		V <sub>DS</sub> = 48 V, T <sub>C</sub> = 150°C			10	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Charact	teristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 27.5 A		0.018	0.022	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 27.5 A		33		S
Dynamic Cl	haracteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		1160	1510	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		375	490	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			60	90	pF
Switching C	Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_{D} = 55 \text{ A},$		30	65	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		130	265	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		/	70	150	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		95	195	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 48 V, I <sub>D</sub> = 55A,		30	37	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		6.5		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		7.5		nC
Drain-Source	Legional Diode Characteristics and Maximum Ratings	5		1		
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				55	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				220	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 55 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 55 A,		40		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		55		μС

#### Notes

<sup>1.</sup> Repetitive Rating : Pulse width limited by maximum junction temperature

<sup>2.</sup> L = 5.6mH, I $_{AS}$  = 55A, V $_{DD}$  = 50V, R $_{G}$  = 25  $\Omega$ , Starting T $_{J}$  = 25°C

<sup>3.</sup> I  $_{SD} \leq$  55A, di/dt  $\leq$  200A/ $\mu$ s, V  $_{DD} \leq$  BV  $_{DSS,}$  Starting T  $_{J}$  = 25°C

<sup>4.</sup> Essentially independent of operating temperature

#### **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

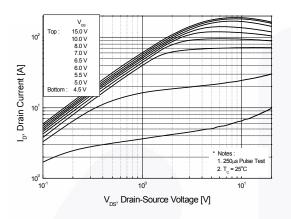


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

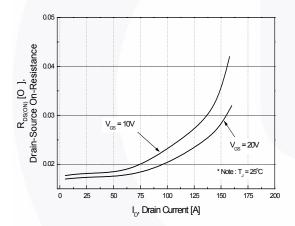


Figure 5. Capacitance Characteristics

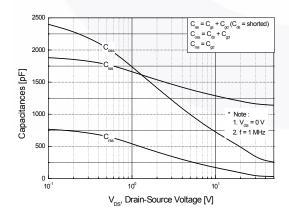


Figure 2. Transfer Characteristics

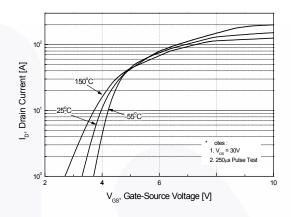


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

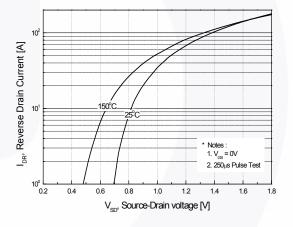
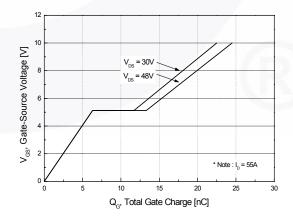


Figure 6. Gate Charge Characteristics



# **Typical Performance Characteristics (Continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

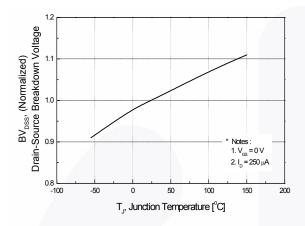


Figure 8. On-Resistance Variation vs. Temperature

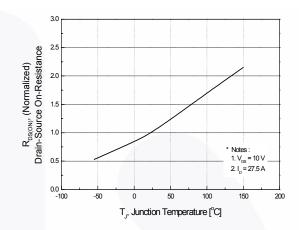


Figure 9-1. Maximum Safe Operating Area for FDP55N06

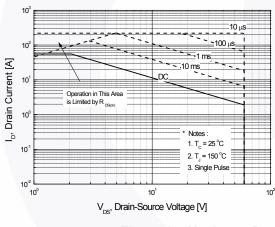


Figure 9-2. Maximum Safe Operating Area for FDPF55N06

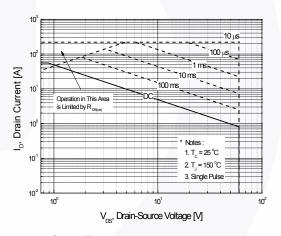
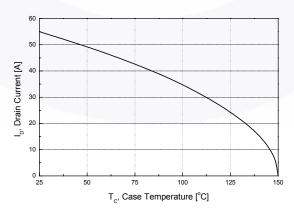


Figure 10. Maximum Drain Current vs. Case Temperature



# **Typical Performance Characteristics** (Continued)

Figure 11-1. Transient Thermal Response Curve for FDP55N06

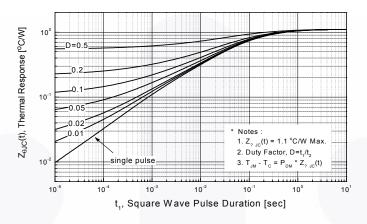


Figure 11-2. Transient Thermal Response Curve for FDPF55N06

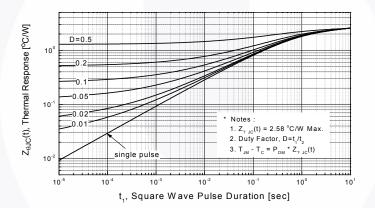


Figure 12. Gate Charge Test Circuit & Waveform

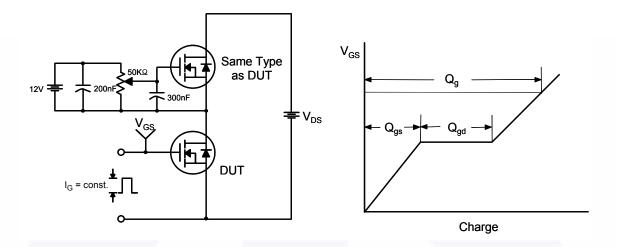


Figure 13. Resistive Switching Test Circuit & Waveforms

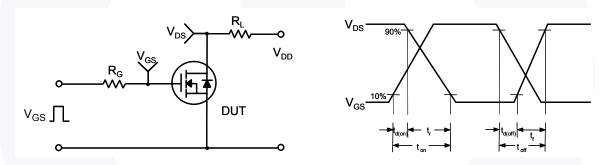
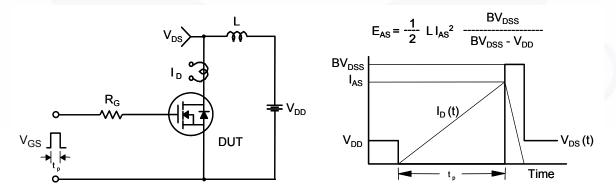
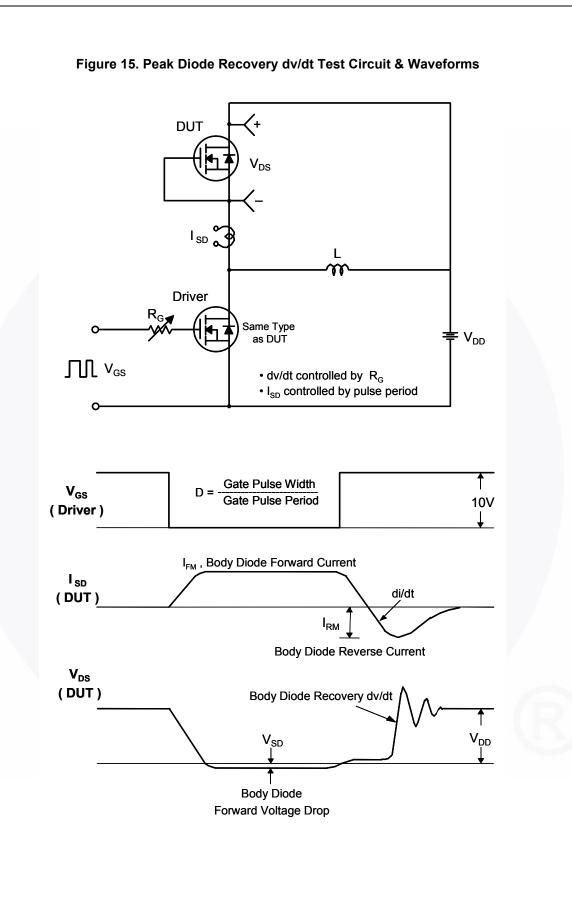


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms





#### **Mechanical Dimensions**

# TO-220 3L

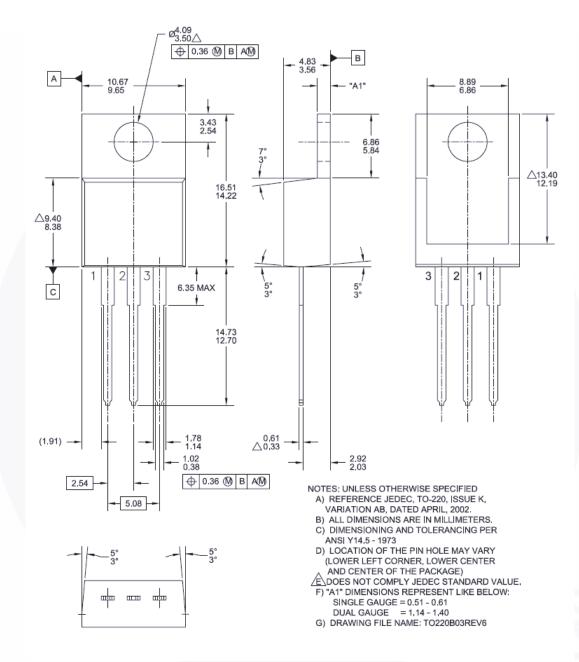


Figure 16. TO-220, Molded, 3Lead, Jedec Variation AB

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Dimension in Millimeters

#### **Mechanical Dimensions**

# TO-220F 3L

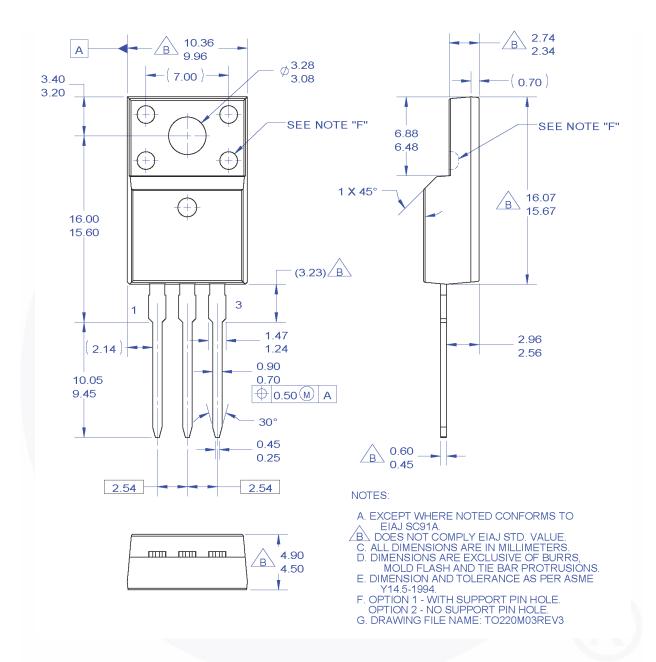


Figure 17. TO220, Molded, 3LD, Full Pack, EIAJ SC91, Straight Lead

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Dimension in Millimeters





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