

October 2013

# FDPF5N50NZU

# N-Channel UniFET<sup>TM</sup> II Ultra FRFET<sup>TM</sup> MOSFET 500 V, 3.9 A, 2.0 $\Omega$

### **Features**

- $R_{DS(on)}$  = 1.7  $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 1.95 A
- Low Gate Charge (Typ. 9 nC)
- Low C<sub>rss</sub> (Typ. 4 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Improved Capability
- · RoHS Compliant

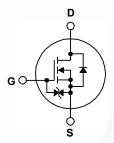
# **Applications**

- LCD/LED TV
- · Lighting
- · Uninterruptible Power Supply
- · AC-DC Power Supply

# Description

UniFET<sup>TM</sup> II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. UniFET II Ultra FRFET<sup>TM</sup> MOSFET has much superior body diode reverse recovery performance. Its  $t_{\rm rr}$  is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET II Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





# MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter			FDPF5N50NZU	Unit
V <sub>DSS</sub>	Drain to Source Voltage	!		500	V
V <sub>GSS</sub>	Gate to Source Voltage			±25	V
	Drain Current	- Continuous (T <sub>C</sub>	= 25°C)	3.9*	^
ID	Drain Current	- Continuous (T <sub>C</sub>	= 100°C)	2.3*	Α
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	15*	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		(Note 2)	135	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	3.9	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note		(Note 1)	7.8	mJ
dv/dt	Peak Diode Recovery d	Recovery dv/dt (Note 3)		20	V/ns
D	Dawer Dissipation	$(T_C = 25^{\circ}C)$		30	W
$P_D$	Power Dissipation - Der		5°C	0.24	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage	Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

<sup>\*</sup>Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FDPF5N50NZU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	C/VV

# **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPF5N50NZU	FDPF5N50NZU	TO-220F	Tube	N/A	50 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A$ , $V_{GS} = 0V$ , $T_C = 25^{\circ}C$	500	-	-	V
ΔBV <sub>DSS</sub> / ΔΤ <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	-	0.5	-	V/°C
1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V	-	-	25	μА
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 400V, V_{GS} = 0V, T_{C} = 125^{\circ}C$	-	-	250	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$	-	-	±10	μΑ

### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.95A	-	1.7	2.0	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1.95A	-	4.2	-	S

# **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 05V V 0V	-	365	485	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1MHz		50	65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	T = TIVITIZ	-\	4	8	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V		- \	9	12	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	$V_{DS} = 400V I_{D} = 3.9A$	-	2	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	V <sub>GS</sub> = 10V (Note 4)	-	4	-	nC

# **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	12	35	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 250V, I_{D} = 3.9A$	-	19	50	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10V, $R_{GEN}$ = 25 $\Omega$	-	31	70	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	22	55	ns

### **Drain-Source Diode Characteristics**

IS	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	3.9	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	15	Α
$V_{SD}$	Drain to Source Diode Forward Voltage V <sub>GS</sub> = 0V, I <sub>SD</sub> = 3.9A		-	-	1.6	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 3.9A	-	45	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge dI <sub>F</sub> /dt = 100A/μs		-	33	/ -	nC

#### Notes:

- Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. L = 18mH, I<sub>AS</sub> = 3.9A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 $\Omega$ , Starting T<sub>J</sub> = 25 $^{\circ}$ C
- 3. I\_{SD}  $\leq$  3.9A, di/dt  $\leq$  200A/µs, V\_{DD}  $\leq$  BV\_DSS, Starting T\_J = 25°C
- Essentially Independent of Operating Temperature Typical Characteristics

# **Typical Characteristics**

Figure 1. On-Region Characteristics

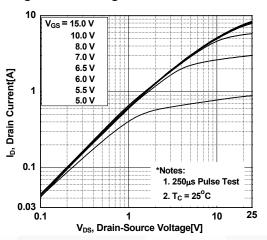


Figure 3. On-Resistance Variation vs. **Drain Current and Gate Voltage** 

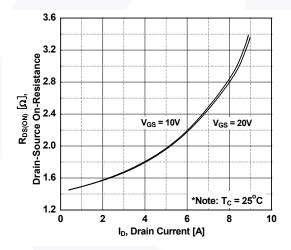


Figure 5. Capacitance Characteristics

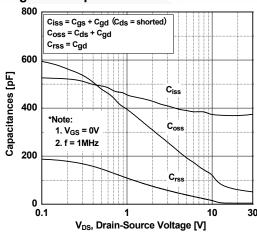


Figure 2. Transfer Characteristics

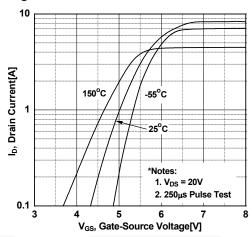


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

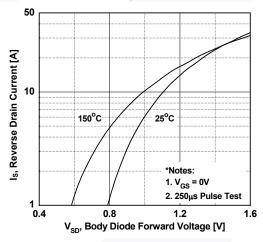
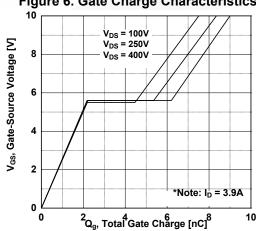


Figure 6. Gate Charge Characteristics



# **Typical Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

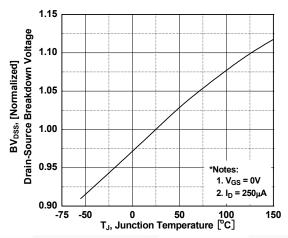


Figure 8. Maximum Safe Operating Area vs. Case Temperature-FDPF5N50NZU

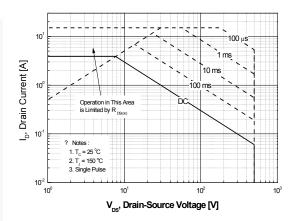


Figure 9. Maximum Drain Current

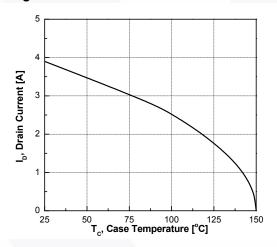


Figure 10. Transient Thermal Response Curve-FDPF5N50NZU

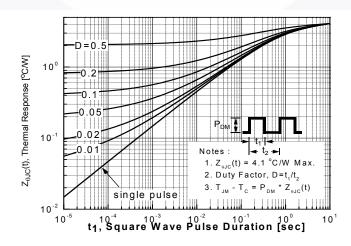


Figure 11. Gate Charge Test Circuit & Waveform

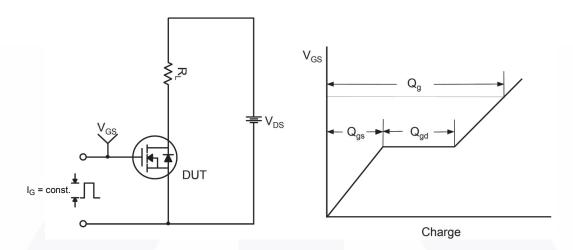


Figure 12. Resistive Switching Test Circuit & Waveforms

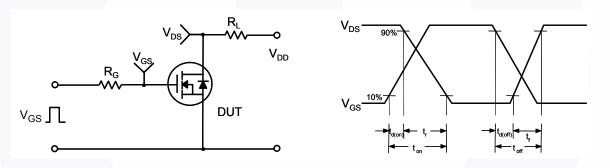
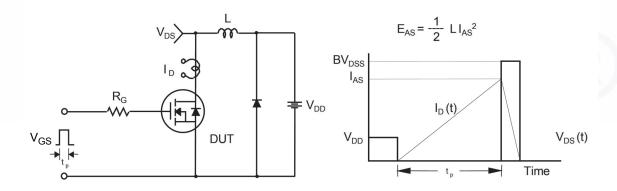


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms



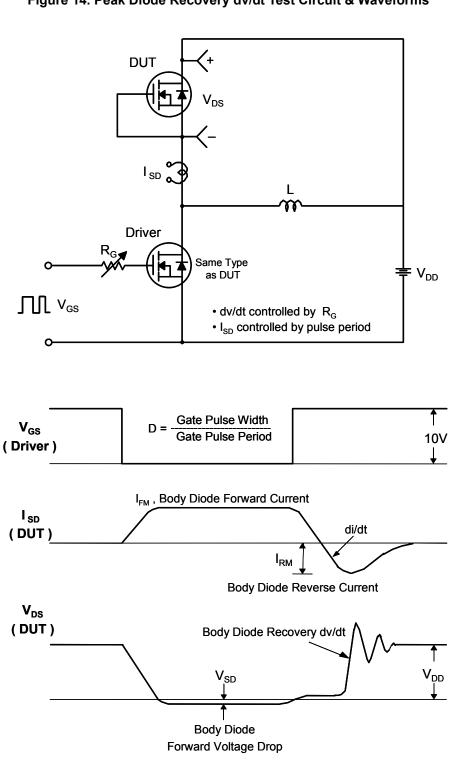


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

### **Mechanical Dimensions**

# TO-220F 3L

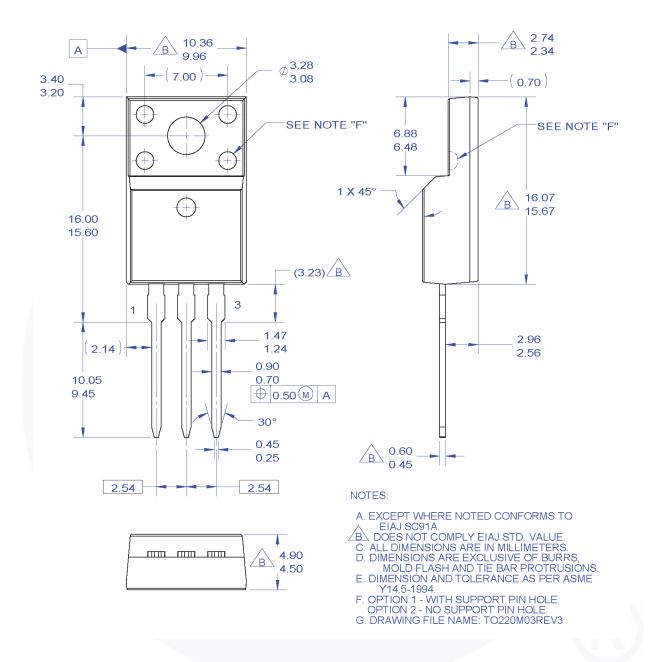


Figure 15. TO220, Molded, 3LD, Full Pack, EIAJ SC91, Straight Lead

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Dimension in Millimeters





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