December 2013

### FQP2P40

# P-Channel QFET $^{\rm @}$ MOSFET -400 V, -2.0 A, 6.5 $\Omega$

### **Description**

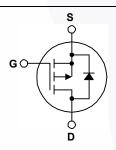
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on complimentary half bridge.

#### **Features**

- -2.0 A, -400 V,  $R_{DS(on)}$  = 6.5  $\Omega$  (Max.) @  $V_{GS}$  = -10 V
- Low Gate Charge (Typ. 10 nC)
- · Low Crss (Typ. 6.5 pF)
- · Fast Switching
- 100% Avalanche Tested
- · Improved dv/dt Capability





### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQP2P40_F080	Unit	
$V_{DSS}$	Drain-Source Voltage		-400	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C	C)	-2.0	Α	
	- Continuous (T <sub>C</sub> = 100°C)		-1.27	Α	
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	-8.0	Α	
$V_{GSS}$	Gate-Source Voltage		± 30	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		120	mJ	
l <sub>AR</sub>	Avalanche Current	(Note 1)	-2.0	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1		6.3	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)		-4.5	V/ns	
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)		63	W	
	- Derate Above 25°C		0.51	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C	

### **Thermal Characteristics**

Symbol	Parameter	FQP2P40_F080	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.98	°C/W	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP2P40_F080	FQP2P40	TO-220	Tube	N/A	N/A	50 units

### Florical Characteristics

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-400			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, Referenced to 25°C	-	-		V/°C
I <sub>DSS</sub>	Zero Osto Veltoro Broin Ormant	$V_{DS} = -400 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -320 \text{ V}, T_{C} = 125 ^{\circ}\text{C}$			-1	μА
	Zero Gate Voltage Drain Current				-10	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	-		-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	I		100	nA
On Cha	aracteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-3.0		-5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.0 A		5.0	6.5	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -50 V, I <sub>D</sub> = -1.0 A	1	1.42		S
	ic Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V},$		270	350	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		45	60	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	6.5	8.5	pF
Switchi	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -200 V, I <sub>D</sub> = -2.0 A,		9	30	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = -10 \text{ V}, R_{G} = 25 \Omega$	-	33	75	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	7 GS 10 V, NG 20 22	-	22	55	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	25	60	ns
Qg	Total Gate Charge	V <sub>DS</sub> = -320 V, I <sub>D</sub> = -2.0 A,	-	10	13	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -10 V	-	2.1		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)	-	5.5		nC
	Source Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				-2.0	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		-		-8.0	Α
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -2.0 \text{ A}$	-		-5.0	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = -2.0 \text{ A},$	-	250		ns
$Q_{rr}$	Reverse Recovery Charge	$dI_{F} / dt = 100 A/\mu s$		0.85		μС

- 1. Repetitive rating : pulse-width limited by maximum junction temperature.
- 2. L = 52.5 mH, I<sub>AS</sub> = -2.0 A, V<sub>DD</sub> = -50 V, R<sub>G</sub> = 25  $\Omega$ , Starting T<sub>J</sub> = 25°C.
- 3. I  $_{SD} \leq$  -2.0 A, di/dt  $\leq$  200 A/µs, V  $_{DD} \leq$  BV  $_{DSS,}$  Starting T  $_{J}$  = 25°C.
- 4. Essentially independent of operating temperature.

### **Typical Performance Characteristics**

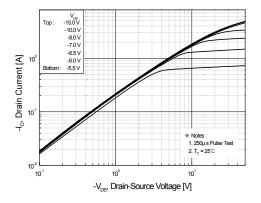


Figure 1. On-Region Characteristics

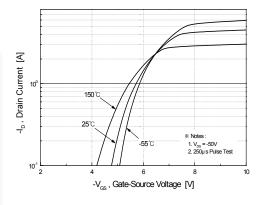


Figure 2. Transfer Characteristics

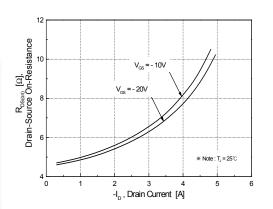


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

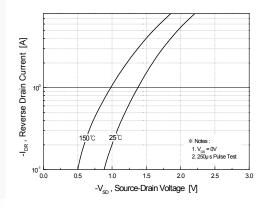


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

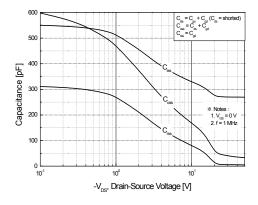


Figure 5. Capacitance Characteristics

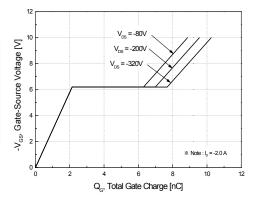
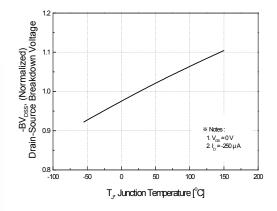


Figure 6. Gate Charge Characteristics

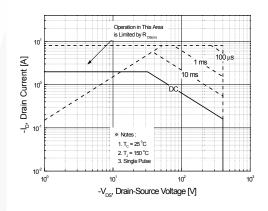
### Typical Performance Characteristics (Continued)



25 (Nomalized) 1.5 (Nomalized)

Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



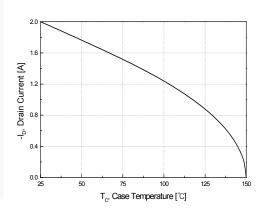


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

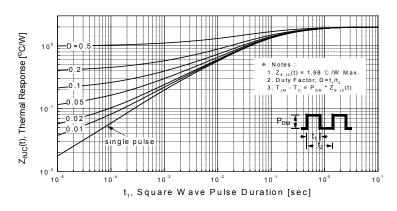


Figure 11. Transient Thermal Response Curve

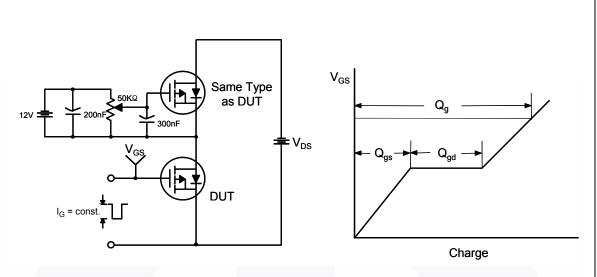


Figure 12. Gate Charge Test Circuit & Waveform

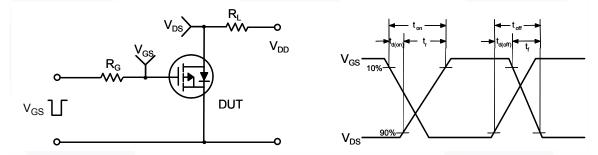


Figure 13. Resistive Switching Test Circuit & Waveforms

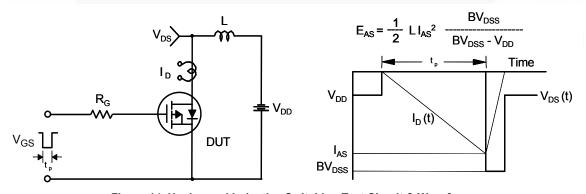
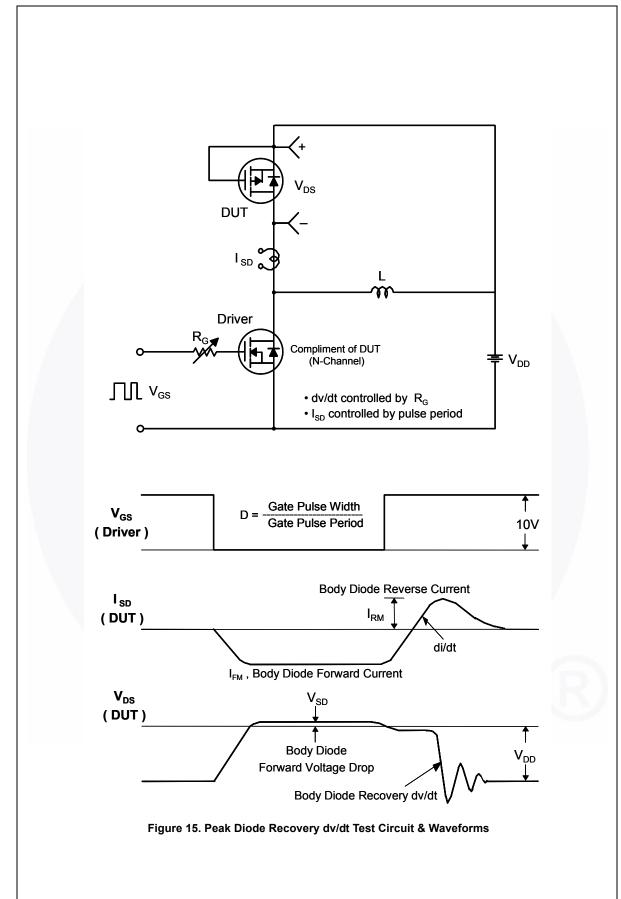


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



### **Mechanical Dimensions**

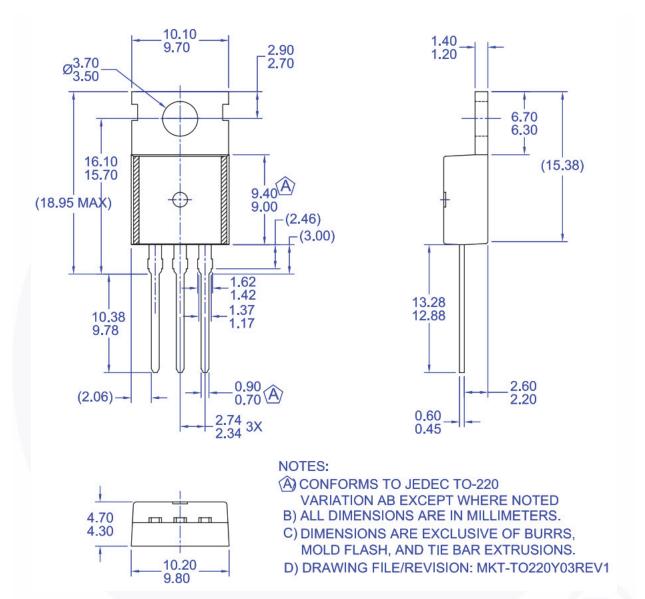


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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