

SEMICONDUCTOR®

November 2013

FQPF6N80T N-Channel QFET[®] MOSFET

800 V, 3.3 A, 1.95 Ω

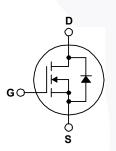
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 3.3 A, 800 V, $R_{DS(on)}$ = 1.95 Ω (Max.) @ V_{GS} = 10 V, I_D = 1.65 A
- Low Gate Charge (Typ. 31 nC)
- Low Crss (Typ. 14 pF)
- 100% Avalanche Tested
- 100% Package Isolation Tested





Absolute Maximum Ratings T_c = 25°C unless otherwise noted.

Symbol	Parameter		FQPF6N80T	Unit
V _{DSS}	Drain-Source Voltage		800	V
I _D	Drain Current - Continuous ($T_C = 25^{\circ}$ C	C)	3.3	A
	- Continuous (T _C = 100	°C)	2.1	A
I _{DM}	Drain Current - Pulsed	(Note 1)	13.2	А
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	680	mJ
I _{AR}	Avalanche Current	(Note 1)	3.3	А
E _{AR}	Repetitive Avalanche Energy	(Note 1)	5.1	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.0	V/ns
PD	Power Dissipation ($T_C = 25^{\circ}C$)		51	W
	- Derate above 25°C		0.41	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
Τ _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

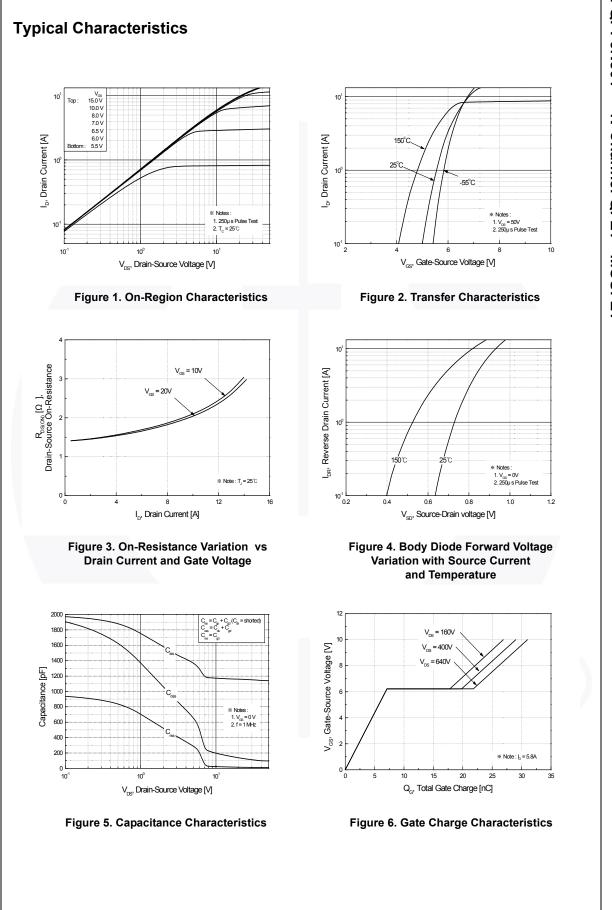
Thermal Characteristics

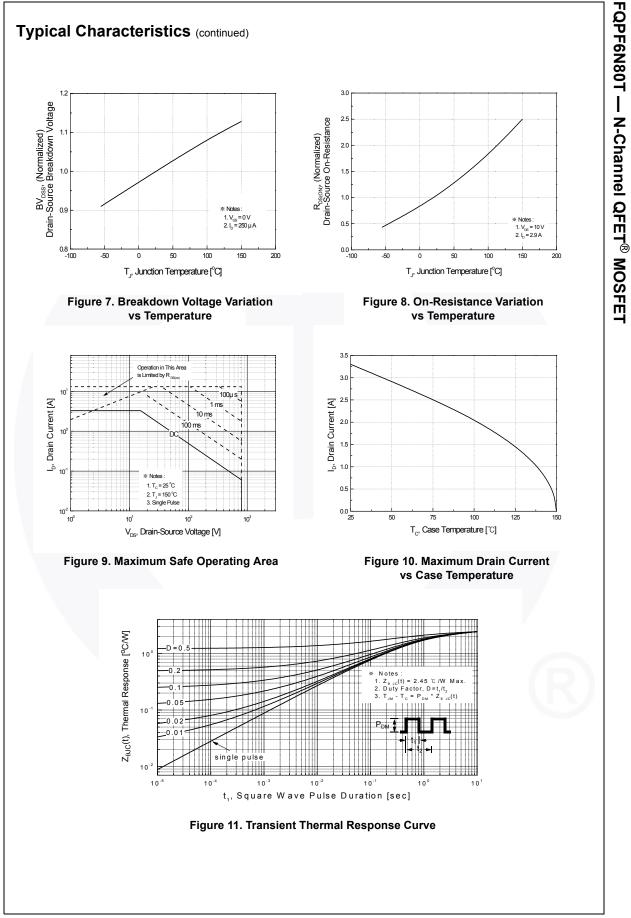
Symbol	Parameter	FQPF6N80T	Unit
$R_{ extsf{ heta}JC}$	Thermal Resistance, Junction-to-Case, Max.	2.45	°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

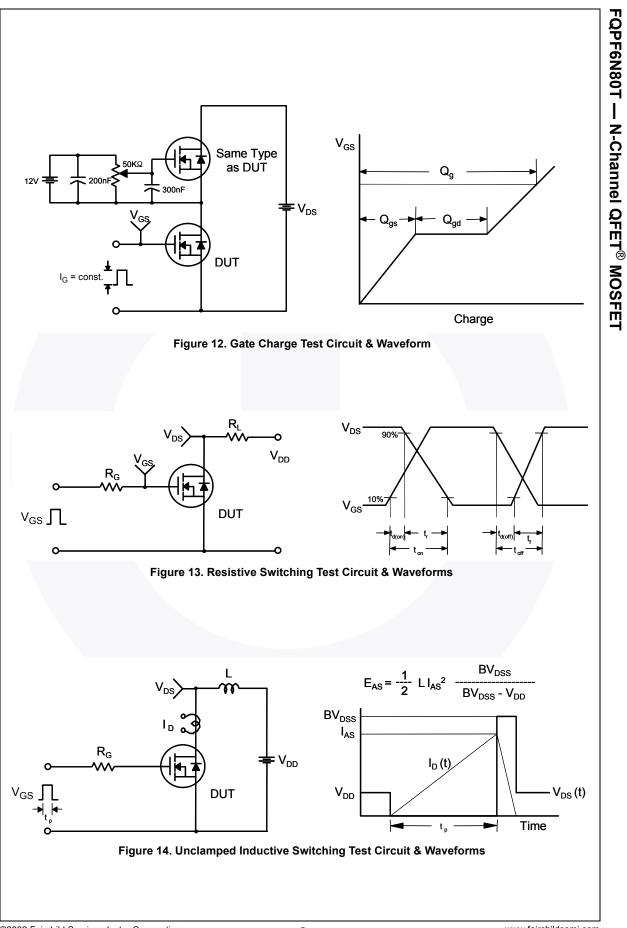
Part Nu	mber	Top Mark	Package	Packing Method	Reel Size	Ta	ape Widt	h Q	uantity
FQPF6	QPF6N80T FQPF6N80T TO-220F		Tube N/A		N/A		5	50 units	
lectri	cal C	haracteristics	T _C = 25°C	unless otherwise noted.					
Symbol		Parameter		Test Cond	itions	Min	Тур	Max	Unit
Off Cha	aracter	ristics							
3V _{DSS}	1	Source Breakdown V	oltage	$V_{GS} = 0 V, I_D = 250$) μΑ	800			V
BV _{DSS} ΔT _{.1}	Break Coeffi	down Voltage Temper cient	ature	I _D = 250 μA, Refere			0.9		V/°C
JSS				V _{DS} = 800 V, V _{GS} =	= 0 V			10	μA
	Zero (Gate Voltage Drain Cu	urrent	$V_{DS} = 640 \text{ V}, \text{ T}_{C} =$				100	μΑ
GSSF	Gate-E	Body Leakage Currer	t, Forward	V_{GS} = 30 V, V_{DS} =	0 V			100	nA
GSSR	Gate-I	Body Leakage Currer	t, Reverse	V_{GS} = -30 V, V_{DS} =	0 V			-100	nA
On Cha	racter	ristics							
GS(th)	Gate 1	Threshold Voltage		$V_{DS} = V_{GS}, I_D = 25$	0 μΑ	3.0		5.0	V
R _{DS(on)}		Drain-Source esistance		$V_{GS} = 10 \text{ V}, I_D = 1.65$	Ā		1.5	1.95	Ω
FS	Forwa	rd Transconductance		V _{DS} = 50 V, I _D = 1.	65 A		4.3		S
Jvnam	ic Cha	racteristics							
viss	1	Capacitance		N/ 05 X/ X/	<u></u>		1150	1500	pF
OSS		t Capacitance		V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz			125	1600	pF
rss		se Transfer Capacita	nce				14	18	pF
100									
Switch	ing Ch	aracteristics							
d(on)	Turn-C	On Delay Time		V _{DD} = 400 V, I _D = 5.8 A,			30	70	ns
	Turn-C	On Rise Time		$R_{G} = 25 \Omega$			70	150	ns
d(off)	Turn-C	Off Delay Time		0			65	140	ns
	Turn-C	Off Fall Time			(Note 4)		45	100	ns
λ ^d	Total C	Gate Charge		V _{DS} = 640 V, I _D = 5	.8 A.		31		nC
λ _{gs}	Gate-S	Source Charge		V _{GS} = 10 V	- ,		7.1		nC
2 _{gd}	Gate-I	Drain Charge		66	(Note 4)		15		nC
		Diode Characte	riation on	d Maximum Da	tingo				1
s					ungs			3.3	A
S SM	Maximum Continuous Drain-Source Diode Forward Cu Maximum Pulsed Drain-Source Diode Forward Curren					/	13.2	A	
SM SD		Source Diode Forwar		$V_{GS} = 0 \text{ V}, \text{ I}_{S} = 3.3$	Δ			1.4	V
′SD т		se Recovery Time	u voliaye	$V_{GS} = 0 V, I_S = 5.3$ $V_{GS} = 0 V, I_S = 5.8$			650		-
		se Recovery Time		$v_{GS} = 0 v, r_S = 5.8$ $dI_F / dt = 100 A/\mu s$	Λ,		5.7		ns
ک ^{رر}	Reven	se Recovery Charge					5.7		μC

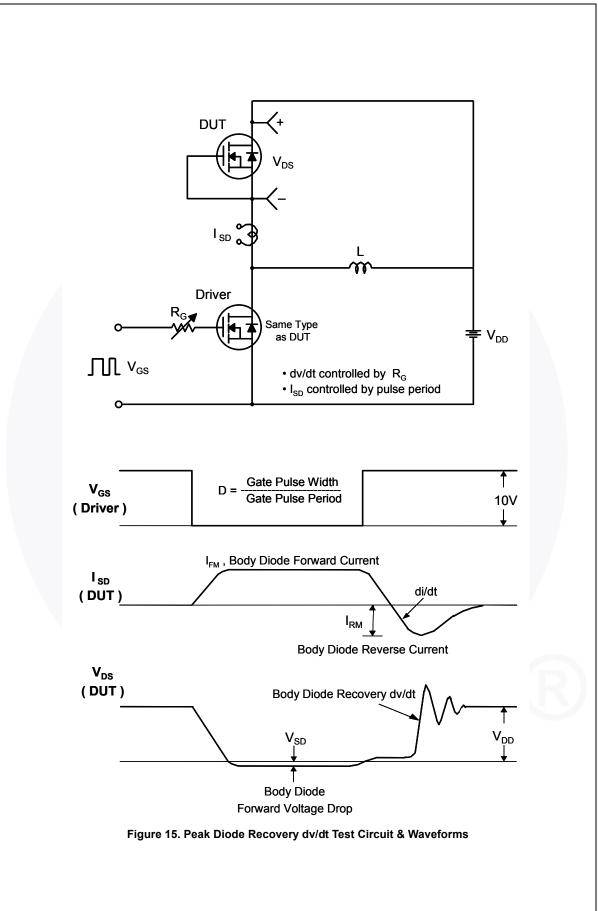
5. Viso=4000V, t=0.3s in single pulse, UL recognized.

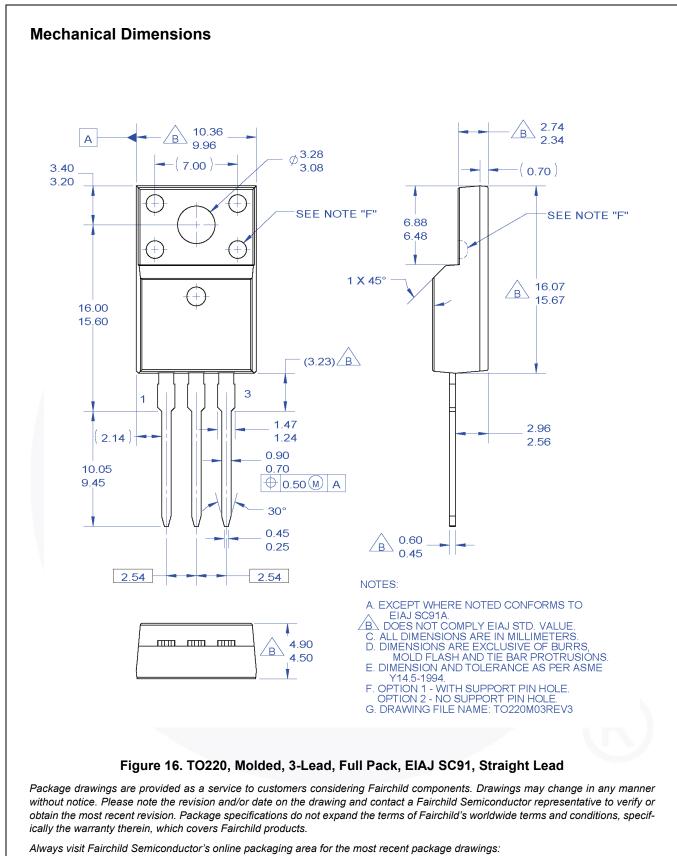
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