

FQT13N06L N-Channel QFET[®] MOSFET 60 V, 2.8 A, 110 mΩ

General Description

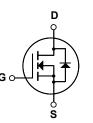
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor[®]'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications. March 2015

FQT13N06L — N-Channel QFET[®] MOSFET

Features

- 2.8 A, 60 V, $R_{DS(on)}$ = 110 m Ω (Max.) @V_{GS} = 10 V, I_D = 1.4 A
- Low Gate Charge (Typ. 4.8 nC)
- Low Crss (Typ. 17 pF)
- 100% Avalanche Tested





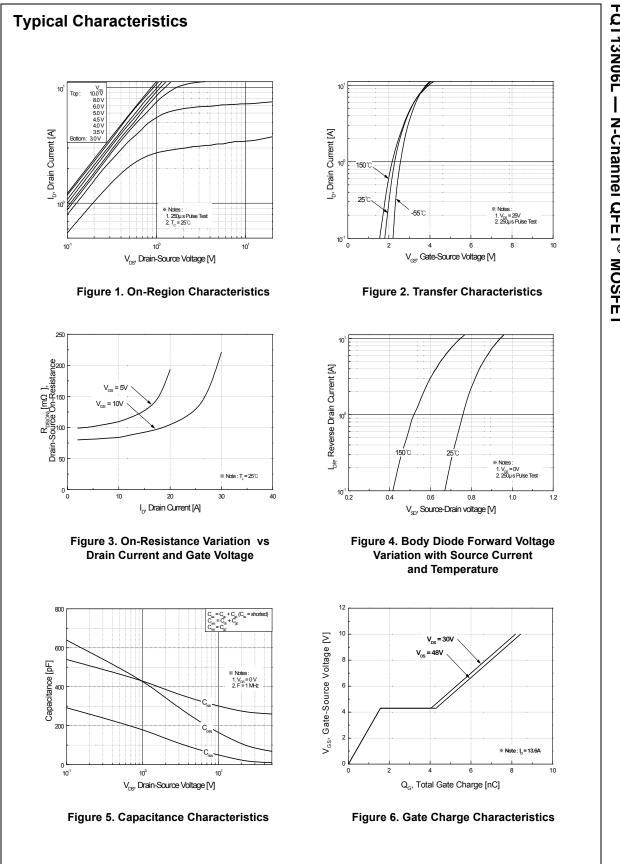
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

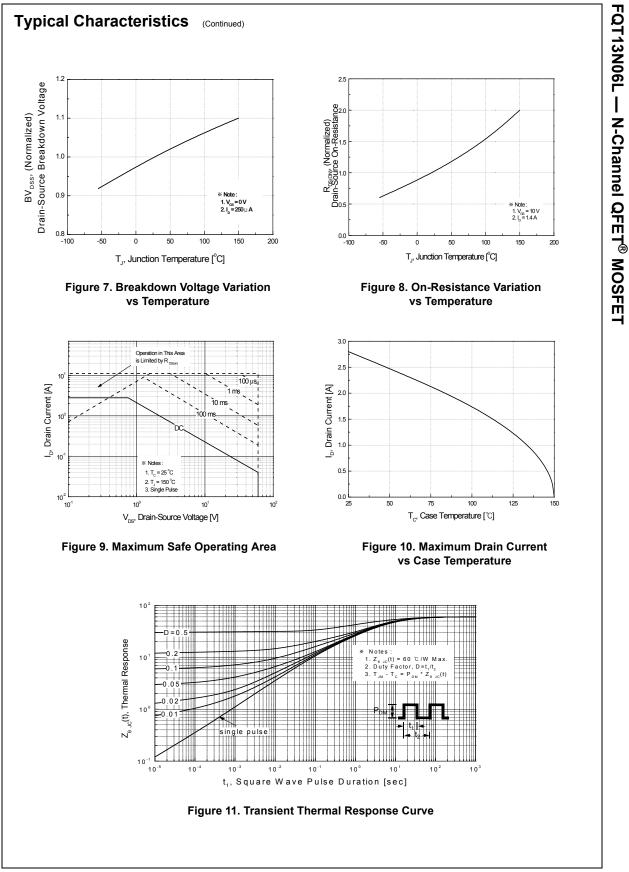
Symbol	Parameter		FQT13N06L	Unit
V _{DSS}	Drain-Source Voltage		60	V
D	Drain Current - Continuous (T _C = 25°C	C)	2.8	Α
	- Continuous (T _C = 70°C)		2.24	Α
DM	Drain Current - Pulsed	(Note 1)	11.2	Α
/ _{GSS}	Gate-Source Voltage		± 20	V
- AS	Single Pulsed Avalanche Energy	(Note 2)	85	mJ
AR	Avalanche Current	(Note 1) 2.8 (Note 1) 0.21		A mJ
AR	Repetitive Avalanche Energy			
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
° D	Power Dissipation (T _C = 25°C) - Derate above 25°C		2.1	W
			0.017	W/°C
Γ _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
Γ _L	Maximum Lead Temperature for Soldering 1/8" from Case for 5 Seconds	300	°C	

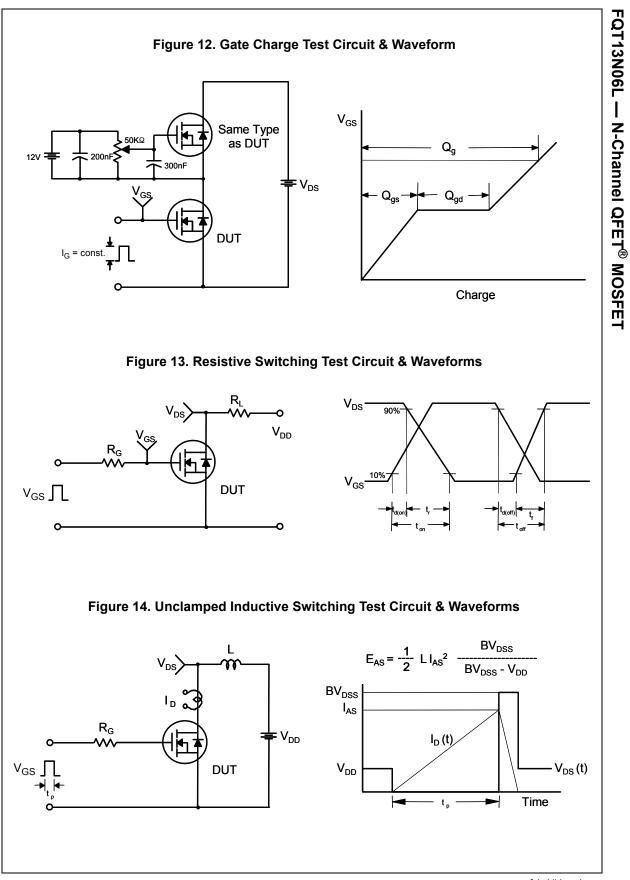
Thermal Characteristics

Symbol	Parameter	Тур	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *		60	°C/W
* When mounter	ed on the minimum pad size recommended(PCB mount).			

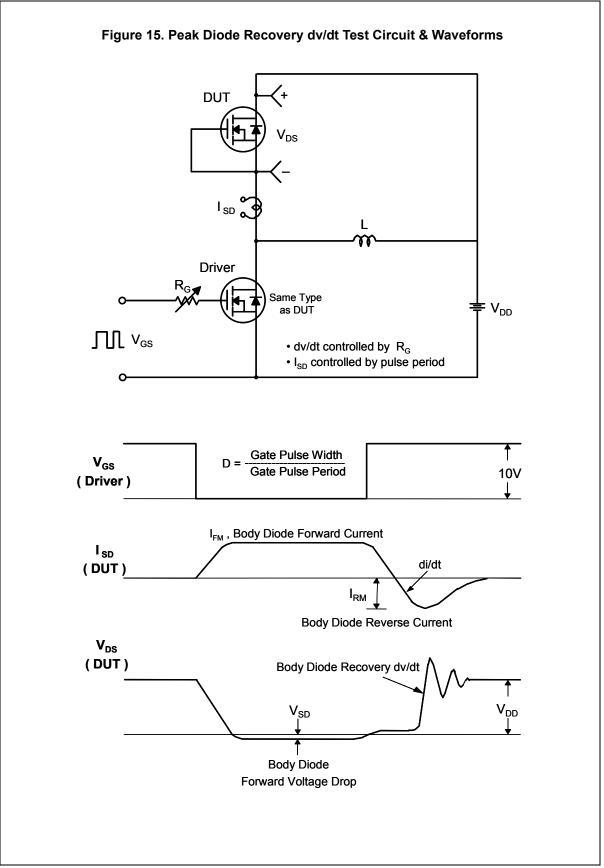
Symbol	Parameter	Test Conditions	5	Min	Тур	Max	Unit
Off Cha	racteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA		60			V
ΔBV _{DSS}	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced	to 25°C		0.05		V/°C
I _{DSS}		V _{DS} = 60 V, V _{GS} = 0 V				1	μA
	Zero Gate Voltage Drain Current	V_{DS} = 48 V, T_{C} = 125°C				10	μA
GSSF	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V				100	nA
GSSR	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
On Cha	racteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA		1.0		2.5	V
R _{DS(on)}	Static Drain-Source	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 1.4 \text{ A}$			0.088	0.11	v
DS(on)	On-Resistance	$V_{GS} = 5 V, I_D = 1.4 A$			0.110	0.14	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 25 V, I _D = 1.4 A	(Note 4)		4.1		S
			, ,				
-	ic Characteristics	1					
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,			270	350	pF
C _{oss}	Output Capacitance	f = 1.0 MHz			95	125	pF
C _{rss}	Reverse Transfer Capacitance				17	23	pF
Switchi	ng Characteristics						
d(on)	Turn-On Delay Time	V _{DD} = 30 V, I _D = 6.8 A,			8	25	ns
·r	Turn-On Rise Time	$R_{G} = 25 \Omega$		-	90	190	ns
d(off)	Turn-Off Delay Time			-	20	50	ns
^t f	Turn-Off Fall Time		(Note 4, 5)		40	90	ns
Qg	Total Gate Charge	V _{DS} = 48 V, I _D = 13.6 A,		-	4.8	6.4	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 5 V			1.6		nC
Q _{gd}	Gate-Drain Charge		(Note 4, 5)		2.7		nC
Drain S	ource Diode Characteristics a	nd Maximum Pating	c				
s	Maximum Continuous Drain-Source Dic	-	5			2.8	А
SM	Maximum Pulsed Drain-Source Diode F					11.2	A
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_S = 2.8 A$				1.5	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 V, I_S = 13.6 A,$			45		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	(Note 4)		45		nC
otes: Repetitive ra L = 12.6 mH $I_{SD} \le 13.6$ A Pulse test : p	ting : pulse-width limited by maximum junction tempera, I _{AS} = 2.8 A, V _{DD} = 25 V, R _G = 25 Ω , starting T _J = 25° A, di/dt \leq 300 A/µs, V _{DD} \leq BV _{DSS} , starting T _J = 25°C. Julse width \leq 300 µs, Duty cycle \leq 2%. Independent of operating temperature.	°C.					



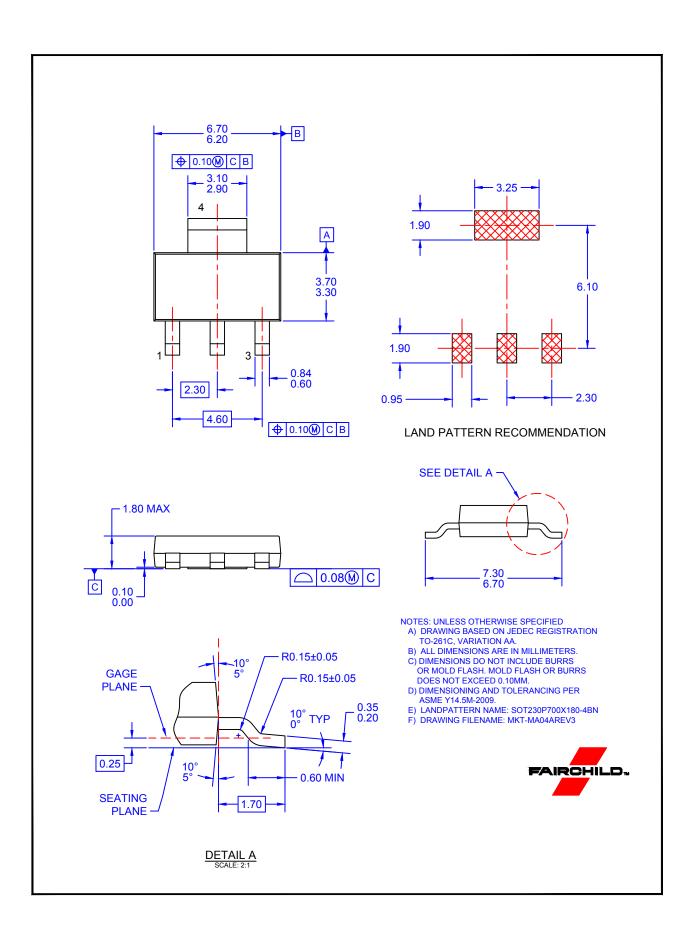




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