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# FSA832 — USB 2.0 High-Speed (480 Mbps) Charger Detection IC with Isolation Switch

## Features

USB Detection	USB Battery Charging Rev. 1.2 Supports Data Contact Detect (DCD) Dead Battery Provision (DBP) with 30-Minute Timer
Proprietary Charger and Other Detection	2.7 V / 2.0 V on DP/DM DP/DM Floating PS/2 Port Detection
Switch Type	Isolation Switch Closes for Charging Downstream Port (CDP) Standard Downstream Port (SDP)
V <sub>BUS</sub>	28 V Over-Voltage Tolerance -2 V Under-Voltage Tolerance
Package	10-Lead MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch
Ordering Information	FSA832L10X

## Description

The FSA832 is a charger detection IC with an integrated isolation switch for use with micro/mini USB port. The FSA832 detects USB battery chargers and is compliant with USB Battery Charging Specification, Rev 1.2 (BC1.2).

The FSA832 also detects proprietary chargers that pull the USB data lines HIGH (2.7 V / 2.0 V), floating data lines, and PS/2 ports. The device determines if a charger, either through a Dedicated Charging Port (DCP) or Charging Downstream Port (CDP), is connected or if a typical PC host, a Standard Downstream Port (SDP), is connected. The FSA832 conforms to all the constraints for the Dead Battery Provision (DBP) within the BC1.2 specification, including a 30-minute timer that cannot exceed 45 minutes per BC1.2.

## Applications

- MP3, Mobile Internet Device (MID), Cell Phone, PDA, Digital Camera, Notebook, and Netbook

## Typical Application

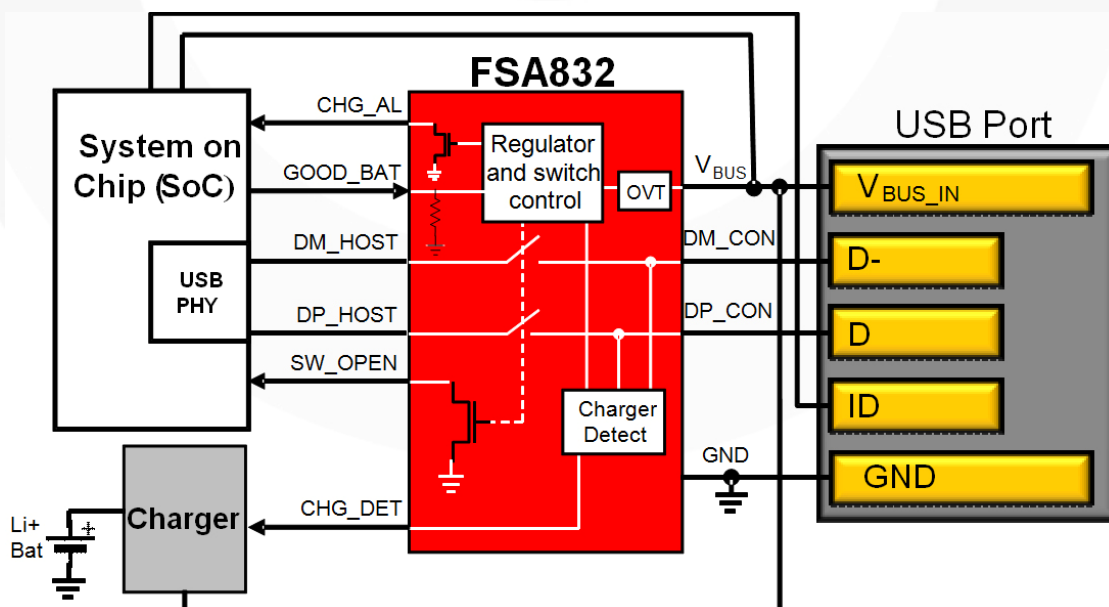


Figure 1. Mobile Phone Example

## Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package Description	Packing Method
FSA832L10X	-40 to 85°C	ZY	10-Lead, MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch	Tape & Reel

## Pin Configurations

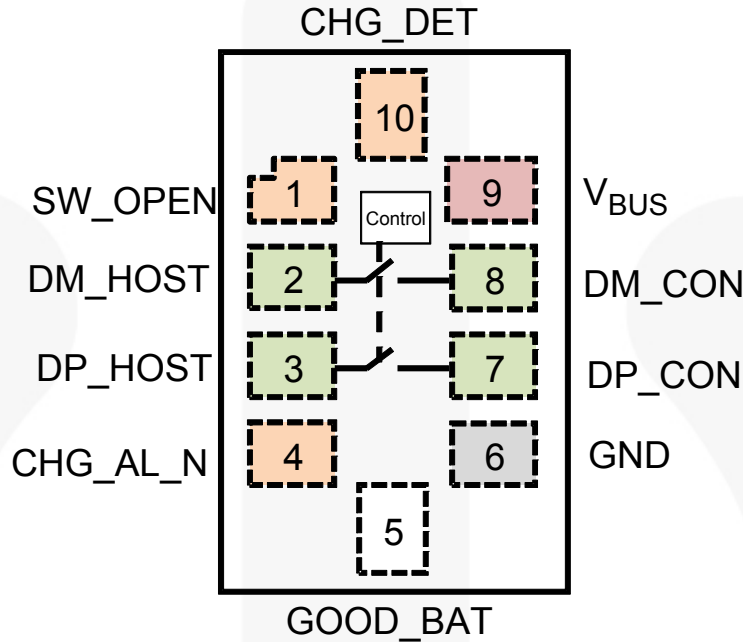


Figure 2. Pin Assignments (Top View)

## Pin Descriptions

Name	Pin #	Description
<b>USB Interface</b>		
DP_HOST	3	D+ signal connected to the resident USB transceiver on the phone.
DM_HOST	2	D- signal connected to the resident USB transceiver on the phone.
<b>Connector Interface</b>		
V <sub>BUS</sub>	9	Input voltage supply pin to be connected to the V <sub>BUS</sub> pin of the USB connector.
GND	6	Ground
DP_CON	7	Connected to the USB connector D+ pin
DM_CON	8	Connected to the USB connector D- pin
<b>Status Outputs</b>		
CHG_DET	10	CMOS push/pull output connected to charger IC to indicate if a charger has been detected (LOW=charger not detected; HIGH=proprietary charger, DCP, or CDP charger detected).
SW_OPEN	1	Open-drain output pin; requires pull-up resistor to I/O voltage supply (LOW=switch closed; Hi-Z=switch open).
CHG_AL_N	4	CMOS open-drain output pin (LOW=V <sub>BUS</sub> is valid and charge is allowed to be drawn from V <sub>BUS</sub> ; Hi-Z=V <sub>BUS</sub> is not at a valid voltage).
<b>Input Pin</b>		
GOOD_BAT	5	Input that indicates if the battery is a good battery or a dead battery (V <sub>IL</sub> =dead battery; V <sub>IH</sub> =good battery).

### Note:

- Output voltage conditions are LOW = V<sub>OL</sub> and HIGH = V<sub>OH</sub>.

**Table 1. Functionality**

Device Detected	GOOD_BAT	SW_OP_EN	CHG_AL_N	CHG_DET	DP_HOST	DM_HOST	DP_CON	DM_CON
DCP	X	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V <sub>DP_SRC</sub> <sup>(2)</sup>	Hi-Z <sup>(2)</sup>
Proprietary Charger	X	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	Hi-Z	Hi-Z
CDP	HIGH	LOW	LOW	HIGH	DP_CON	DM_CON	DP_HOST	DM_HOST
CDP	LOW	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V <sub>DP_SRC</sub>	Hi-Z
PS/2 Ports <sup>(3)</sup>	X	Hi-Z	LOW	LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SDP	HIGH	LOW	LOW	LOW	DP_CON	DM_CON	DP_HOST	DM_HOST
SDP	LOW	Hi-Z	LOW	LOW	Hi-Z	Hi-Z	V <sub>DP_SRC</sub>	Hi-Z
SDP, CDP, or DCP plugged in and after 30-minute timer expires	LOW	Hi-Z	Hi-Z	LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z
V <sub>BUS</sub> < V <sub>BUS</sub> valid to V <sub>BUS</sub> > V <sub>BUS</sub> valid operation prior to completing detection of SDP, CDP, or DCP. Upon detection, all outputs switch as in rows above.	X	Hi-Z	Hi-Z	Hi-Z to LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z

**Note:**

- Hi-Z is the internal state of DM\_CON. Since a DCP has been detected, DM\_CON is shorted to DP\_CON externally and DM\_CON is shorted to V<sub>DP\_SRC</sub>. V<sub>DP\_SRC</sub> is not put on DP\_CON for proprietary chargers.
- DP\_CON and DM\_CON are pulled to V<sub>BUS</sub> through a resistor by the PS/2 port when it is connected to the FSA832.

## Functional Description

### Data Contact Detect (DCD)

DCD relies on the D+ and D- lines being present. DCD waits until the internal timeout t<sub>DCD\_TOUT</sub> has expired in the following cases:

- If a charger does not have a D+ pin on the USB connector;
- If the D+ pin is not shorted to D- pin on the connector,
- If D+ is pulled up to a supply; or
- If D+ does not have a sufficient path to ground to defeat a pull-up IDP\_SRC (I<sub>DP\_SRC</sub>) current source.

The FSA832 proceeds with charger detection even though it is unlikely that a charger is present. If there is no charge, the algorithm reports an SDP and closes the switch. If a device is pulling D+ HIGH, this voltage presents itself to the USB transceiver or Physical Layer Interface (PHY) block within a System on Chip (SoC) after the switch is closed.

If the DCD timeout is insufficient and the PHY block is so equipped, DCD and the charging algorithm can be repeated in the PHY block. The stipulation is that the total time from V<sub>BUS</sub> valid to USB transceiver connection with a 1.5 kΩ pull-up to 3.3 V must be one (1) second, per USB 2.0 standards, provided the portable device does not have a dead battery.

### CHG\_AL\_N Output and Output Timing

CHG\_AL\_N output indicates that charge is allowed to be drawn from V<sub>BUS</sub> when CHG\_AL\_N is LOW. When the FSA832 first powers up and prior to detection, the CHG\_AL\_N pin can follow V<sub>BUS</sub> up to 28 V, which is the

absolute maximum V<sub>BUS</sub> voltage allowed. Whenever V<sub>BUS</sub> is at GND, the FSA832 is completely off and the switches and all I/Os are in the Hi-Z state. When V<sub>BUS</sub> climbs above the valid V<sub>BUS</sub> threshold, detection occurs automatically and CHG\_DET, SW\_OPEN, and CHG\_AL\_N all simultaneously switch to the states indicated in Table 1 if GOOD\_BAT is HIGH (see *Dead Battery Provision description for GOOD\_BAT = LOW*).

### Dead Battery Provision

BC1.2 and USB 2.0 allow a portable device (defined as a device with a battery) with a dead battery to take a maximum of 100 mA from the USB V<sub>BUS</sub> line for a maximum of 45 minutes as long as the portable device forces the D+ line to V<sub>DP\_SRC</sub>. The FSA832 starts detection when V<sub>BUS</sub> crosses the V<sub>BUSVLD</sub> threshold and, if it detects a CDP or SDP and GOOD\_BAT is HIGH, automatically closes the switch and does not force the DP\_CON pin to V<sub>DP\_SRC</sub>.

Once charger detection is complete, the FSA832 starts a 30-minute timer and forces the DP\_CON pin to V<sub>DP\_SRC</sub> until the timer elapses. During the 30-minute period; if GOOD\_BAT is LOW, V<sub>DP\_SRC</sub> is applied to DP\_CON and the D+/D- switches are opened. If GOOD\_BAT is HIGH, V<sub>DP\_SRC</sub> is not applied to DP\_CON and the D+/D- switches are closed. If GOOD\_BAT is LOW when the 30-minute timer expires; regardless of whether a proprietary charger, SDP, CDP, or DCP was previously detected; the FSA832 removes V<sub>DP\_SRC</sub> from DP\_CON and forces CHG\_DET LOW and CHG\_AL\_N to Hi-Z (SW\_OPEN remains in Hi-Z). To exit this fault condition, remove V<sub>BUS</sub>, wait for all the V<sub>BUS</sub> Printed Circuit Board

(PCB) capacitance to discharge, and re-apply  $V_{BUS}$ . Table 1 provides the functionality of the pins when the timer expires.

When GOOD\_BAT is HIGH and the battery is removed from the portable device while  $V_{BUS}$  is valid, bringing GOOD\_BAT LOW; the FSA832 opens the isolation switches on DP\_CON and DM\_CON and forces the DP\_CON pin to  $V_{DP\_SRC}$ . In this scenario, the timer generally expires because the SoC does not have a supply to bring GOOD\_BAT HIGH unless the battery that was removed is re-inserted within 30 minutes after the USB plug is inserted.

If an SDP or CDP is inserted with GOOD\_BAT HIGH during the 30-minute timer; then GOOD\_BAT changes to LOW, SW\_OPEN changes to Hi-Z, and the counter continues counting until the 30 minutes expires. If GOOD\_BAT then returns to HIGH, SW\_OPEN changes to LOW and finishes out the 30-minute time.

GOOD\_BAT has an internal pull-down resistor to ensure it is LOW when the SoC is powered down. This input is designed to have very  $V_{IH}$  interface with low-voltage SoCs driven with 1.2 V supplies. GOOD\_BAT can be connected to the processor supply voltage because the processor should wake up whenever  $V_{BUS}$  is turned on.

### Proprietary Chargers

Chargers pulling the USB data line DM\_CON HIGH to 2.0 V or 2.7 V and data line DP\_CON HIGH to 2.0 V or 2.7 V are detected by the FSA832 and reported proprietary chargers with a higher charge current allowed. Other chargers that float the DP/DM lines are also detected as a proprietary by means of float detection. This allows a proprietary charger with floating DP/DM to benefit from higher charge current.

### PS/2 Port

Mice and keyboards utilizing the PS/2 port interface pull the clock and data pins of the PS/2 connector HIGH to  $V_{BUS}$  through a resistive pull-up. When the PS/2 device is adapted to a USB interface, the clock and data pins are translated to the DP\_CON and DM\_CON lines of the USB connector, respectively.

The benefit of detecting the PS/2 port as a separate device is the ability to limit the current that can be drawn from the bus, thus protecting the PS/2 port. Once the PS/2 port is detected, the DP\_HOST and DM\_HOST switches remain open to protect the USB PHY connected to DP\_HOST and DM\_HOST from voltages as high as  $V_{BUS}$ .

### Ground Drops

When a DCP is detected,  $V_{DP\_SRC}$  is forced on DP\_CON provided GOOD\_BAT is HIGH or GOOD\_BAT is LOW and the DBP timer has not expired. When  $\sim 1.5$  A is flowing into  $V_{BUS}$  and GND lines of the USB cable, the current can create substantial ground drops that lift the ground of the portable device. This drop adds to the voltage at the DP\_CON pin as seen from the DCP D+ pin. For the maximum ground drop of 375 mV specified in the BC1.2 specification and for the maximum  $V_{DP\_SRC}$  of 0.7 V; the voltage as seen by the DCP would be 1.075 V. Smart DCPs that rely on this voltage detection to determine attach and detach detection need to take this into account.

### $V_{BUS}$ Tolerance

When  $V_{BUS}$  rises, an internal Power-On Reset (POR) detects this voltage and prepares the FSA832 for charger detection.

$V_{BUS}$  voltages up to 28 V can be tolerated by the  $V_{BUS}$  pin.  $V_{BUS}$  can tolerate voltages up to -2 V for cases where a charger is plugged in backwards.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>BUS</sub>	Voltage from USB Connector		-2	28	V
V <sub>SW</sub>	USB Switch I/O Voltage (DP_CON, DM_CON, DP_HOST, DM_HOST)		-0.5	6.0	V
I <sub>SW</sub>	USB Switch Current (DP_CON to DP_HOST, DM_CON to DM_HOST)		-30	+30	mA
V <sub>I/O</sub>	Voltage from GOOD_BAT, CHG_AL_N, CHG_DET and SW_OPEN I/Os		-0.5	6.0	V
V <sub>CA</sub>	Voltage from CHG_AL_N Output		-0.5	28.0	V
I <sub>I/O</sub>	CHG_AL_N, CHG_DET and SW_OPEN Outputs Sink/Source Current		-5	+5	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
T <sub>J</sub>	Maximum Junction Temperature			+150	°C
T <sub>L</sub>	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	IEC 61000-4-2 System	USB Pins (DP_CON, DM_CON, V <sub>BUS</sub> )	Air Gap	15	kV
			Contact	8	
	Human Body Model, JEDEC JESD22-A114		All Pins	6	
	Charged Device Model, JEDEC JESD22-C101		All Pins	1	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>BUS</sub>	V <sub>BUS</sub> Input HIGH Voltage	4	6	V
V <sub>SW</sub>	Switch I/O Voltage for USB Path	0	3.6	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C

## DC Electrical Characteristics

Unless otherwise indicated,  $V_{BUS}=4$  V to 6 V and  $T_A=-40$  to  $+85^{\circ}\text{C}$ . Typical values are at  $T_A=25^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Status Outputs</b>						
$V_{OHCD}$	Output HIGH Voltage (CHG_DET)	$I_{OH}=-2$ mA	2.0			V
$V_{OL}$	Output LOW Voltage (CHG_DET, CHG_AL_N, SW_OPEN)	$I_{OL}=2$ mA			0.4	V
$t_{DIFF}$	Skew Between Any Output (CHG_DET, CHG_AL_N, SW_OPEN) Switching Relative to Other Outputs Switching	$I_{I/O}=\pm 2$ mA, CHG_AL_N=20 k $\Omega$ to 5 V, SW_OPEN=10 k $\Omega$ to 1.8 V			100	ns
<b><math>V_{BUS}</math> Pin</b>						
$V_{BUSVLD}$	$V_{BUS}$ Valid Detection Threshold <sup>(4)</sup>		0.8		4.0	V
$I_{BUSIN}$	$V_{BUS}$ Input Leakage	$V_{BUS}=0$ V to 0.8 V			3	$\mu\text{A}$
$I_{VBUSACT}$	$V_{BUS}$ Active Mode Average Current	USB Path Active, USB Switch Closed After Charger Detection			250	$\mu\text{A}$
$t_{OUT}$	Time from $V_{BUS}$ Valid Asserted to CHG_DET, CHG_AL_N and SW_OPEN Outputs Valid for BC1.2 Standard Accessory Detection (SDP, DCP, or CDP)	DP_CON Pulled Down to GND with 15 k $\Omega$ ; All Voltages Forced on $V_{BUS}$ , DP_CON, DM_CON, and GND simultaneously			250	ms
<b>Switch Characteristics</b>						
$I_{OFF}$	Power Off Leakage Current	USB Path $V_{BUS}=0$ V, $V_{SW}=0$ V or 3.6 V, Figure 4			10	$\mu\text{A}$
$R_{ONUSB}$	High-Speed USB Range Switch On Resistance <sup>(4)</sup>	$V_{DP\_CON} / V_{DM\_CON}=0$ V, 0.4 V; $I_{ON}=8$ mA; Figure 3; $V_{BUS}=4$ V to 6 V		4.5	6.0	$\Omega$
<b>Control Input</b>						
$V_{IH}$	Input HIGH Voltage (GOOD_BAT)		1.1			V
$V_{IL}$	Input LOW Voltage (GOOD_BAT)				0.5	V
$R_{PD}$	Pull-Down Resistance (GOOD_BAT)		1			M $\Omega$
$I_{IN}$	Input Leakage Current (GOOD_BAT)	$V_{BUS}=5$ V, GOOD_BAT=0 V to 4.4 V			10	$\mu\text{A}$
$I_{IOFF}$	Off-State Leakage Current (GOOD_BAT)	$V_{BUS}=0$ V, GOOD_BAT=0 V to 4.4 V			10	$\mu\text{A}$
$t_{DBP}$	Dead Battery Provision (DBP) Timer		15	30	45	min
$t_{GB}$	Time from GOOD_BAT Asserted to SW_OPEN De-Asserted, Switches Closed and Meet the $R_{ONUSB}$ Specification				30	ms
$t_{DB}$	Time from GOOD_BAT De-asserted to SW_OPEN Asserted, Switches Opened				65	ms
<b>Battery Charger Detection Parameters from BC1.2 Specification</b>						
$V_{DAT\_REF}$	Data Detect Voltage		0.25		0.40	V
$V_{DM\_SRC}$	D- Source Voltage <sup>(5)</sup>		0.5		0.7	V
$V_{DP\_SRC}$	D+ Source Voltage <sup>(5)</sup>		0.5		0.7	V
$V_{LGC}$	Logic Threshold		0.8		2.0	V
$I_{DM\_SINK}$	D- Sink Current		25		175	$\mu\text{A}$
$I_{DP\_SINK}$	D+ Sink Current		25		175	$\mu\text{A}$
$I_{DP\_SRC}$	Data Contact Detect Current Source		7		13	$\mu\text{A}$

Continued on the following page...

## DC Electrical Characteristics

Unless otherwise indicated,  $V_{BUS}=4\text{ V to }6\text{ V}$  and  $T_A=-40\text{ to }+85^\circ\text{C}$ . Typical values are at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{DCD\_DBNC}$	Data Contact Detect Debounce		10			ms
$t_{DCD\_TOUT}$	Time for DCD to Timeout		300	450	900	ms
$t_{VDPSRC\_ON}$	D+ Voltage Source On Time		40			ms
$t_{VDMSRC\_ON}$	D- Voltage Source On Time		40			ms

### Notes:

- Guaranteed by characterization; not production tested.
- The voltage source,  $V_{DP\_SRC} / V_{DM\_SRC}$ , is able to source at least  $250\ \mu\text{A}$  when the output voltage is in the specified range. This voltage source should not pull  $DP\_CON / DM\_CON$  below  $2.2\text{ V}$  when  $DP\_CON / DM\_CON$  is pulled to a voltage of  $3.0\text{ V}$  minimum or  $3.6\text{ V}$  maximum with a resistance of  $900\ \Omega$  minimum or  $1575\ \Omega$  maximum.

## AC Electrical Characteristics

Unless otherwise specified, values are at  $T_A=-40\text{ to }+85^\circ\text{C}$ ; all typical values are for  $V_{CC}=3.3\text{ V}$  at  $T_A=25^\circ\text{C}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Figure
Xtalk	Active Channel Crosstalk, $DP\_COM$ to $DM\_CON^{(6)}$	$F=1\text{ MHz}$ , $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-78		dB	Figure 6
		$F=240\text{ MHz}$ , $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-36			
$O_{IRR}$	Off Isolation Rejection Ratio, $DM\_HOST$ to $DM\_CON$ , $DP\_HOST$ to $DP\_CON^{(6)}$	$f=1\text{ MHz}$ , $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-84		dB	Figure 5
		$f=240\text{ MHz}$ , $R_T=50\ \Omega$ , $C_L=0\text{ pF}$		-34			
BW	Bandwidth of Switch <sup>(6)</sup>	$R_T=50\ \Omega$		1.5		GHz	Figure 5

### Note:

- Guaranteed by characterization; not production tested.

## Capacitance

Unless otherwise specified, values are at  $T_A=-40\text{ to }+85^\circ\text{C}$ .

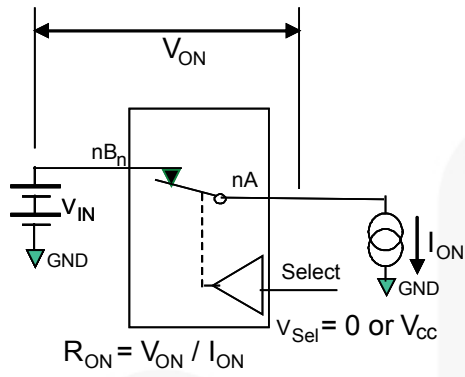
Symbol	Parameter	Condition	Typical	Unit	Figure
$C_{OFF}$	$DP\_CON$ , $DM\_CON$ Off Capacitance <sup>(7)</sup>	$V_{BIAS}=0.2\text{ V}$ , $f=1\text{ MHz}$	3.2	pF	Figure 7
$C_{ON}$	$DP\_CON$ , $DM\_CON$ On Capacitance <sup>(7)</sup>	$V_{BIAS}=0.2\text{ V}$ , $f=1\text{ MHz}$	5.8	pF	Figure 8

### Note:

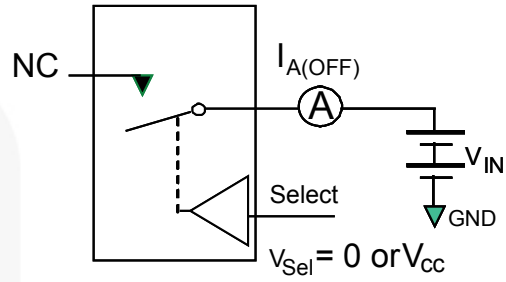
- Guaranteed by characterization; not production tested.



**Test Diagrams**

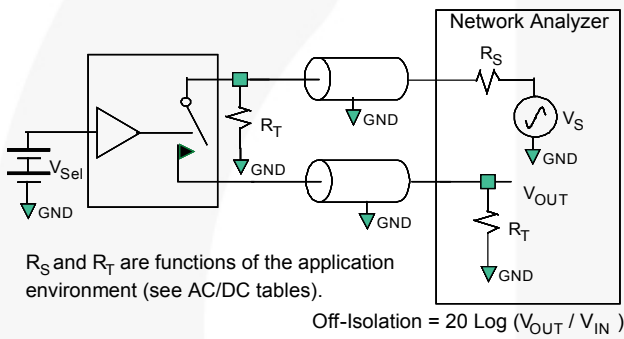


**Figure 3. On Resistance**

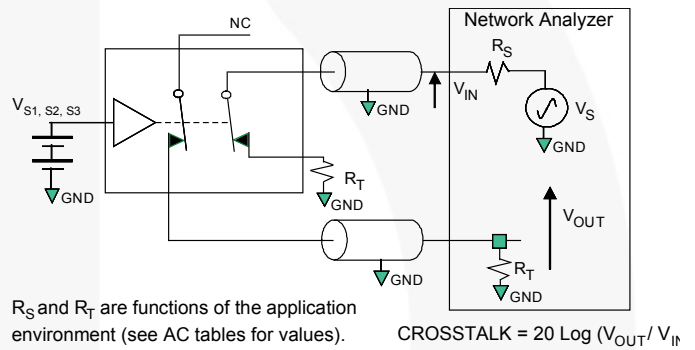


\*\*Each switch port is tested separately.

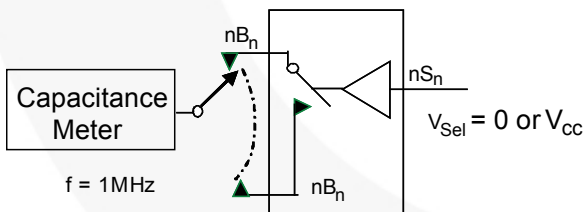
**Figure 4. Off Leakage**



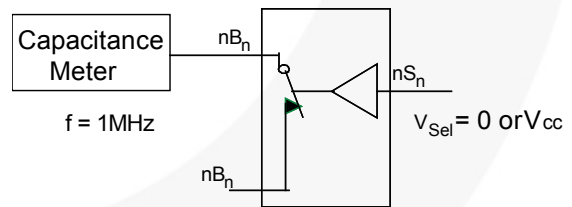
**Figure 5. Channel Off Isolation**



**Figure 6. Active Channel Crosstalk**



**Figure 7. Channel Off Capacitance**



**Figure 8. Channel On Capacitance**





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| Fairchild Semiconductor® | MotionGrid®                                    | SuperSOT™-6                           | VoltagePlus™     |
| FACT Quiet Series™       | MTi®   | SuperSOT™-8                           | XST™             |
| FACT®                    | MTx®   | SupreMOS®                             | Xsens™           |
| FastvCore™               | MVN®   | SyncFET™                              | 仙童®              |
| FETBench™                | mWSaver®                                       | Sync-Lock™                            |                  |
| FPS™                     | OptoHiT™                                       |                                       |                  |
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