April 2015

FUSB300C
Programmable USB Type-C Controller

Features

- Type-C Detection of Attach and Orientation
- Flexible Multi-Platform Support through I^2C Programmability
- Supports:
  - Dual Role Port (DRP)
  - Downstream Facing Port (DFP)
  - Upstream Facing Port (UFP)
  - Accessory Modes
  - Alternate Interfaces

Applications

- Smartphones
- Tablets
- Laptops
- Wearables

Description

The FUSB300C is a flexible, thin client solution for USB Type-C control. This product is a generic hardware solution that targets system designers looking to implement a DRP/DFP/UFP USB Type-C connector while providing the software flexibility for multiple platform support.

The FUSB300C performs USB Type-C detection including attach and orientation. TheFUSB300C automates VBUS threshold detection as well as the various charging current levels. The FUSB300C also includes an integrated VCONN power switch.

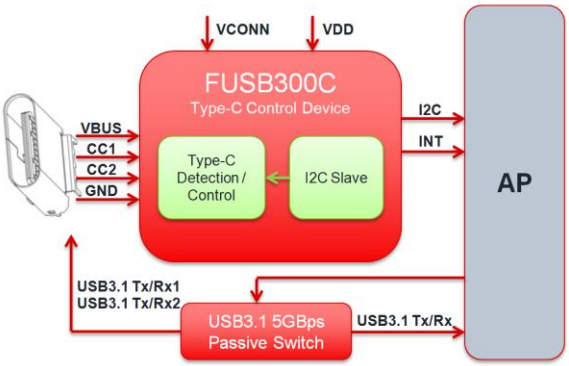


Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FUSB300CUCX	-40 to 85°C	9-Ball Wafer-Level Chip Scale Package (WLCSP), 1.215 x 1.215 x 0.6 mm, 0.4 mm Pitch	Tape and Reel

Typical Application

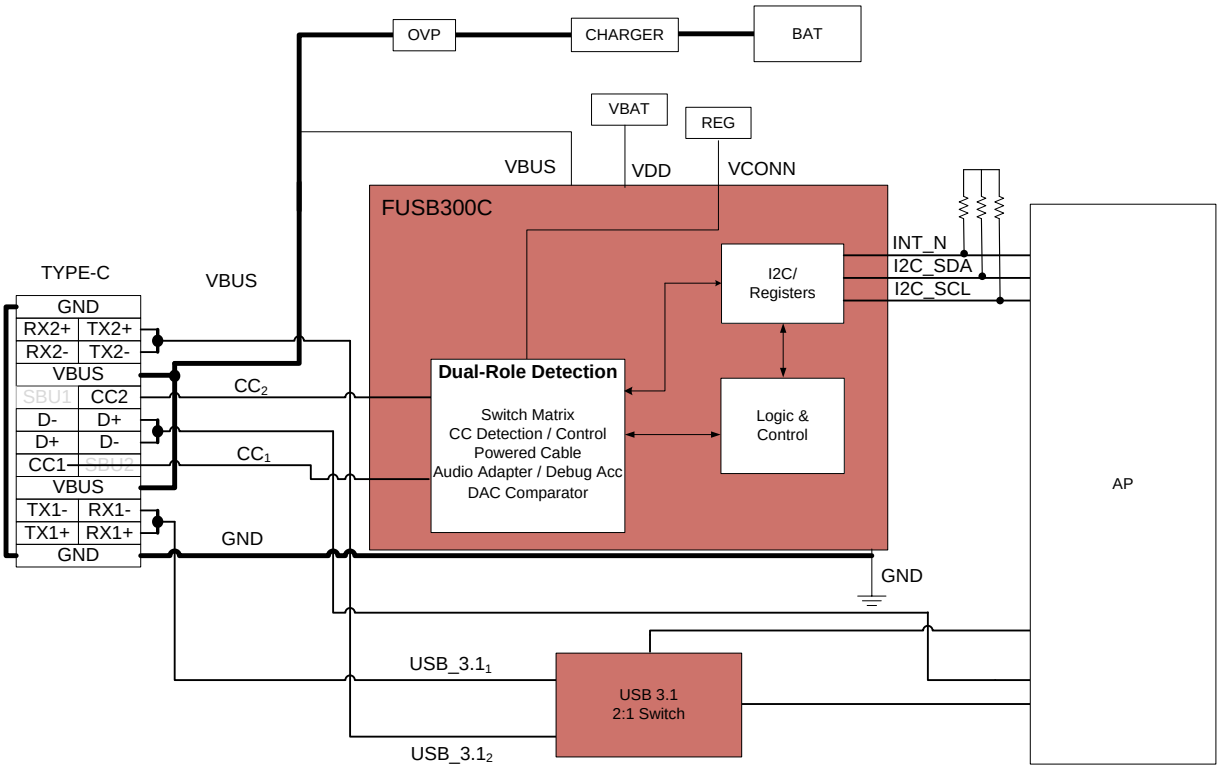


Figure 2. Typical Application

Block Diagram

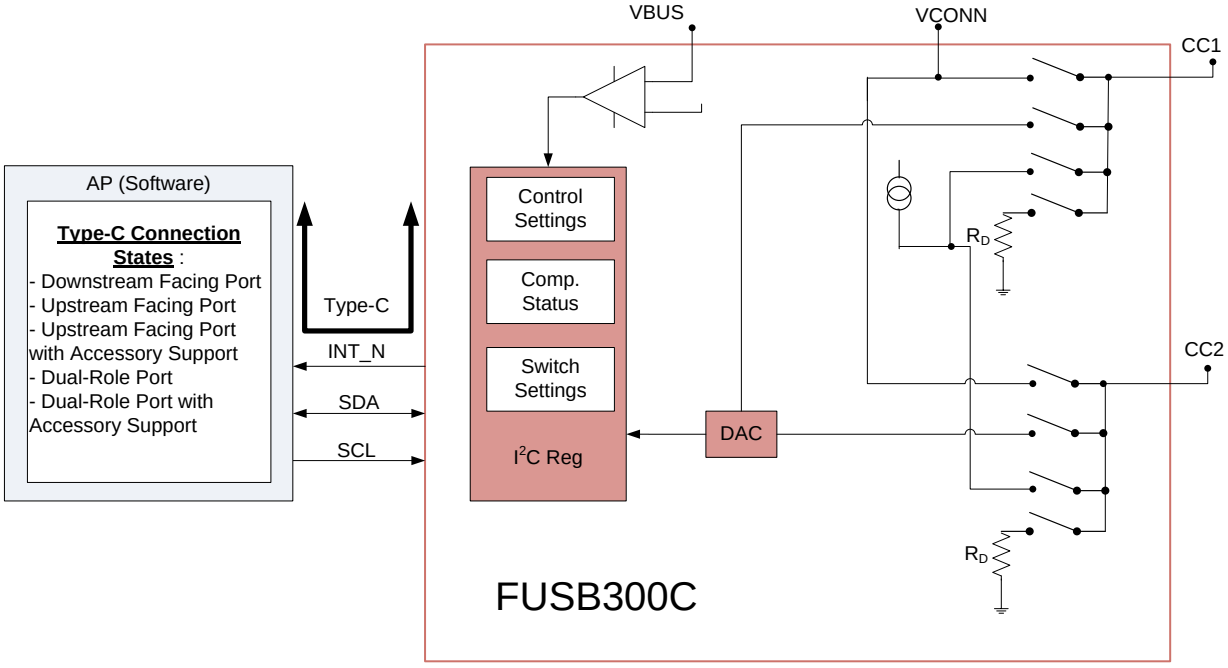


Figure 3. Functional Block Diagram

Pin Configuration

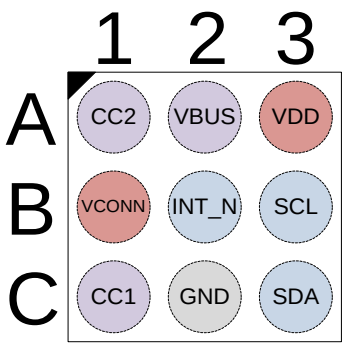


Figure 4. Pin Assignment (Top Through View)

Pin Map

	Column 1	Column 2	Column 3
Row A	CC2	VBUS	VDD
Row B	VCONN	INT_N	SCL
Row C	CC1	GND	SDA

Pin Descriptions

Name	Type	Description
USB Type-C Connector Interface		
CC1/CC2	I/O	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: • Sets the allowable charging current for VBUS to be sensed by the attached device • Used to detect when a detach has occurred Operating as a device: • Indicates what the allowable sink current is from the attached host.
GND	Ground	Ground
VBUS	Input	VBUS input pin for attach and detach detection when operating as an upstream facing port (Device).
Power Interface		
VDD	Power	Input supply voltage.
VCONN	Power Switch	Regulated input to be switched to correct CC pin as VCONN to power USB3.1 full-featured cables and other accessories
Signal Interface		
SCL	Input	I^2C serial clock signal to be connected to the phone-based I^2C master.
SDA	Open-Drain I/O	I^2C serial data signal to be connected to the phone-based I^2C master
INT_N	Open-Drain Output	Active LOW open drain interrupt output used to prompt the phone baseband processor to read the I^2C register bits.

Configuration Channel Switch

The FUSB300C integrates the control and detection functionality required to implement a USB Type-C host, device or dual-role port including:

- Device Port Pull-Down(R_D)
- Host Port Pull-Up (I_P)
- VCONN Power Switch for Full-Featured USB3.1 Cables
- Configuration Channel (CC) Threshold Comparators.

Each CC pin contains a flexible switch matrix that allows the host software to control what type of Type-C port is implemented. The switches are shown in Figure 5.

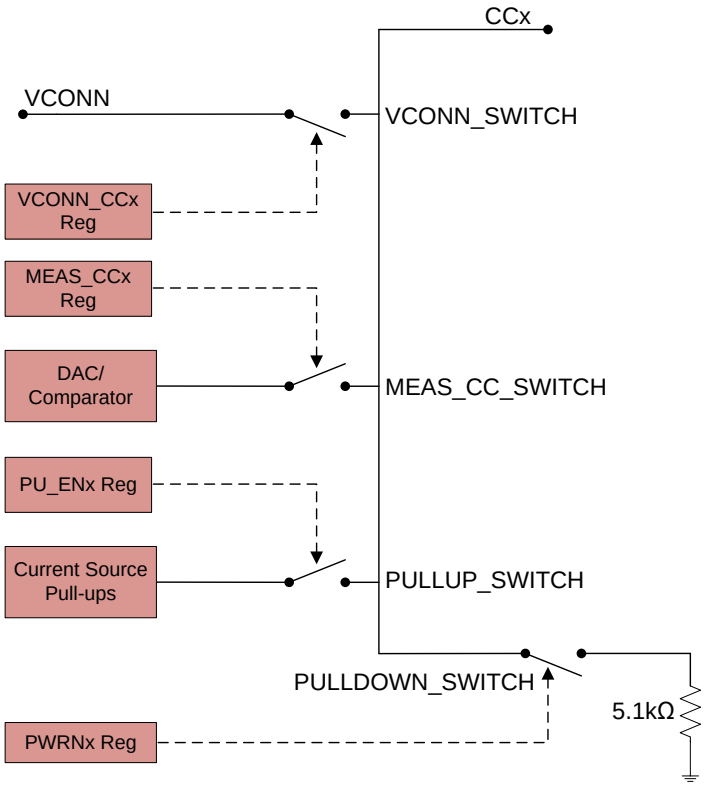


Figure 5. Configuration Channel Switch Functionality

Type-C Detection

The FUSB300C implements multiple comparators and a programmable DAC that can be used by software to determine the state of the CC and VBUS pins. This status information provides the software all the information required to determine attach, detach and charging current capabilities based on the specific Type-C port to which the FUSB300C has been configured.

The FUSB300C has three fixed threshold comparators that match the USB Type-C specification for the three charging current levels that can be detected by a Type-C device. These comparators automatically cause a BC_LVL interrupt to occur when there is a change of state. In addition to the fixed threshold comparators, the host software can use the 6-bit DAC to determine the state of the CC lines more accurately.

The FUSB300C also has a fixed comparator that monitors if VBUS has reached a valid threshold or not. The DAC can be used to measure VBUS up to 15 V which allows the software to confirm that changes to the VBUS line have occurred as expected based on various communication methods to change the charging level.

Initial Attach Detection

The FUSB300C implements the Type-C Disabled state which removes all termination from the CC pins. In this state, the FUSB300C monitors the CC pins for any activity which indicates that either a host or a device is attempting to attach. When the FUSB300C detects this activity, it interrupts the host software through the WAKE interrupt. The host software can then enable the desired termination based on the required port type and validate the attach per the Type-C specification.

Device Detection and Configuration

A Type-C device must monitor VBUS to determine if it is attached or detached. The FUSB300C provides this information through the VBUSOK interrupt. After the Type-C device knows that a Type-C host has been attached, it needs to determine what type of termination is applied to each CC pin. The software determines if a Ra or Rd termination is present based on the BC_LVL and COMP interrupt and status bits.

Additionally, for Rd terminations, the software can further determine what charging current is allowed by the Type-C host by reading the BC_LVL status bits. This is summarized in Table 1.

Table 1. Device Interrupt Summary

	Interrupt Status				
Status Type	**BC_LVL[1:0]**	**COMP**	**COMP Setting**	**VBUSOK**	**Meaning**
CC Detection	2'b00	NA	NA	1	vRA
	2'b01	NA	NA	1	vRd-Connect and vRd-USB
	2'b10	NA	NA	1	vRd-Connect and vRd-1.5
	2'b11	0	6'b11_0000 (2.05 V)	1	vRd-Connect and vRd-3.0
Attach	NA	NA	NA	1	Host Attached, VBUS Valid
Detach	NA	NA	NA	0	Host Detached, VBUS Invalid

The high level software flow diagram for a Type-C device (UFP) is shown in Figure 6.

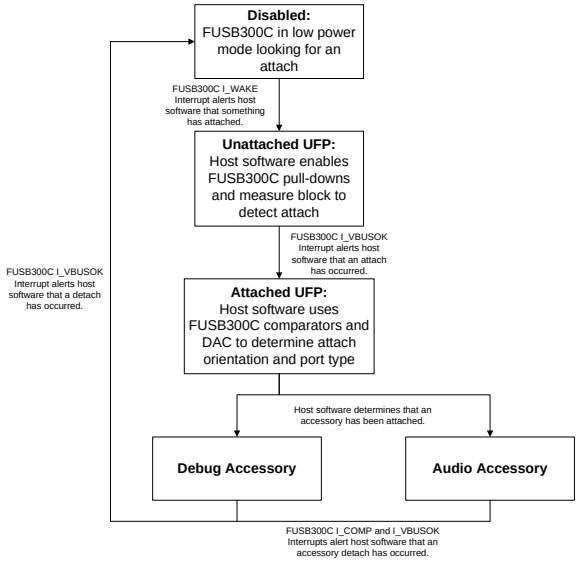


Figure 6. UFP Software Flow

Host Detection and Configuration

When the FUSB300C is configured as a Type-C host, the software can use the status of the comparators and DAC to determine when a Type-C device has been attached or detached and what termination type has been attached to each CC pin.

The FUSB300C allows the host software to change the charging current capabilities of the port through the HOST_CUR control bits. If the HOST_CUR bits are changed prior to attach, the FUSB300C will automatically indicate the programmed current capability when a device is attached. If the current capabilities are changed after a device is attached, the FUSB300C will immediately change the CC line to the programmed capability.

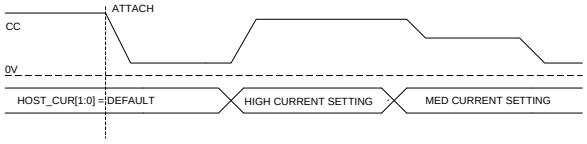


Figure 7. HOST_CUR Changed After Attach

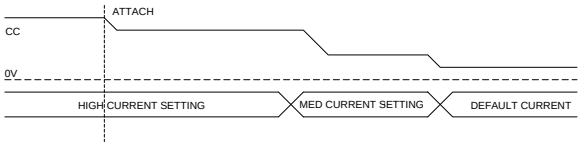


Figure 8. HOST_CUR Changed Prior To Attach

The Type-C specification outlines different attach and detach thresholds for a Type-C host that are based on how much current is supplied to each CC pin. Based on the programmed HOST_CUR setting, the software adjusts the DAC comparator threshold to match the Type-C specification requirements. The BC_LVL comparators can also be used as part of the Ra detection flow. This is summarized in Table 2.

Table 2. Host Interrupt Summary

Termination	HOST_CUR[1:0]	Interrupt Status			Attach/Detach
		BC_LVL[1:0]	COMP	COMP Setting	
Ra	2'b01	2'b00	NA	NA	NA
	2'b10	2'b01	0	6'b00_1000 (0.4 V)	
	2'b11	2'b10	0	6'b01_0010 (0.8 V)	
Rd	2'b01, 2'b10	NA	0	6'b10_0100 (1.6 V)	Attach
		NA	1	6'b10_0100 (1.6 V)	Detach
	2'b11	NA	0	6'b11_1101 (2.6 V)	Attach
		NA	1	6'b11_1101 (2.6 V)	Detach

The high level software flow diagram for a Type-C Host (DFP) is shown below in Figure 9.

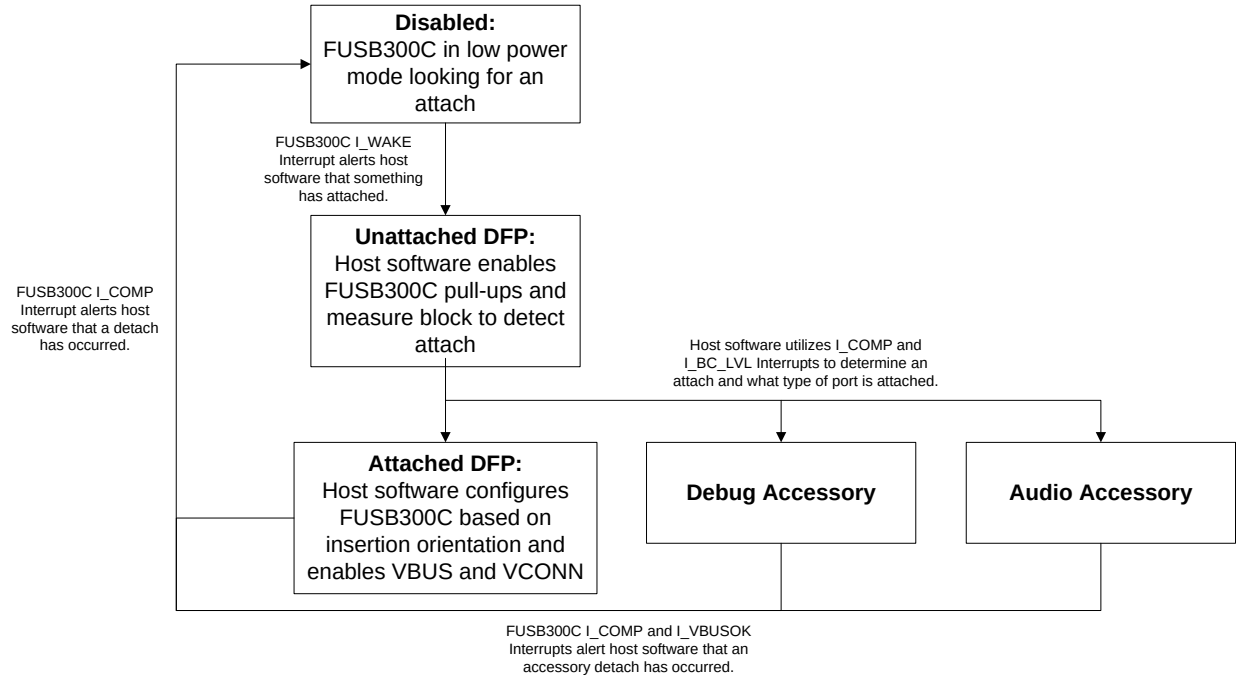


Figure 9. DFP Software Flow

Dual-Role Detection and Configuration

The Type-C specification allows ports to be both a device, or a host depending on what type of port has attached. This functionality is similar to USB OTG ports with the current USB connectors and is called a dual-role port. The FUSB300C can be used to implement a dual-role port. A Type-C dual role port toggles between presenting as a Type-C device and a Type-C host. The host software controls the toggle time and configuration of the FUSB300C in each state as shown in Figure 10.

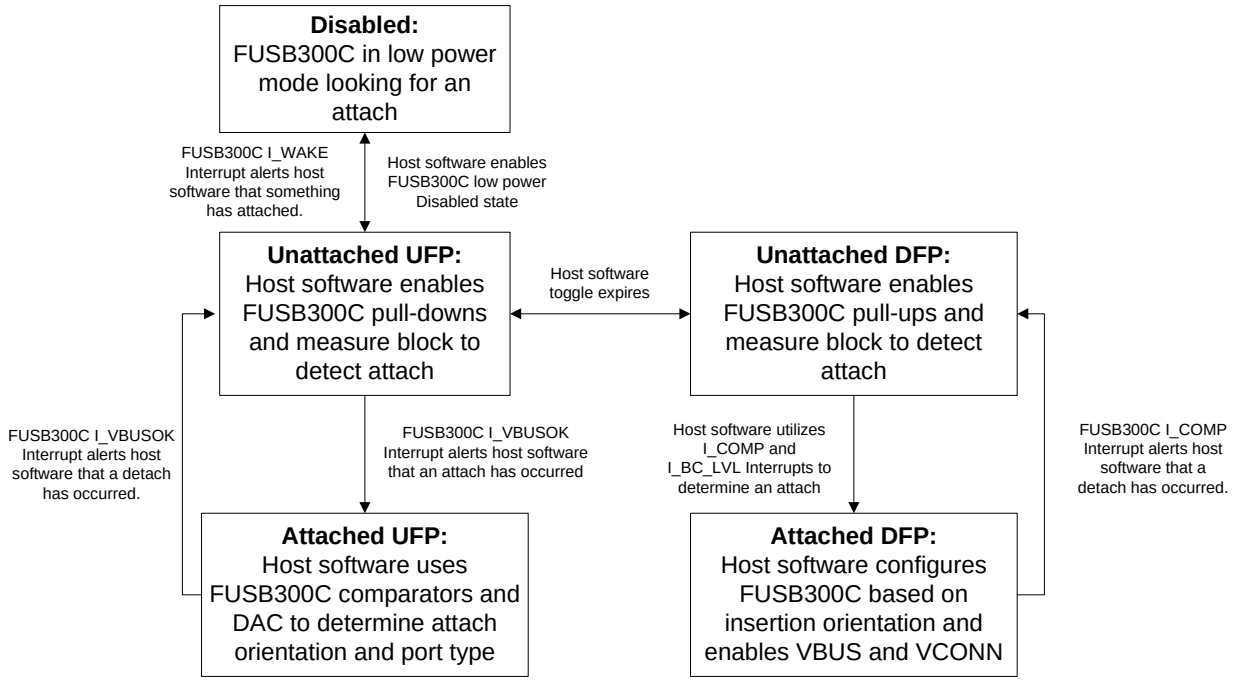


Figure 10. DRP Software Flow

Power Level Determination

The Type-C specification outlines the order of precedence for power level determination which covers power levels from basic USB2.0 levels to the highest levels of USB PD. The host software is expected to follow the USB Type-C specification for charging current priority based on feedback from the FUSB300C detection, external BC1.2 detection and any USB Power Delivery communication.

The FUSB300C does not integrate BC1.2 charger detection which is assumed available in the USB transceiver or USB charger in the system.

Power Up, Initialization and Reset

When power is first applied through VDD, the FUSB300C is reset and registers are initialized to the default values shown in the register map.

The FUSB300C can be reset through software by programming the SW_RES bit in the RESET register.

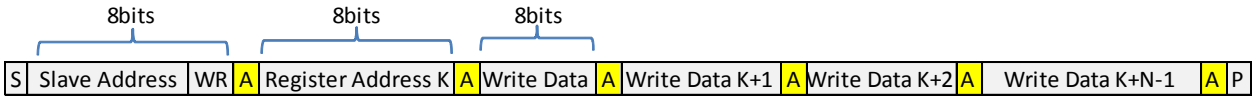
To properly configure the device in low power operation, place a 0.2µF cap on each CC pin and set the following registers:

Address 0x03:	00
Address 0x05:	00
Address 0x06 (bit0):	0
Address 0x06 (bit1):	0
Address 0x06 (bit4):	0
Address 0x07:	00
Address 0x0A (bit0)	1
Address 0x0A (bit3)	1
Address 0x0A (bit4)	0
Address 0x0A (bit6)	1
Address 0x0B (bit4)	0

I²C Interface

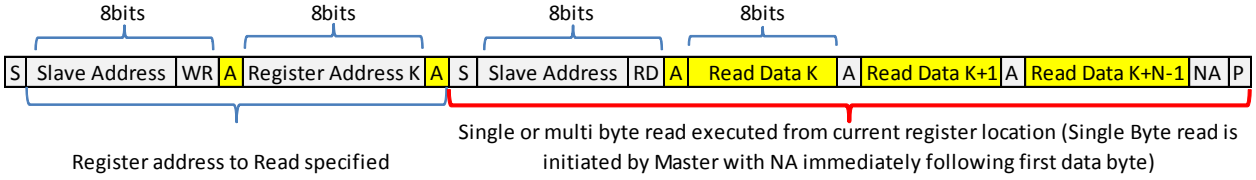
The FUSB300C includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 6 requirements.

This block is designed for fast mode. Examples of an I²C write and read sequence are shown in Figure 11 and Figure 12 respectively.



Note: Single Byte read is initiated by Master with P immediately following first data byte

Figure 11. I²C Write Example



Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

	From Master to Slave	**S**	Start Condition	**NA**	NOT Acknowledge (SDA High)	**RD**	Read =1
	From Slave to Master	**A**	Acknowledge (SDA Low)	**WR**	Write=0	**P**	Stop Condition

Figure 12. I²C Read Example

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
Vv_{DD}	Supply Voltage from V_{DD}			-0.5	6.0	V
V_{CC}	CC Pin Input Voltage			-0.5	6.0	V
V_{VBUS}	VBUS Supply Voltage			-0.5	28.0	V
$T_{STORAGE}$	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System ESD	Connector Pins (VBUS, CCx)	Air Gap	15		kV
			Contact	8		
	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins		2		kV
	Charged Device Model, JEDEC JESD22-C101	All Pins		1		kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{VBUS}	VBUS Supply Voltage	4.0	5.0	21.0	V
V_{VDD}	VDD Supply Voltage	3.0(1)	3.3	3.5	V
V_{CONN}	VCONN Supply Voltage	V_{VDD}		5.50	V
T_A	Operating Temperature	-40		+85	°C

Notes:

1. I^2C registers access functions down to 2.8 V
2. The external I²C pull-up voltage must be 1.8 V (±10%).

Type-C CC Switches[3]

Symbol	Parameter		T_A=-40 to +85°C T_J=-40 to +125°C			Unit
			Min.	Typ.	Max.	
R_{SW_CCx}	R_{DSON} for SW1_CC1 and SW1_CC2	VCONN to CC1 & CC2		0.4	1.5	Ω
I_{TOL_CCX}	Tolerance of CC Current to VDD of 80 µA (default), 180 µA (1.5 A) and 320 µA (3 A)		-8		8	%
R_{DEVICE}	Device Pull-down Resistance (VDD>3.0 V)		4.59	5.10	5.61	kΩ
	Device Pull-down Resistance (VDD=0 V. CCx=2.18 V)		4.08	5.10	6.20	kΩ
zOPEN	CC Resistance for Disabled State		126			kΩ
WAKElow	Wake threshold for CC pin DFP or UFP LOW value. Assumes bandgap and wake circuit turned on ie PWR[0]=1			0.25		V
$WAKE_{high}$	Wake threshold for CC pin DFP or UFP HIGH value. Assumes bandgap and wake circuit turned on ie PWR[0]=1			1.45		V
vBC_LVL	CC Pin Thresholds. Assumes PWR=4'h7	BC=2'b00	0.15	0.20	0.25	V
		BC=2'b01	0.61	0.66	0.70	V
		BC=2'b10	1.16	1.23	1.31	V
vMDACvt	Meas_VBUS=0	MDAC='h08	0.350		0.450	V
		MDAC='h12	0.750		0.850	V
		MDAC='h24	1.50		1.65	V
		MDAC='h30	2.04		2.16	V
		MDAC='h3D	2.45		2.75	V
vMDACstep	Measure block MDAC step size for each code in MDAC[5:0] register from 0 to 'h3D. MEAS_VBUS=0			42		mV
	Measure block MDAC step size for each code in MDAC[5:0] register from 0 to 'h28. MEAS_VBUS=1			375		mV
vVBUSthr	VBUS threshold at which I_VBUSOK interrupt is triggered. Assumes measure block on ie; PWR[2]=1.			4.0		V

Note:

3. For MEAS_VBUS=0, do not exceed register 'h3D. For MEAS_VBUS=1, do not exceed register 'h28.

Current Consumption

Symbol	Parameter	V_{DD} (V)	Conditions	T_A=-40 to +85°C T_J=-40 to +125°C			Unit
				Min.	Typ.	Max.	
Idisable	Disabled Current	3.0 to 3.5	Nothing Attached, No I^2C Transactions. PWR[2:0]='h0			5	µA
Istdby	Standby Current	3.0 to 3.5	Nothing attached, no I2C traffic, PWR[2:0]='h1, Wake block on.		20	40	µA
Idrp	Dual Role Port Unattached Current	3.0 to 3.5	Attached and Monitoring VBUS and CC with Terminations Enabled and Toggling. PWR[2:0]='h7		200		µA
Tshut	Temp. for Vconn Switch Off	3.0 to 3.5			145		°C
Thys	Temp. Hysteresis for Vconn Switch Turn On	3.0 to 3.5			10		°C

IO Specifications(4)

Symbol	Parameter	V_{DD} (V)	Conditions	T_A=-40 to +85°C T_J=-40 to +125°C			Unit
				Min.	Typ.	Max.	
Host Interface Pins(INT_N)							
V_{OLINTN}	Output Low Voltage	3.0 to 3.5	I_{OL}=4 mA			0.4	V
I^2C Interface Pins – Fast Mode (I2C_SDA, I2C_SCL)							
V_{ILI2C}	Low-Level Input Voltage	3.0 to 3.5				0.4	V
V_{IHI2C}	High-Level Input Voltage	3.0 to 3.5		1.2			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 3.5		0.09			V
I_{I2C}	Input Current of SDA and SCL Pins,	3.0 to 3.5	Input Voltage 0.26 V to 2 V	-10		10	µA
I_{CCTI2C}	VDD Current when SDA or SCL is HIGH	3.0 to 3.5	Input Voltage 1.8 V	-10		10	µA
V_{OLSDA}	Low-Level Output Voltage (Open-Drain)	3.0 to 3.5	I_{OL}=3 mA	0		0.3	V
C_I	Capacitance for Each I/O Pin	3.0 to 3.5			5		pF

Note:

4. The external I²C pull-up voltage must be 1.8V (±10%).

I²C Specifications Fast Mode I²C Specification

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	I2C_SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	Low Period of I2C_SCL Clock	1.3		µs
t_{HIGH}	High Period of I2C_SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(5)	100		ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals(5)	20+0.1C_b	300	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals(5)	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	Bus-Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

5. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line $t_{r\_max} + t_{SU;DAT}$ (according to the standard-mode I²C bus specification) before the I2C_SCL line is released.
6. C_b equals the total capacitance of one BUS line in Pf. If mixed with high-speed devices, faster fall times are allowed according to the I²C specification.

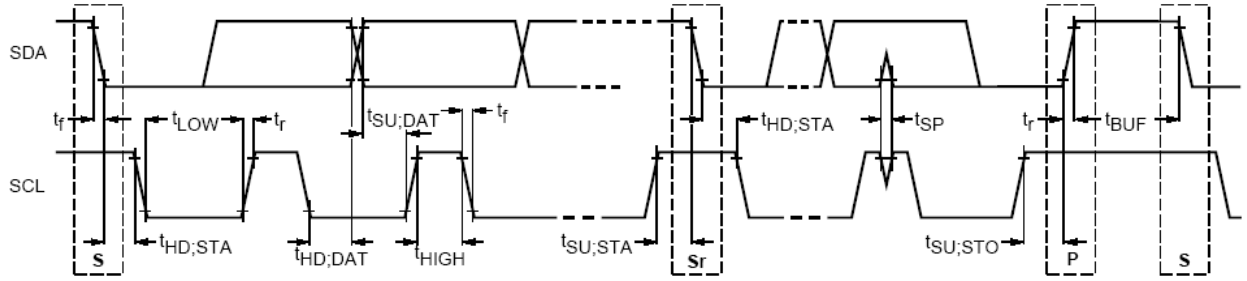


Figure 13. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Table 3. I²C™ Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	0	1	0	R/W

Register Definitions[7]

Address	Register Name	Type	Rst Val	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	Device ID	RO	60	Version ID[3:0]				Revision ID[3:0]			
0x02	Switches0	R/W	03	PU_EN2	PU_EN1	VCONN _CC2	VCONN _CC1	MEAS_CC2	MEAS_CC1	PDWN2	PDWN1
0x03	Reserved			Do Not Use							
0x04	Measure	R/W	00		MEAS_VBUS	MDAC5	MDAC4	MDAC3	MDAC2	MDAC1	MDAC0
0x05	PDDetVT	R/W	20			PDVT5	PDVT4	PDVT3	PDVT2	PDVT1	PDVT0
0x06	Control0	R/W	20			INT_MASK		HOST_CUR1	HOST_CUR0		
0x07	Reserved			Do Not Use							
0x08	Reserved			Do Not Use							
0x09	Reserved			Do Not Use							
0x0A	Mask0	R/W	00	M_VBUSOK	M_FCTY_USE3[9]	M_COMP_CHNG	M_FCTY_USE2[9]	M_FCTY_USE1[9]	M_WAKE	M_FCTY_USE0[9]	M_BC_LVL
0x0B	Power	R/W	0F					PWR3[8]	PWR2	PWR1	PWR0
0x0C	SWReset	W/C	00								SW_RES
0x0C-0x1F	Reserved			Do Not Use							
0x40	Status0	RO	27	VBUSOK	FCTY_USE3[10]	COMP	FCTY_USE2[10]	FCTY_USE1[10]	WAKE	BC_LVL1	BC_LVL0
0x41	Status1	RO	28							OVRTEMP	SHORT
0x42	Interrupt	R/C	25	I_VBUSOK	I_FCTY_USE3[10]	I_COMP_CHNG	I_FCTY_USE2[10]	FCTY_USE1[10]	I_WAKE	I_FCTY_USE0[10]	I_BC_LVL
0x43	Reserved										

Notes:

7. Do not use registers that are blank.
8. Registers for M_FCTY_USEx must be written to “0”
9. Registers for M_FCTY_USEx must be written to “1”
10. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers.

Table 4. Device ID

NOTE: Register descriptions in **BOLD** reflect the default state of the register.
Address: 01h

Reset Value: 0x0110_0000

Type: Read

Bit #	Name	Size (Bits)	Description
7:3	Version ID	5	Device version ID **B_[Revision ID]: 01100 (e.g. A_revB)**
2:0	Revision ID	3	Revision History of each version **[Version ID]_revB: 000 (e.g. A_revB)**

Table 5. Switches0

Address: 02h

Reset Value: 0x0000_0011

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	PU_EN2	1	1: Enable host pull up current to CC2 pin based on Control0 register HOST_CUR[1:0] setting.
6	PU_EN1	1	1: Enable host pull up current to CC1 pin based on Control0 register HOST_CUR[1:0] setting.
5	VCONN _CC2	1	1: Enable the VCONN pin to CC2 pin switch.
4	VCONN _CC1	1	1: Enable the VCONN pin to CC1 pin switch.
3	MEAS_CC2	1	1: Connect the measure block to CC2 pin to monitor or measure the voltage on CC2 pin. Note, PWR=0x07 for proper operation.
2	MEAS_CC1	1	1: Connect the measure block to CC2 pin to monitor or measure the voltage on CC2 pin. Note, PWR=0x07 for proper operation.
1	PDWN2	1	**1: Enable Device pull down on CC2 pin**.
0	PDWN1	1	**1: Enable Device pull down on CC1 pin**.

Table 6. Measure

Address: 04h

Reset Value: 0x0000_0000

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	Reserved	1	Do Not Use
6	MEAS_VBUS	1	1: Measure VBUS with the MDAC/comparator. This requires MEAS_CC* bits in Switches0 register to be 0. **0: MDAC/comparator measurement is controlled by MEAS_CC* bits.**
5:0	MDAC[5:0]	6	Measure Block DAC data input. The step size is vMDACstep which is dependent on Meas_VBUS register setting. Examples are shown below. Valid values from 00_0000 to 11_1001 for MEAS_VBUS=1. Note which CC pin is currently being measured is controlled by the MEAS_CCx bits in the Switches0 register. For MEAS_VBUS=0, do not exceed register 'h3D. For MEAS_VBUS=1, do not exceed register 'h28.

MDAC[5:0]	MEAS_VBUS=0	MEAS_VBUS=1	Unit
00_0000	**0.042**	**0.420**	**V**
00_0001	0.084	0.840	V
11_0000	2.058	20.58	V
11_0011	2.217	21.84	V
11_1110	2.837	26.46	V
11_1111	>2.888	26.88	V

Table 7. PDDetVT

Address: 05h

Reset Value: 0x0010_0000

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:6	Reserved	2	Do Not Use
5:0	PDVT[5:0]	6	The FUSB300C is capable of alerting the host software if the connected device is attempting PD communication. This feature is enabled by default. To disable PD communication detection, this register must be cleared by writing PDVT=0.

Table 8. Control0

Address: 06h

Reset Value: 0x0010_0000

Type: (See Column Below)

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	Reserved	N/A	2	Do Not Use
5	INT_MASK	R/W	1	**1: Mask all interrupts.** 0: Interrupts to host are enabled.
4	Reserved	N/A	1	Do Not Use
3:2	HOST_CUR[1:0]	R/W	2	Controls the host pull-up current enabled by PU_EN[2:1] bits in the Switches0 register: **00: Current disabled** 01: 80 µA – Default USB power. 10: 180 µA – Medium Current Mode: 1.5 A 11: 330 µA – High Current Mode: 3 A
1:0	Reserved	N/A	2	Do Not Use

Table 9. Mask0

Address: 0Ah

Reset Value: 0x0000_0000

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	M_VBUSOK	1	1: Mask I_VBUSOK interrupt bit. **0: Do not mask.**
6	M_FCTY_USE3	1	1: Must be written for this bit.
5	M_COMP_CHNG	1	1: Mask I_COMP_CHNG interrupt bit. **0: Do not mask.**
4	M_FCTY_USE2	1	1: Must be written for this bit.
3	M_FCTY_USE1	1	1: Must be written for this bit.
2	M_WAKE	1	1: Mask I_WAKE interrupt bit. **0: Do not mask.**
1	M_FCTY_USE0	1	1: Must be written for this bit.
0	M_BC_LVL	1	1: Mask I_BC_LVL interrupt bit. **0: Do not mask.**

Table 10. Power

Address: 0Bh

Reset Value: 0x0000_0111

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	Reserved	4	Do Not Use
3:0	PWR[3:0]	4	Power enables: PWR[0]: Bandgap and wake circuit. PWR[1]: Current references for measure block. PWR[2]: Measure block powered. PWR[3]: Must be written to 0. It is expected that PWR=4'h1 is used for low power WAKE detection. PWR=4'h7 is used for all other detection

Table 11. SWReset

Address: 0Ch

Reset Value: 0x0000_0000

Type: Write/Clear

Bit #	Name	Size (Bits)	Description
7:6	Reserved	4	Do Not Use
0	SW_RES	1	1: Software reset. Resets the FUSB300C, including all the registers.

Table 12. Status0

Address: 40h

Reset Value: 0x0010_0111

Type: Read

Bit #	Name	Size (Bits)	Description
7	VBUSOK	1	1: VBUS is higher than vVBUSthr threshold. 0: VBUS is lower than vVBUSthr threshold.
6	FCTY_USE3	1	Factory use only. Do not use.
5	COMP	1	1: Measured CC* input is higher than reference level driven from the MDAC. **0: Measured CC* input is lower than reference level driven from the MDAC.**
4	FCTY_USE2	1	Factory use only. Do not use.
3	FCTY_USE1	1	Factory use only. Do not use.
2	WAKE	1	1: Voltage on CCx indicated that either a device, host or dual-role port is attempting to attach.
1:0	BC_LVL[1:0]	2	Current voltage status of the measured CC pin interpreted as host current levels as follows: 00: < 200 mV (vRA) 01: >200 mV, <660 mV (vRd-USB) 10: >660 mV, <1.23 V (vRd-1.5) 11:>1.23 V (vRd-3.0*) Note the software must measure these at an appropriate time, while there is no signaling activity on the selected CC line. *require use of properly set DAC and COMP interrupt for detection of vRD-3.0.

Table 13. Status1

Address: 41h

Reset Value: 0x0010_1000

Type: Read

Bit #	Name	Size (Bits)	Description
7:2	Reserved	6	Do not use.
1	OVRTEMP	1	1: Temperature of the device has exceeded Tshut temperature.
0	SHORT	1	1: Indicates an over-current or short condition has occurred on the VCONN switch. This feature is guaranteed for VCONN=3.0V.

Table 14. Interrupt

Address: 42h

Reset Value: 0x0010_0101

Type: Write/Clear

Bit #	Name	Size (Bits)	Description
7	I_VBUSOK	1	1: A change in the value of VBUSOK has occurred. This bit typically is used to recognize a port partner attach or detach when configured as a device/upstream facing port.
6	I_FCTY_USE3	1	Factory use only. Do not use.
5	I_COMP_CHNG	1	1: A change in the value of COMP has occurred. Indicates selected CC line has tripped a threshold programmed into the MDAC. This bit is typically used as an attach/detach threshold when configured as a host/downstream facing port or as part of the charging current detection when configured as a device/upstream facing port.
4	I_FCTY_USE2	1	Factory use only. Do not use.
3	I_FCTY_USE1	1	Factory use only. Do not use.
2	I_WAKE	1	1: A change in the value of WAKE has occurred. This bit is typically used to detect that something is trying to attach to the FUSB300C and starts the software to determine what type of device is attached and the orientation of the attach.
1	I_FCTY_USE0	1	Factory use only. Do not use.
0	I_BC_LVL	1	1: A change in BC_LVL has occurred. This bit is typically used to indicate that the host has changed the allowed charging current level on the connected CC pin.

Reference Schematic

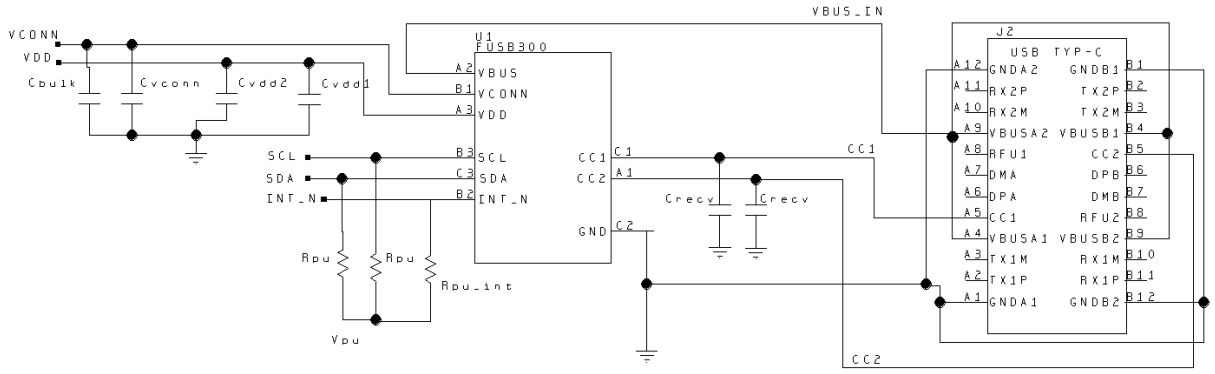


Figure 14. Reference Schematic Diagram

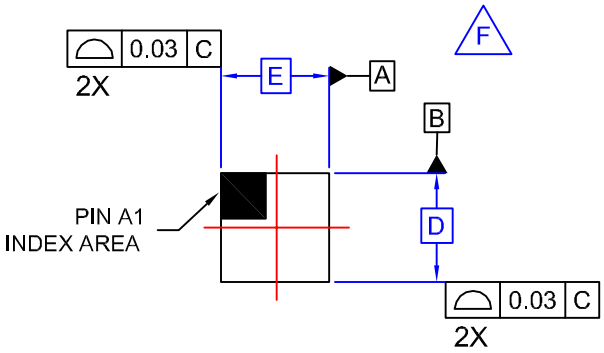
Table 15. Recommended Component Values for Reference Schematic

Symbol	Parameter	Recommended Value			Unit	Notes
		Min.	Typ.	Max.		
C_{RECV}	CC_X Receiver Capacitance	0.2		2.2	µF	
C_{BULK}	VCONN Source Bulk Capacitance	10		220	µF	Section 4.4.3, USB Type-C Specification Revision 1.0
C_{VCONN}	VCONN Decoupling Capacitance		0.1		µF	
C_{VDD1}	V_{DD} Decoupling Capacitance		0.1		µF	
C_{VDD2}	V_{DD} Decoupling Capacitance		1.0		µF	
R_{PU}	I2C Pull-up Resistors		4.7		kΩ	These values are application specific
R_{PU_INT}	INT_N pull-up Resistor	1	4.7		kΩ	
V_{PU}	I2C Pull-up Voltage	1.62	1.8	1.98	V	

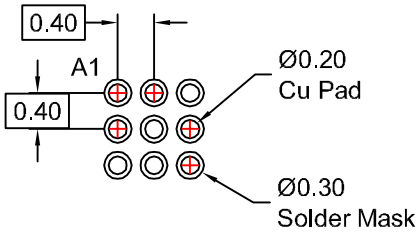
Product-Specific Dimensions

Product	D	E	X	Y
FUSB300CUCX	1.215 mm	1.215 mm	0.208 mm	0.208 mm

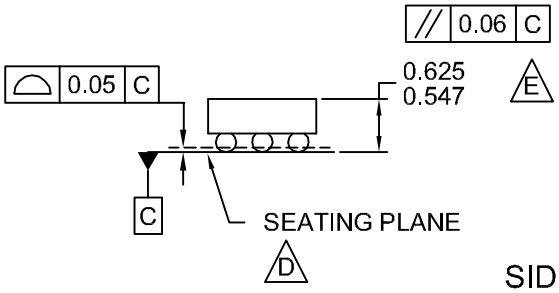
REVISIONS			
REV	DESCRIPTION	DATE	BY/SITE
1	INITIAL DRAWING RELEASE.	2-15-2008	L. ENGLAND/FSME
2	Updated land pattern to individual solder mask openings. Removed solder alloy note. Other misc updates for standardization.	4-9-2010	L. ENGLAND/FSME

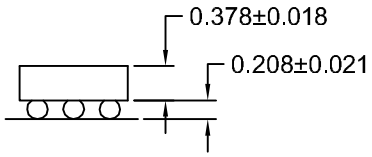


TOP VIEW

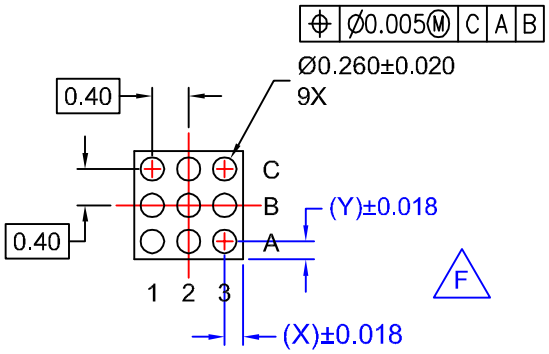


LAND PATTERN RECOMMENDATION
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC009ABrev2

APPROVALS	DATE
DRAWN L. England	4-9-10
DFTG. CHK. H. Allen	4-9-10
ENGR. CHK.	

FAIRCHILD SEMICONDUCTOR™

9 BALL WLCSP, 3X3 ARRAY
0.4MM PITCH, 250UM BALL

PROJECTION
INCH
[MM]

SCALE	SIZE	DRAWING NUMBER	REV
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