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January 2011

Single-Channel: 6N137, HCPL2601, HCPL2611 Dual-Channel: HCPL2630, HCPL2631 High Speed 10MBit/s Logic Gate Optocouplers

Features

- Very high speed 10 MBit/s
- Superior CMR 10 kV/µs
- Double working voltage-480V
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)

Applications

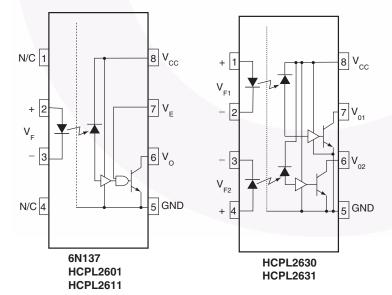
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

Description

The 6N137, HCPL2601, HCPL2611 single-channel and HCPL2630, HCPL2631 dual-channel optocouplers consist of a 850 nm AlGaAS LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5mA will provide a minimum output sink current of 13mA (fan out of 8).

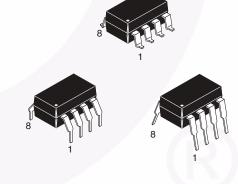
An internal noise shield provides superior common mode rejection of typically $10kV/\mu s$. The HCPL2601 and HCPL2631 has a minimum CMR of $5kV/\mu s$. The HCPL2611 has a minimum CMR of $10kV/\mu s$.

Schematics



A $0.1\mu F$ bypass capacitor must be connected between pins 8 and $5^{(1)}$.

Package Outlines



Truth Table (Positive Logic)

	` ,	
Input	Enable	Output
Н	Н	L
L	Н	Н
Н	L	Н
L	L	Н
Н	NC	L
L	NC	Н

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Param	Value	Units	
T _{STG}	Storage Temperature	-55 to +125	°C	
T _{OPR}	Operating Temperature		-40 to +85	°C
T _{SOL}	Lead Solder Temperature (for wave s	oldering only)*	260 for 10 sec	°C
EMITTER				
I _F	DC/Average Forward	Single Channel	50	mA
	Input Current	Dual Channel (Each Channel)	30	
V _E	Enable Input Voltage Not to Exceed V _{CC} by more than 500mV	Single Channel	5.5	V
V _R	Reverse Input Voltage	Each Channel	5.0	V
Pı	Power Dissipation	Single Channel	100	mW
	Dual Channel (Each Channel)		45	
DETECTOR				
V _{CC} (1 minute max)	Supply Voltage		7.0	V
I _O	Output Current	Single Channel	50	mA
		Dual Channel (Each Channel)	50	
Vo	Output Voltage	Each Channel	7.0	V
Po	Collector Output Single Channel		85	mW
	Power Dissipation	Dual Channel (Each Channel)	60	

^{*}For peak soldering reflow, please refer to the Reflow Profile on page 11.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
I _{FL}	Input Current, Low Level	0	250	μΑ
I _{FH}	Input Current, High Level	*6.3	15	mA
V _{CC}	Supply Voltage, Output	4.5	5.5	V
V _{EL}	Enable Voltage, Low Level	0	0.8	V
V _{EH}	Enable Voltage, High Level	2.0	V _{CC}	V
T _A	Low Level Supply Current	-40	+85	°C
N	Fan Out (TTL load)		8	

^{*6.3}mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less.

Electrical Characteristics (T_A = 0 to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions		Min.	Тур.*	Max.	Unit
EMITTER				!			
V _F	Input Forward Voltage	I _F = 10mA				1.8	V
			$T_A = 25^{\circ}C$		1.4	1.75	
B _{VR}	Input Reverse Breakdown Voltage	I _R = 10μA		5.0			V
C _{IN}	Input Capacitance	V _F = 0, f = 1MHz			60		pF
$\Delta V_F / \Delta T_A$	Input Diode Temperature Coefficient	I _F = 10mA			-1.4		mV/°C
DETECTOR	?						
I _{CCH}	High Level Supply Current	$V_{CC} = 5.5V, I_F = 0mA,$	Single Channel		7	10	mA
		$V_E = 0.5V$	Dual Channel		10	15	
I _{CCL}	Low Level Supply Current	Single Channel	$V_{CC} = 5.5V$, $I_F = 10mA$		9	13	mA
		Dual Channel	$V_{E} = 0.5V$		14	21	
I _{EL}	Low Level Enable Current	$V_{CC} = 5.5V, V_{E} = 0.5V$			-0.8	-1.6	mA
I _{EH}	High Level Enable Current	$V_{CC} = 5.5V, V_{E} = 2.0V$			-0.6	-1.6	mA
V _{EH}	High Level Enable Voltage	$V_{CC} = 5.5V, I_F = 10mA$		2.0			V
V _{EL}	Low Level Enable Voltage	$V_{CC} = 5.5V, I_F = 10mA^{(3)}$				0.8	V

Switching Characteristics ($T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_{CC} = 5V$, $I_F = 7.5$ mA unless otherwise specified)

Symbol	AC Characteristics	Test Co	nditions	Min.	Тур.*	Max.	Unit
T _{PLH}	Propagation Delay	$R_L = 350\Omega,$ $C_L = 15pF^{(4)}$ (Fig. 12)	$T_A = 25^{\circ}C$	20	45	75	ns
	Time to Output HIGH Level	$C_L = 15pr^{(1)}$ (Fig. 12)				100	
T_PHL	Propagation Delay	$T_A = 25^{\circ}C^{(5)}$		25	45	75	ns
	Time to Output LOW Level	$R_L = 350\Omega, C_L = 15pF$ (Fig. 12)			100	
IT _{PHL} -T _{PLH} I	Pulse Width Distortion	$(R_L = 350\Omega, C_L = 15pF)$	(Fig. 12)		3	35	ns
t _r	Output Rise Time (10–90%)	$R_L = 350\Omega, C_L = 15pF^{(6)}$	⁽⁾ (Fig. 12)		50		ns
t _f	Output Rise Time (90–10%)	$R_L = 350\Omega, C_L = 15pF^{(7)}$	(Fig. 12)		12		ns
t _{ELH}	Enable Propagation Delay Time to Output HIGH Level	$I_F = 7.5$ mA, $V_{EH} = 3.5$ V, $R_L = 350\Omega$, $C_L = 15$ pF $^{(8)}$ (Fig. 13)			20		ns
t _{EHL}	Enable Propagation Delay Time to Output LOW Level	I _F = 7.5mA, V _{EH} = 3.5V, (Fig. 13)	$R_L = 350\Omega, C_L = 15pF^{(9)}$		20		ns
ICM _H I	Common Mode	$T_A = 25^{\circ}C, V_{CM} = 50V$	6N137, HCPL2630		10,000		V/µs
	Transient Immunity (at Output HIGH Level)	(Peak), $I_F = 0mA$, V_{OH} (Min.) = 2.0V, $R_L = 350Ω^{(10)}$ (Fig. 14)	HCPL2601, HCPL2631	5000	10,000		
		V _{CM} = 400V	HCPL2611	10,000	15,000		V/µs
ICM _L I Common Mode	$R_L = 350\Omega, I_F = 7.5 \text{mA},$	6N137, HCPL2630		10,000			
	Transient Immunity (at Output LOW Level)	V_{OL} (Max.) = 0.8V, $T_A = 25^{\circ}C^{(11)}$ (Fig. 14)	HCPL2601, HCPL2631	5000	10,000		
		IV _{CM} = 400V	HCPL2611	10,000	15,000		

Electrical Characteristics (Continued)

Transfer Characteristics (T_A = -40 to +85°C unless otherwise specified)

Symbol	DC Characteristics	Test Conditions	Min.	Тур.*	Max.	Unit
I _{OH}	HIGH Level Output Current	$V_{CC} = 5.5V, V_O = 5.5V,$ $I_F = 250\mu A, V_E = 2.0V^{(2)}$			100	μΑ
V _{OL}	LOW Level Output Current	$V_{CC} = 5.5V$, $I_F = 5mA$, $V_E = 2.0V$, $I_{CL} = 13mA^{(2)}$.35	0.6	V
I _{FT}	Input Threshold Current	$V_{CC} = 5.5V, V_O = 0.6V, V_E = 2.0V,$ $I_{OL} = 13mA$		3	5	mA

Isolation Characteristics (T_A = -40°C to +85°C unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Тур.*	Max.	Unit
I _{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25$ °C, $t = 5s$, $V_{I-O} = 3000 \text{ VDC}^{(12)}$			1.0*	μА
V _{ISO}	Withstand Insulation Test Voltage	RH < 50%, $T_A = 25$ °C, $I_{I-O} \le 2\mu A$, $t = 1 \text{ min.}^{(12)}$	2500			V _{RMS}
R _{I-O}	Resistance (Input to Output)	$V_{I-O} = 500V^{(12)}$		10 ¹²		Ω
C _{I-O}	Capacitance (Input to Output)	$f = 1MHz^{(12)}$		0.6		pF

^{*}All Typicals at $V_{CC} = 5V$, $T_A = 25$ °C

Notes:

- The V_{CC} supply to each optoisolator must be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic
 or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible
 to the package V_{CC} and GND pins of each device.
- 2. Each channel.
- 3. Enable Input No pull up resistor required as the device has an internal pull up resistor.
- 4. t_{PLH} Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- 5. t_{PHL} Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- 6. t_r Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- 7. t_f Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- 8. t_{ELH} Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
- 9. t_{EHL} Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
- 10. CM_H The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., $V_{OLIT} > 2.0V$). Measured in volts per microsecond (V/μ s).
- 11. CM_L The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V). Measured in volts per microsecond (V/μs).</p>
- 12. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Typical Performance Curves

Fig.1 Low Level Output Voltage vs. Ambient Temperature

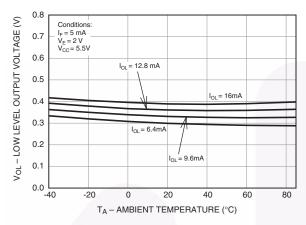


Fig. 2 Input Diode Forward Voltage vs. Forward Current

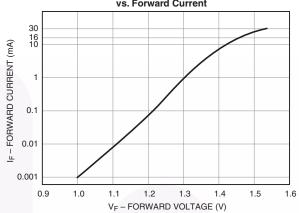


Fig.3 Switching Time vs. Forward Current

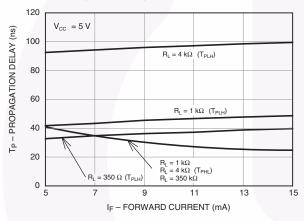


Fig. 4 Low Level Output Current vs. Ambient Temperature

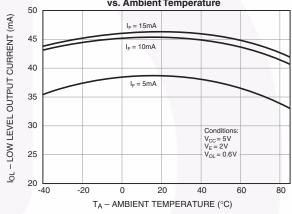


Fig. 5 Input Threshold Current

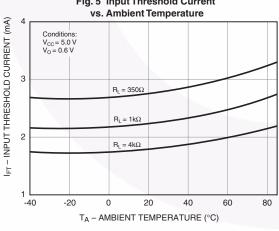
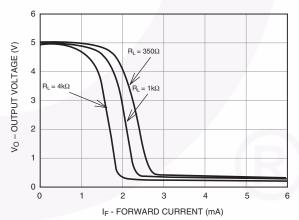
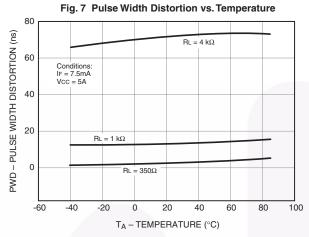
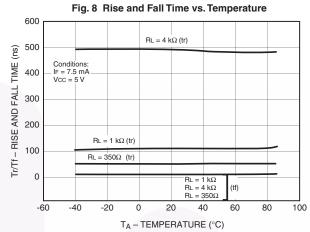


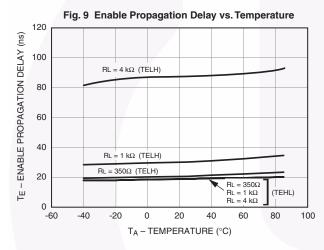
Fig. 6 Output Voltage vs. Input Forward Current

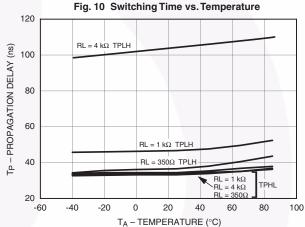


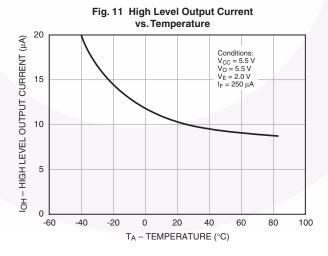
Typical Performance Curves (Continued)











Test Circuits

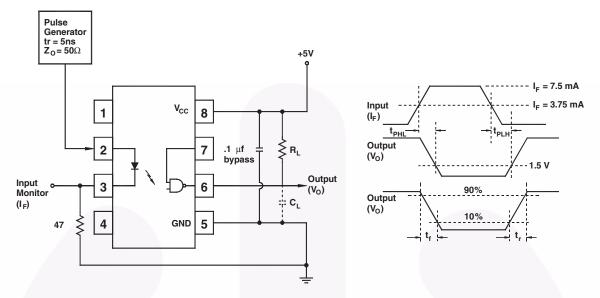


Fig. 12 Test Circuit and Waveforms for $t_{\text{PLH}},\,t_{\text{PHL}},\,t_{\text{r}}$ and t_{f}

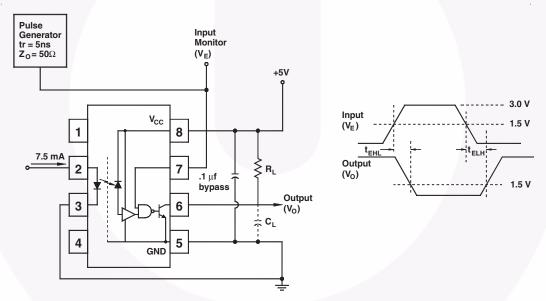


Fig. 13 Test Circuit t_{EHL} and t_{ELH}

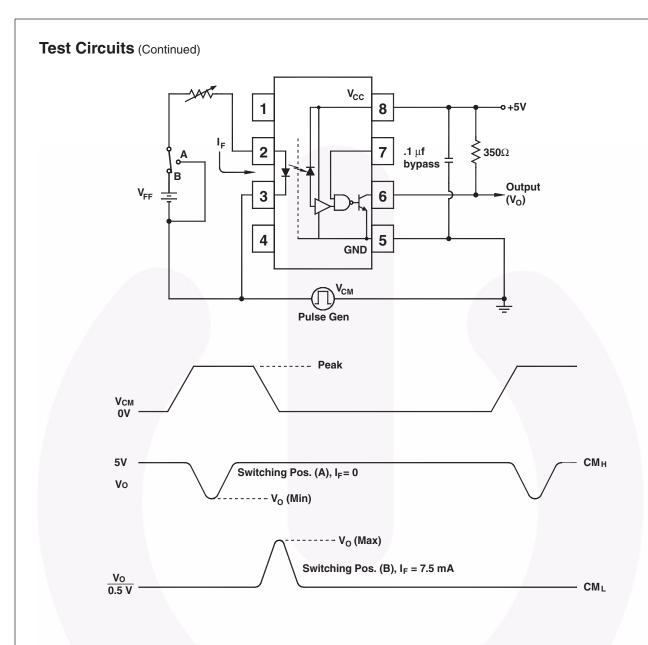
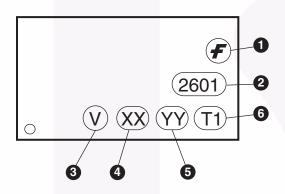


Fig. 14 Test Circuit Common Mode Transient Immunity

Ordering Information

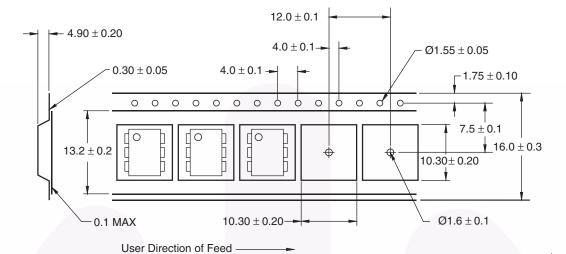
Option	Example Part Number	Description
S	6N137S	Surface Mount Lead Bend
SD	6N137SD	Surface Mount; Tape and Reel
W	6N137W	0.4" Lead Spacing
V	6N137V	VDE0884
WV	6N137WV	VDE0884; 0.4" Lead Spacing
SV	6N137SV	VDE0884; Surface Mount
SDV	6N137SDV	VDE0884; Surface Mount; Tape and Reel

Marking Information

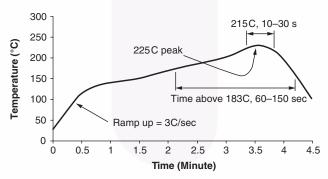


Definiti	Definitions						
1	Fairchild logo						
2	Device number						
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)						
4	Two digit year code, e.g., '03'						
5	Two digit work week ranging from '01' to '53'						
6	Assembly package code						

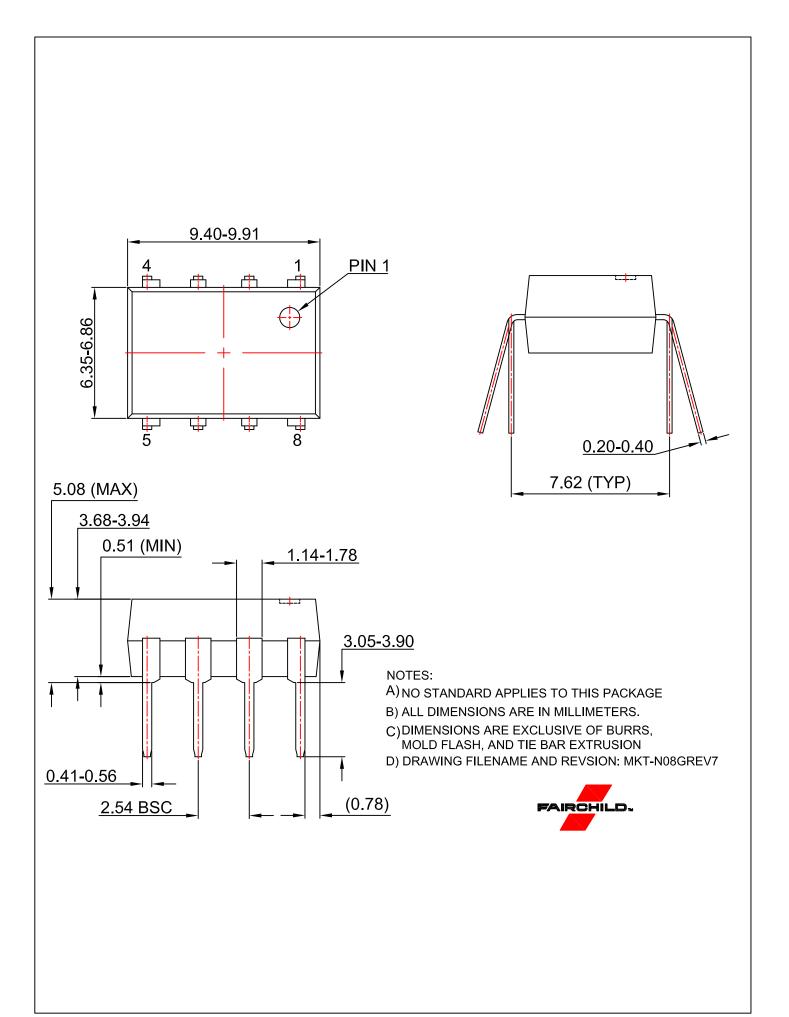
Tape Specifications

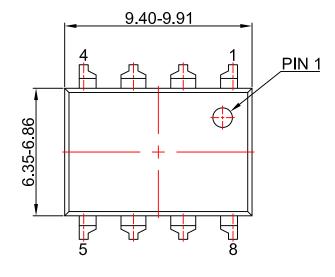


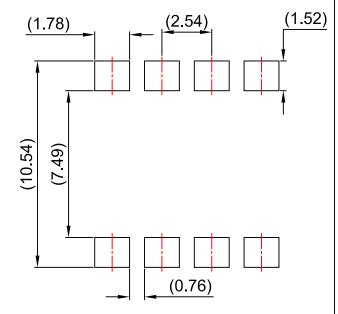
Reflow Profile

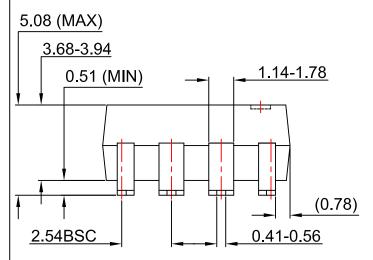


- Peak reflow temperature: 225C (package surface temperature)
 Time of temperature higher than 183C for 60–150 seconds
 One time soldering reflow is recommended

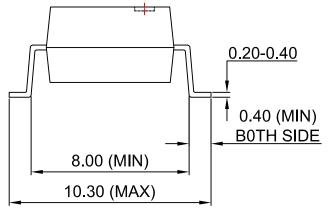








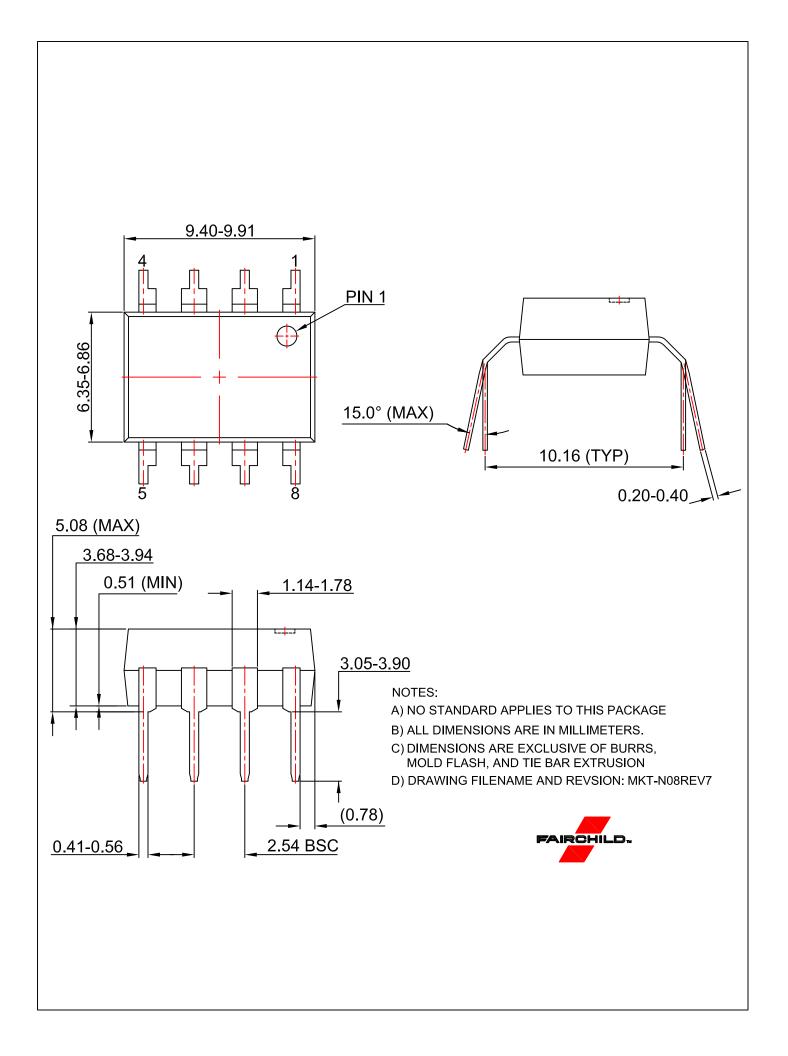




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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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