

# KSD526 NPN Epitaxial Silicon Transistor

# **Power Amplifier Applications**

Complement to KSB596



1.Base 2.Collector 3.Emitter

# Absolute Maximum Ratings \* T<sub>a</sub> = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V <sub>CBO</sub>	Collector-Base Voltage	80	V
V <sub>CEO</sub>	Collector-Emitter Voltage	80	V
V <sub>EBO</sub>	Emitter-Base Voltage	5	V
I <sub>C</sub>	Collector Current	4	A
I <sub>B</sub>	Base Current	0.4	A
P <sub>C</sub>	Collector Dissipation (T <sub>C</sub> =25°C)	30	W
TJ	Junction Temperature	150	°C
T <sub>STG</sub>	Storage Temperature	-55~150	°C

\* These ratings are limiting values above which the serviceability of any semiconductor device may by impaired.

# **Electrical Characteristics** $T_{C} = 25^{\circ}C$ unless otherwise noted

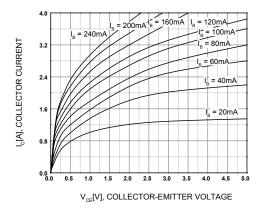
Symbol	Parameter	Test Condition	MIN	MAX	MAX	Units
I <sub>CBO</sub>	Collector Cut-off Current	V <sub>CB</sub> = 80V, I <sub>E</sub> = 0			30	μA
I <sub>EBO</sub>	Emitter Cut-off Current	V <sub>EB</sub> = 5V, I <sub>C</sub> = 0			100	μA
BV <sub>CEO</sub>	Collector-Emitter Breakdown Voltage	I <sub>C</sub> = 50mA, I <sub>B</sub> = 0	80			V
BV <sub>EBO</sub>	Emitter-Base Breakdown Voltage	I <sub>E</sub> = 10mA, I <sub>C</sub> = 0	5			V
hfe	DC Current Gain	$V_{CE} = 5V, I_C = 0.5A$ $V_{CE} = 5V, I_C = 3A$	40 15	50	240	
Vce(sat)	Collector-Emitter Saturation Voltage	I <sub>C</sub> = 3A, I <sub>B</sub> = 0.3A		0.45	1.5	V
VBE(on)	Base-Emitter On Voltage	V <sub>CE</sub> = 5V, I <sub>C</sub> = 3A		1	1.5	V
fr	Current Gain - Bandwidth Product	V <sub>CE</sub> = 5V, I <sub>C</sub> = 0.5A	3	8		MHz
Ccb	Collector Output Capacitance	V <sub>CB</sub> = 10V, I <sub>E</sub> = 0, f = 1MHz		90		pF

## h<sub>FE</sub> Classification

Classification	R	0	Y
h <sub>FE</sub>	40~80	70~140	120~240

# **KSD526** Power Amplifier Applications

# **Typical Characteristics**



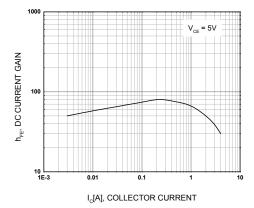
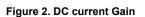
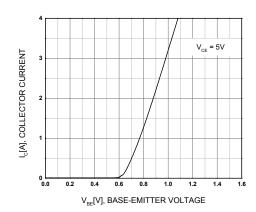


Figure 1. Static Characteristic







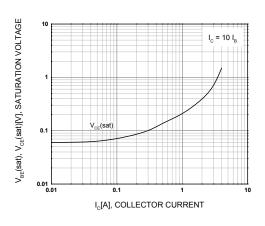


Figure 4. Collector-Emitter Saturation Voltage

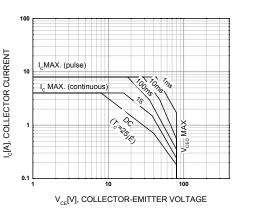


Figure 5. Safe Operating Area

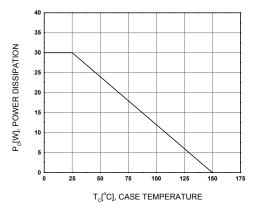
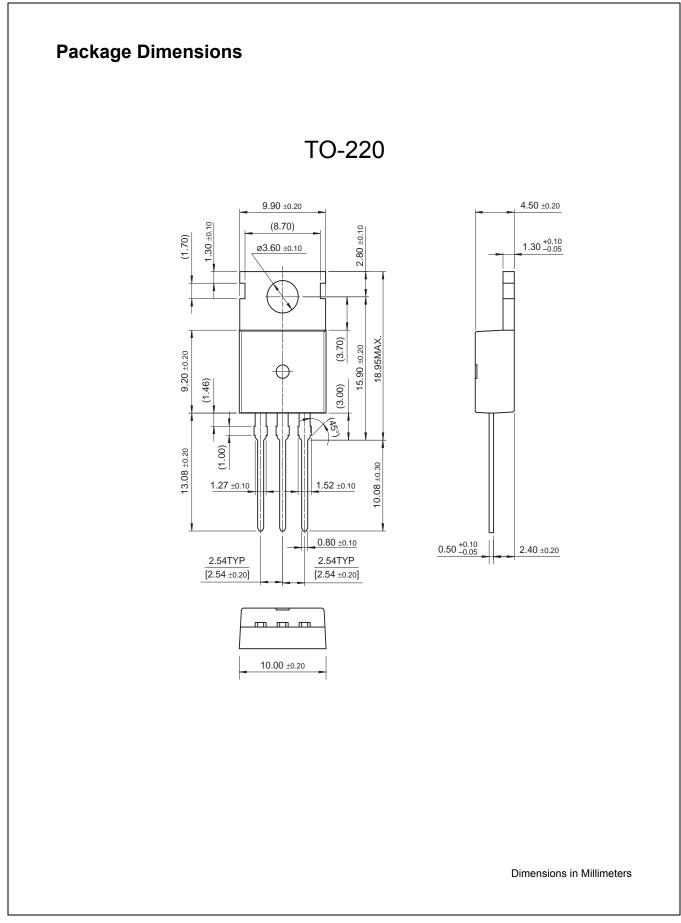


Figure 6. Power Derating



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