January 2015

KA78M05 / LM78M05 / MC78M05
3-Terminal 0.5 A Positive Voltage Regulator

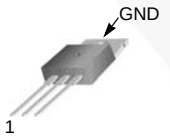
Features

- Output Current up to 0.5 A
- Output Voltages of 5 V
- Thermal Overload Protection
- Short-Circuit Protection
- Output Transistor Safe Operating Area (SOA) Protection

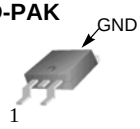
Description

The KA78M05 / LM78M05 / MC78M05 series of three-terminal positive regulators is available in the TO-220 / D-PAK packages, making it useful in a wide range of applications.

TO-220



D-PAK



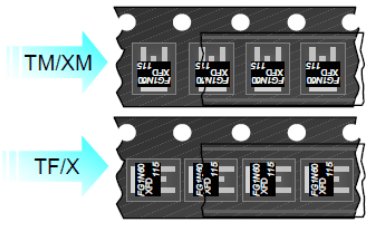
1. Input 2. GND 3. Output

Ordering Information(1)

Product Number	Package	Packing Method	Operating Temperature
KA78M05TU	TO-220 (Dual Gauge)	Rail	-40 to +125°C
KA78M05RTM	D-PAK	Tape and Reel	
MC78M05CDTX			
LM78M05CT	TO-220 (Single Gauge)	Rail	

Note:

1. Refer to below figure for TM / TF suffix of DPAK packing option.



D-PAK Unit Orientation

Block Diagram

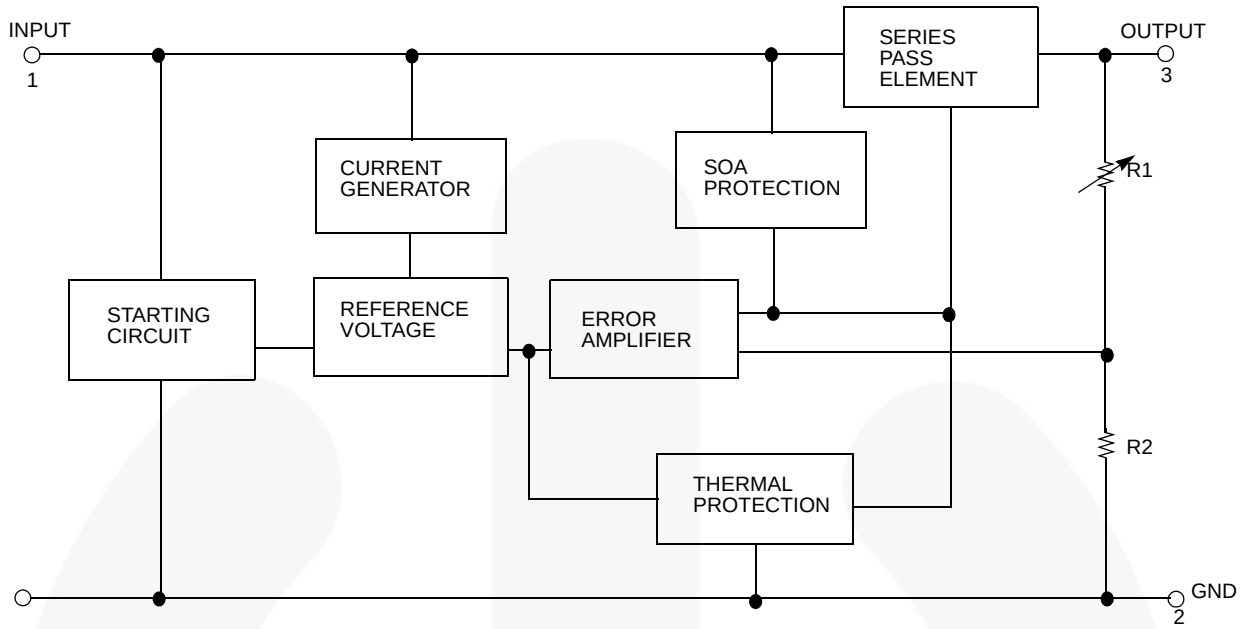


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Value	Unit
V_I	Input Voltage (for V_O = 5 V)		35	V
$R_{\theta JC}$	Thermal Resistance, Junction-Case(2)	TO-220 (T_C = +25°C)	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-Air(2), (3)	TO-220 (T_A = +25°C)	66	°C/W
		D-PAK (T_A = +25°C)	92	
T_{OPR}	Operating Junction Temperature Range		-40 to +125	°C
$T_{J(MAX)}$	Maximum Junction Temperature Range		150	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

Notes:

2. Thermal resistance test board.
   Size: 76.2 mm x 114.3 mm x 1.6 mm (1S0P)
   JEDEC standard: JESD51-3, JESD51-7
3. Assume no ambient airflow.

Electrical Characteristics

Refer to the test circuits, $-40 \leq T_J \leq +125°C$, I_O = 350 mA, V_I = 10 V, C_I = 0.33 µF, C_O = 0.1 µF unless otherwise specified.(4)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.8	5.0	5.2	V
		I_O = 5 mA to 350 mA, V_I = 7 V to 20 V		4.75	5.00	5.25	
ΔV_O	Line Regulation(5)	I_O = 200 mA, T_J = +25°C	V_I = 7 V to 25 V			100	mV
			V_I = 8 V to 25 V			50	
ΔV_O	Load Regulation(5)	I_O = 5 mA to 0.5 A, T_J = +25°C				100	mV
		I_O = 5 mA to 200 mA, T_J = +25 °C				50	
I_Q	Quiescent Current	T_J = +25°C			4.0	6.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5 mA to 350 mA				0.5	mA
		I_O = 200 mA, V_I = 8 V to 25 V				0.8	
$\Delta V/\Delta T$	Output Voltage Drift	I_O = 5 mA, T_J = -40 to +125°C			-0.5		mV/°C
V_N	Output Noise Voltage	f = 10 Hz to 100 kHz			40		µV/Vo
RR	Ripple Rejection	f = 120 Hz, I_O = 300 mA, V_I = 8 V to 18 V, T_J = +25 °C			80		dB
V_D	Dropout Voltage	T_J = +25°C, I_O = 500 mA			2		V
I_{SC}	Short-Circuit Current	T_J = +25°C, V_I = 35 V			300		mA
I_{PK}	Peak Current	T_J = +25°C			700		mA

Notes:

4. The parameters are guaranteed across the temperature range by characterization.
5. Load and line regulation are specified at constant junction temperature. Change in V_o due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Applications(6), (7)

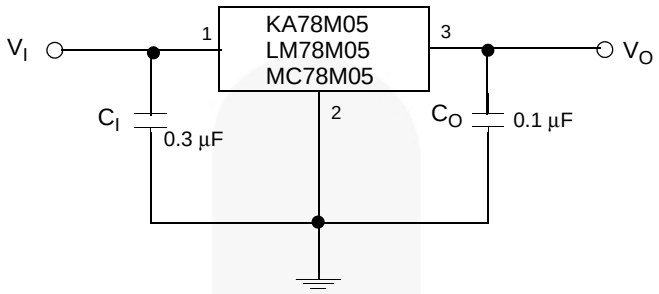


Figure 2. Fixed-Output Regulator

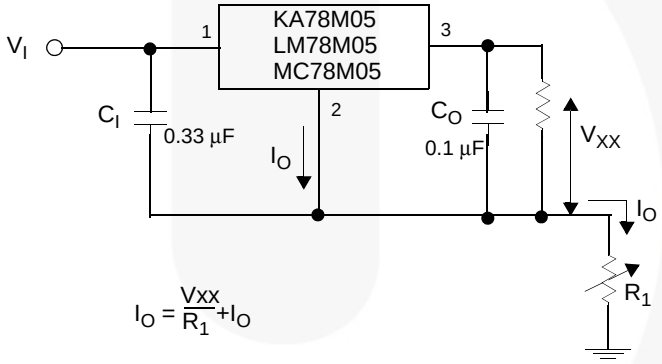


Figure 3. Constant-Current Regulator

Notes:

6. C_I is required if the regulator is located an appreciable distance from the power supply filter.
7. Although no output capacitor is needed for stability, it does improve transient response.

Typical Applications (Continued)

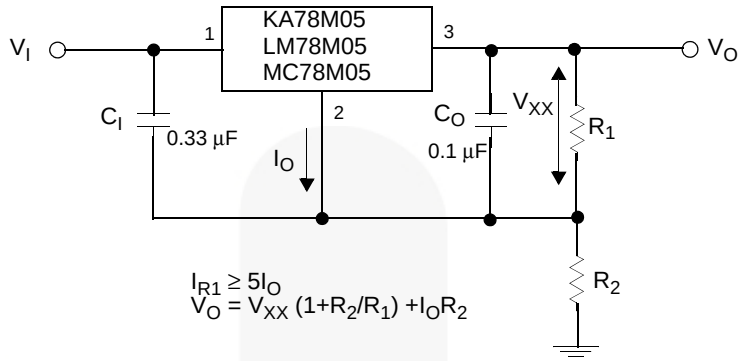


Figure 4. Circuit for Increasing Output Voltage

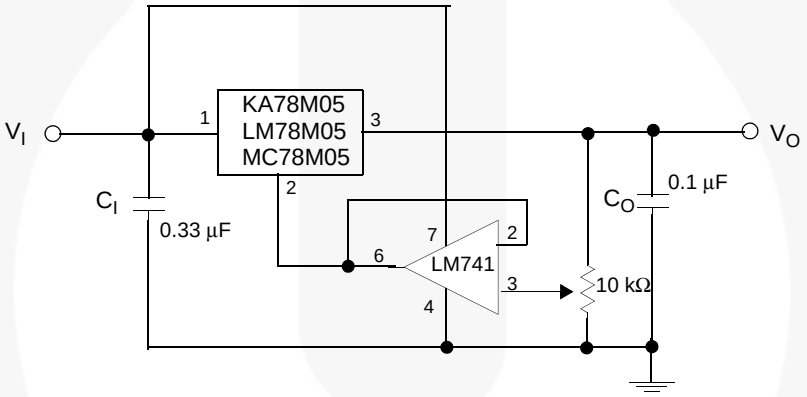


Figure 5. Adjustable Output Regulator (7 to 30 V)

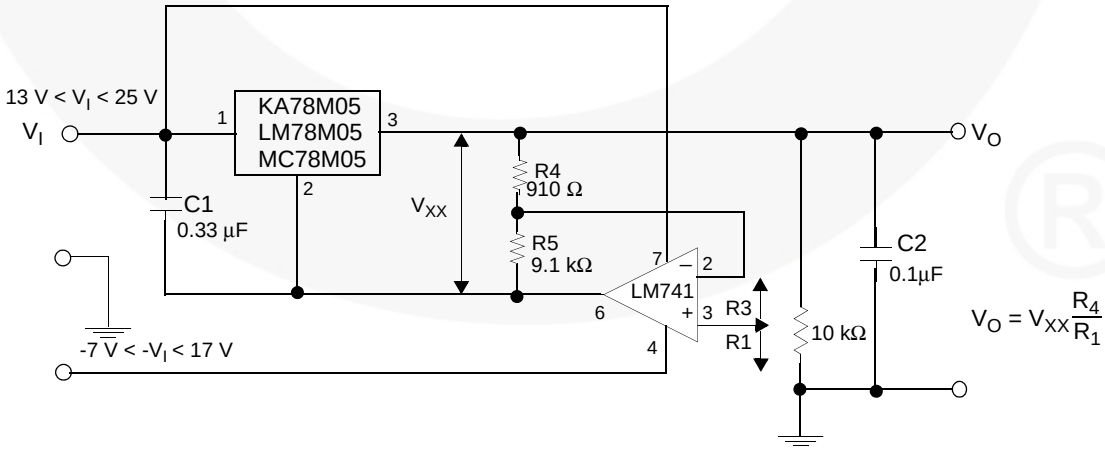


Figure 6. 0.5 to 10 V Regulator

Physical Dimensions

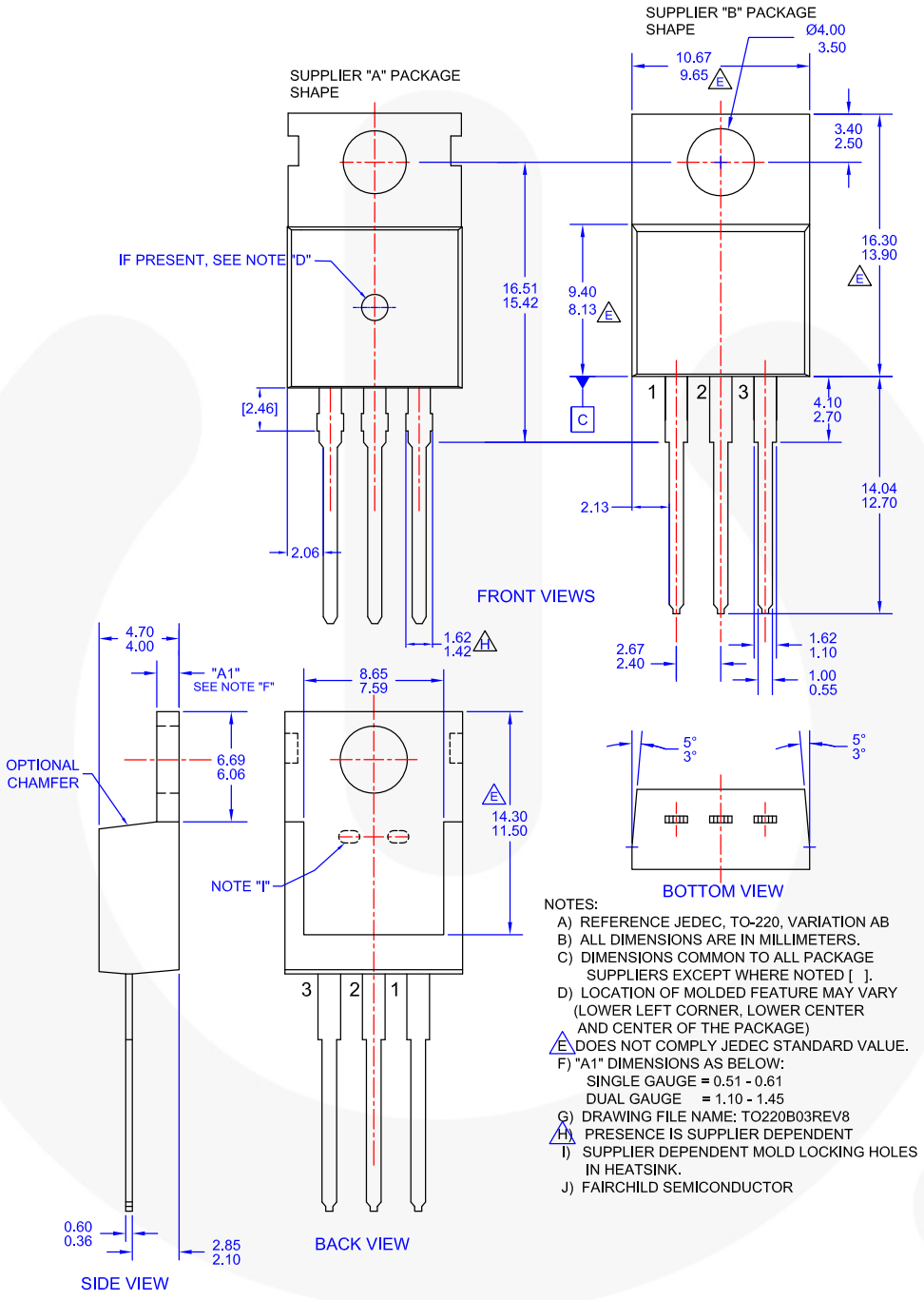
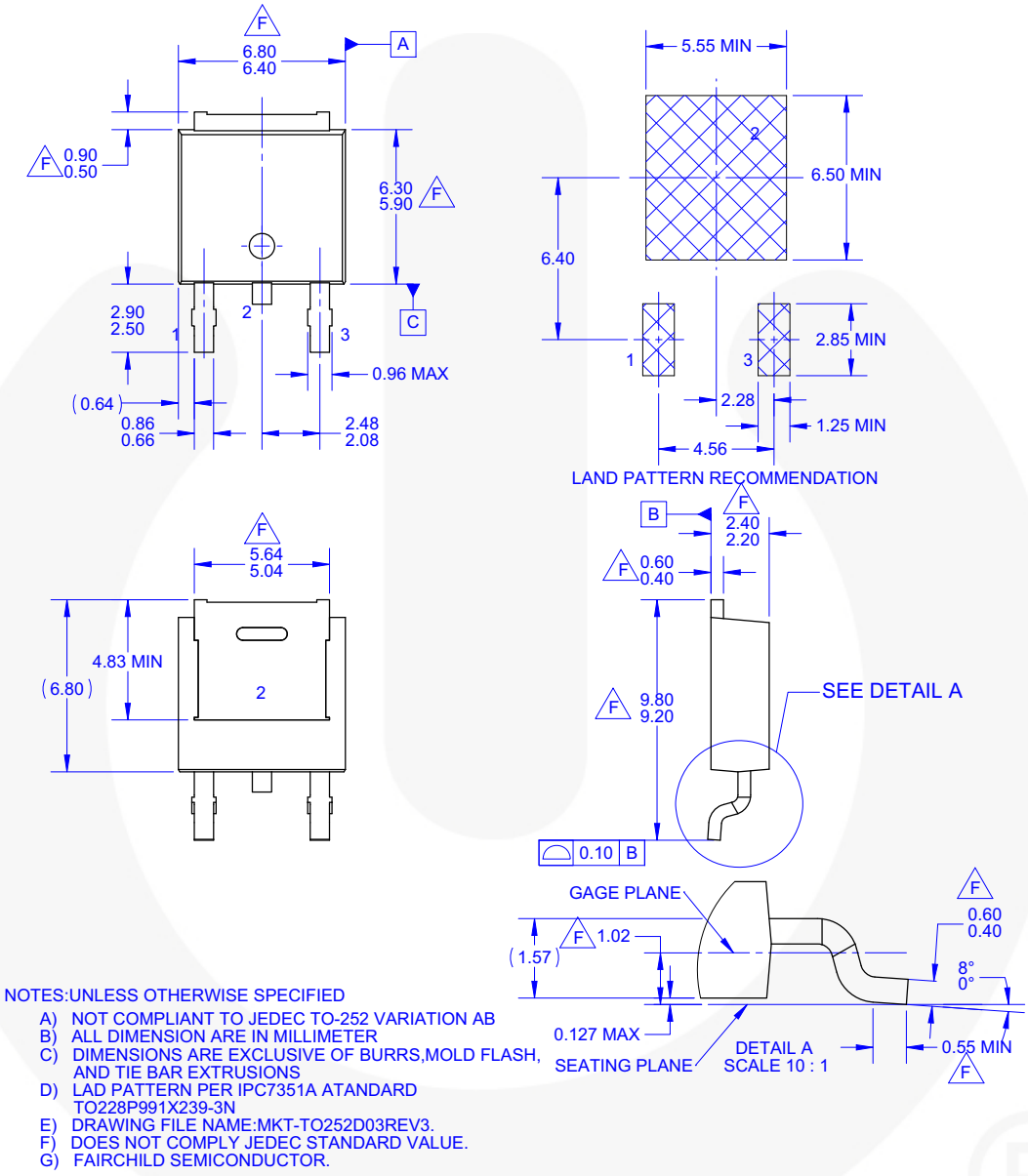


Figure 7. TO-220, MOLDED, 3LEAD, JEDEC VARIATION AB

Physical Dimensions (Continued)



NOTES:UNLESS OTHERWISE SPECIFIED

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B) ALL DIMENSION ARE IN MILLIMETER
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,MOLD FLASH, AND TIE BAR EXTRUSIONS
D) LAD PATTERN PER IPC7351A ATANDARD TO228P991X239-3N
E) DRAWING FILE NAME:MKT-TO252D03REV3.
F) DOES NOT COMPLY JEDEC STANDARD VALUE.
G) FAIRCHILD SEMICONDUCTOR.

Figure 8. 3-LEAD, TO-252, JEDEC TO-252 VAR. AB, SURFACE MOUNT (DPAK)

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