

June 2015

### FQB5N60CTM\_WS

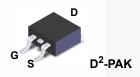
# N-Channel QFET<sup>®</sup> MOSFET 600 V, 4.5 A, 2.5 $\Omega$

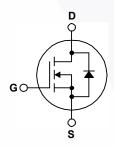
### **Features**

- 4.5 A, 600 V,  $R_{DS(on)}$  = 2.5  $\Omega$  (Max.)  $@V_{GS}$  = 10 V,  $I_D$  = 2.1 A
- Low Gate Charge (Typ. 15 nC)
- Low Crss (Typ. 6.5 pF)
- · 100% Avalanche Tested

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.





### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQB5N60CTM_WS	Unit
V <sub>DSS</sub>	Drain-Source Voltage		600	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		4.5	Α
	- Continuous (T <sub>C</sub> = 100°C)		2.6	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	18	Α
$V_{GSS}$	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	210	mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	4.5	Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	10	mJ
dv/dt	Peak Diode Recovery dv/dt (N		4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)		100	W
' D	- Derate Above 25°C		0.8	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

### **Thermal Characteristics**

Symbol	Parameter	FQB5N60CTM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.25	
D	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

### **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB5N60CTM_WS	FQB5N60CS	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units

### $\textbf{Electrical Characteristics} \quad \textbf{T}_{C} = 25^{\circ} \text{C unless otherwise noted}.$

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	600			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.6		V/°C
1	Zara Cata Valtaga Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.25 A		2.0	2.5	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 2.25 A		4.7		S
<b>Dynam</b> i C <sub>iss</sub>	ic Characteristics Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		515	670	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		55	72	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			6.5	8.5	pF
Switchi	ng Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 4.5 A,		10	30	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V, } R_{G} = 25 \Omega$		42	90	ns
$t_{d(off)}$	Turn-Off Delay Time	VGS 10 V, NG 20 32		38	85	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		46	100	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 4.5 A,	/	15	19	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		2.5		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		6.6		nC
Drain-S	ource Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				4.5	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F	Forward Current			18	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.5 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 4.5 A,		300		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		2.2		μC

#### NOTES:

 $<sup>{\</sup>bf 1.} \ {\bf Repetitive} \ {\bf rating: pulse \ width \ limited \ by \ maximum \ junction \ temperature.}$ 

<sup>2.</sup> L = 18.9 mH,  $I_{AS}$  = 4.5 A,  $V_{DD}$  = 50V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C.

 $<sup>3.~</sup>I_{SD} \leq 4.5~A,~di/dt \leq 200~A/\mu s,~V_{DD} \leq BV_{DSS,}~starting~~T_J = 25^{\circ}C.$ 

<sup>4.</sup> Essentially independent of operating temperature.

### **Typical Characteristics**

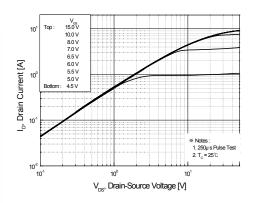


Figure 1. On-Region Characteristics

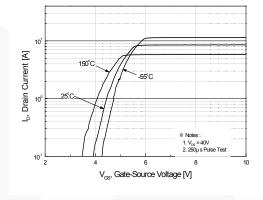


Figure 2. Transfer Characteristics

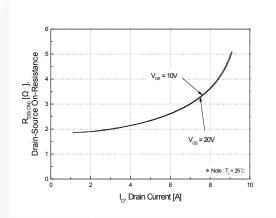


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

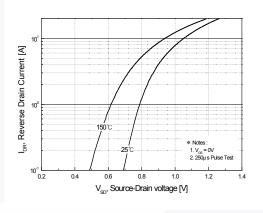


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

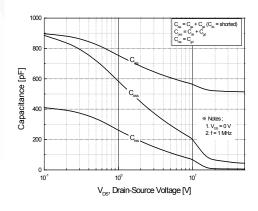


Figure 5. Capacitance Characteristics

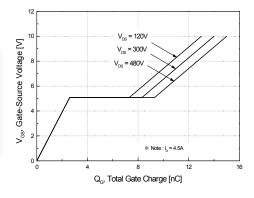


Figure 6. Gate Charge Characteristics

### Typical Characteristics (Continued)

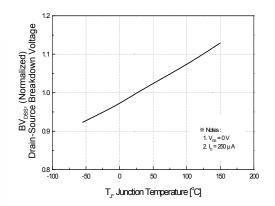
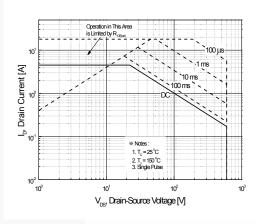


Figure 7. Breakdown Voltage Variation vs Temperature





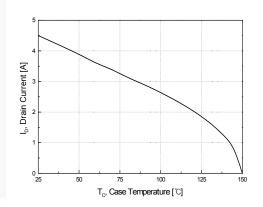


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs Case Temperature

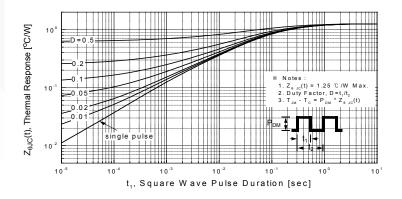


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

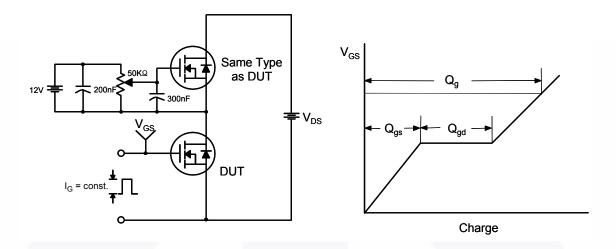


Figure 13. Resistive Switching Test Circuit & Waveforms

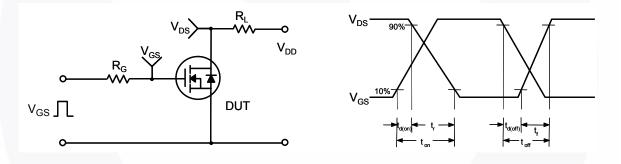
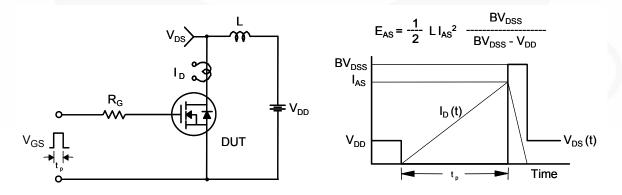


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



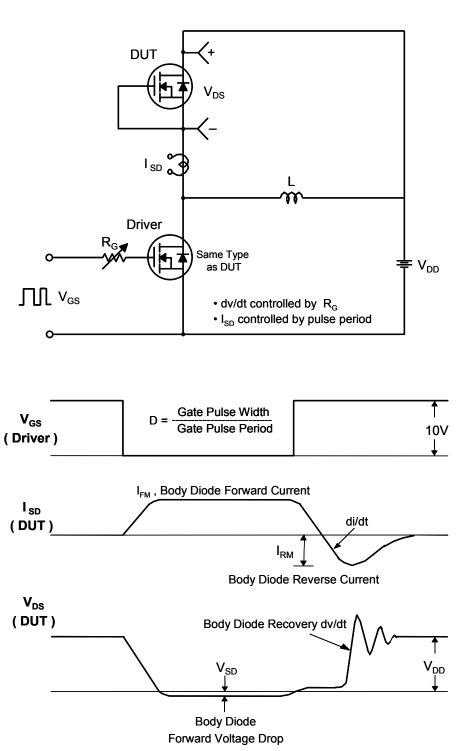
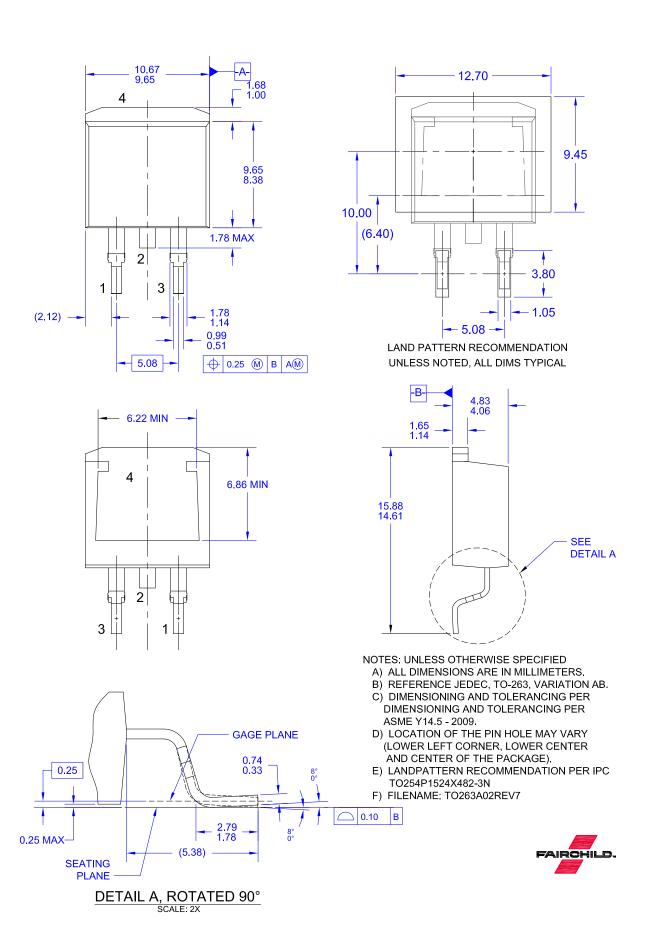


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms







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