USB3803C

USB 2.0 High-Speed Hub Controller Optimized for Portable Applications

Features

- Integrated USB 2.0 Compatible 3-Port Hub.
- Advanced power saving features
  - 1 µA Typical Standby Current
  - Port goes into power saving state when no devices are connected downstream
  - Port is shutdown when port is disabled.
  - Digital core shut down in Bypass and Standby Mode
- Provides USB Battery Charger Detection for:
  - USB-IF Battery Charging 1.1 compliant Dedicated Charging Ports (DCP)
  - USB-IF Battery Charging 1.1 compliant Charging Downstream Port (CDP)
  - Standard Downstream Port (SDP); ie. USB host or downstream hub port
  - Downstream Hub Ports Support USB-IF Battery Charging 1.1 as Charging Downstream Port (CDP)
- Supports either Single-TT or Multi-TT configurations for Full-Speed and Low-Speed connections (when connected to a High-Speed host).
- Bypass Switch for low power single port operation
  - Battery charging detection using a PMIC
  - Stereo and mono/mic audio
  - USB1.1 Data
- Enhanced configuration options available through serial I2C Slave Port
  - VID/PID/DID
  - String Descriptors
  - Configuration options for Hub.
- Internal Default configuration option when serial I2C host not available.
- MultiTRAK™
  - Dedicated Transaction Translator per port.
- PortMap
  - Configurable port mapping and disable sequencing.
- PortSwap
  - Configurable differential intra-pair signal swapping.
- PHYBoost™
  - Programmable USB transceiver drive strength for recovering signal integrity
- VariSense™
  - Programmable USB receiver sensitivity
- flexPWR® Technology
  - Low current design ideal for battery powered applications
  - Internal supply switching provides low power modes
- External 12, 19.2, 26, or 38.4MHz clock input
- Internal 3.3V & 1.2V Voltage Regulators for single supply operation.
  - External VBAT and 1.8V dual supply input option
- Internal Short Circuit protection of USB differential signal pins.
- USB Port ESD Protection (**DP**/**DM**)
  - ±15kV (air discharge)
  - ±8kV (contact discharge)
  - IEC 61000-4-2 level 4 ESD protection without external devices
- 25-pin WLCS (1.95mm x 1.95mm Wafer Level Chip Scale) Package - 0.4mm ball pitch

Target Applications

The USB3803 is targeted for applications where more than one USB port is required. As mobile devices add more features and the systems become more complex it is necessary to have more than one USB port to take communicate with the internal and peripheral devices.

- Mobile Phones
- Ultra Mobile PCs
- Tablet Computers
- Digital Still Cameras
- Digital Video Camcorders
- Gaming Consoles
- PDAs
- Portable Media Players
- GPS Personal Navigation Devices
- Media Players/Viewers

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1.0 GENERAL DESCRIPTION

The USB3803 is a low-power, USB 2.0 hub controller with three downstream ports. The USB3803 can attach to an upstream port as a full-speed hub or as a full-/hi-speed hub and supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

The USB3803 has been specifically optimized for mobile embedded applications. The pin-count has been reduced by optimizing the USB3803 for mobile battery-powered embedded systems where power consumption, small package size, minimal BOM, and battery charger detection capabilities are critical design requirements. Standby mode and Bypass mode power has been minimized. Instead of a dedicated crystal, reference clock inputs are aligned to mobile applications. Flexible integrated power regulators ease integration into battery powered devices. Automatic battery charger detection is available on the upstream port. All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins.

The integrated USB switch allows USB3803 to bypass the USB Hub and directly connect the upstream and Port 3 downstream USB port for operational modes that do not require Hi-Speed media transfers. The bypass switch enables multiple connectivity options to the USB port while preserving the high speed signal quality in USB Hub Mode.

The USB3803 integrated battery charger detection circuitry supports USB-IF 1.1 charger detection methods. These circuits are used to detect the attachment and type of a USB Charger and provide an interrupt output to the portable device indicating that charger information is available to be read from USB3803 status registers via the serial interface.

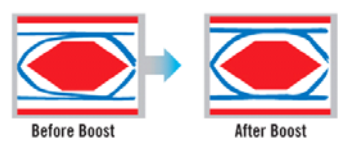
The USB3803 includes programmable features such as:

MultiTRAK™ Technology which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB3803 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB3803 hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost which provides programmable levels of Hi-Speed USB signal drive strength in the upstream and downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration.



VariSense which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

1.1 Customer Selectable Features

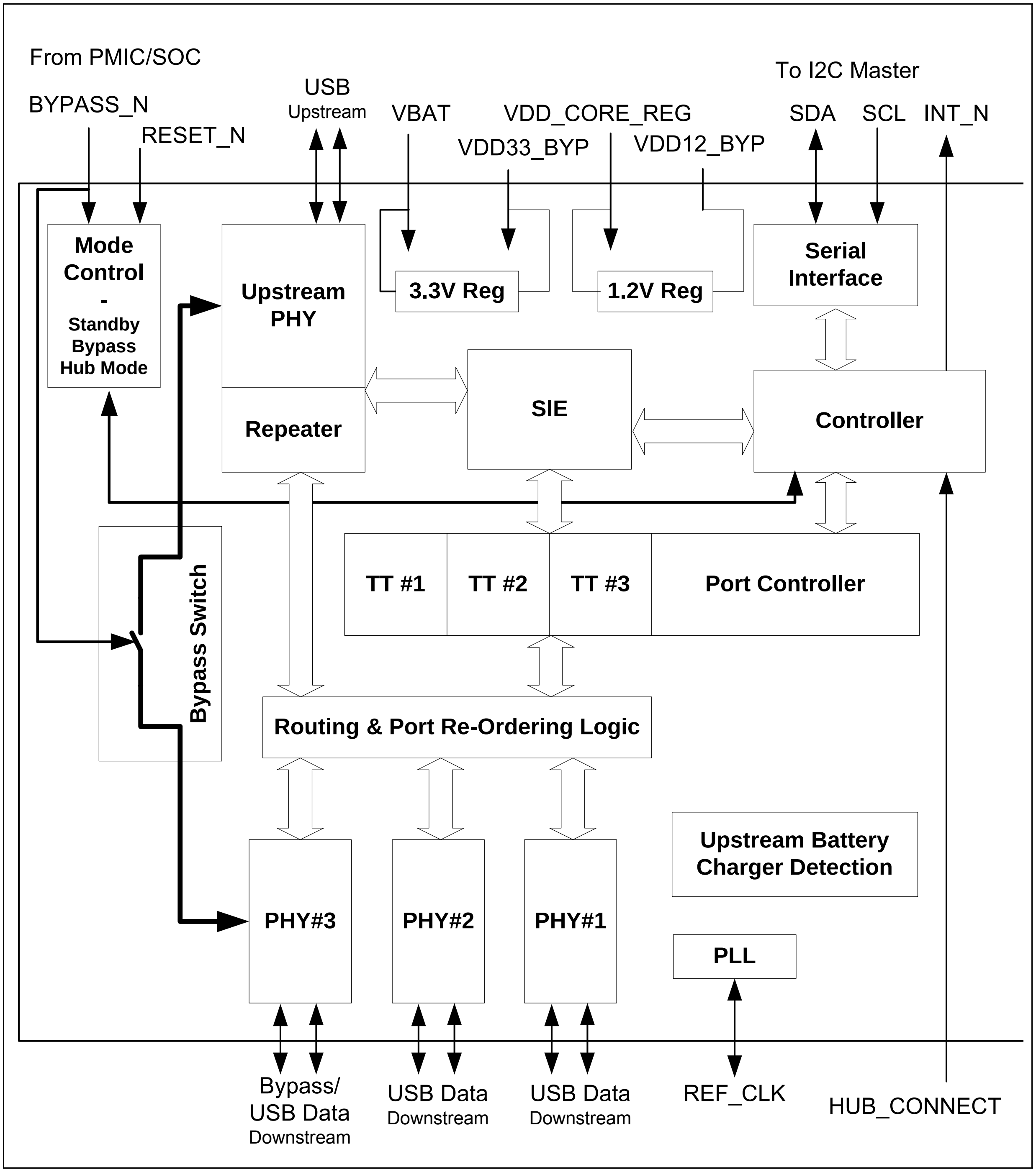
A default configuration is available in the USB3803 following a reset. This configuration may be sufficient for most applications. The USB3803 hub may also be configured by an external microcontroller. When using the microcontroller interface, the hub appears as an I^2C slave device.

The USB3803 hub supports customer selectable features including:

- Optional customer configuration via I^2C.
- Supports compound devices on a port-by-port basis.
- Customizable vendor ID, product ID, and device ID.
- Configurable downstream port power-on time reported to the host.
- Supports indication of the maximum current that the hub consumes from the USB upstream port.
- Supports Indication of the maximum current required for the hub controller.
- Configurable as a Self-Powered and Bus-Powered Hub
- Supports custom string descriptors (up to 30 characters):
  - Product string
  - Manufacturer string
  - Serial number string
- When available, I^2C configurable options for default configuration may include:
  - Downstream ports as non-removable ports
  - Downstream ports as disabled ports
  - USB signal drive strength
  - USB receiver sensitivity
  - USB differential pair pin location

1.1.1 BLOCK DIAGRAM

FIGURE 1-1: USB3803 BLOCK DIAGRAM



2.0 ACRONYMS AND DEFINITIONS

2.1 Acronyms

EP: Endpoint

FS: Full-Speed

HS: Hi-Speed

I^2C®: Inter-Integrated Circuit[1]

LS: Low-Speed

2.2 Reference Documents

1. USB Engineering Change Notice dated December 29th, 2004, *UNICODE UTF-16LE For String Descriptors*.
2. *Universal Serial Bus Specification*, Revision 2.0, Dated April 27th, 2000.
3. *Battery Charging Specification*, Revision 1.1, Release Candidate 10, Dated Sept. 22, 2008
4. *High-Speed Inter-Chip USB Electrical Specification*, Version 1.0, Dated Sept. 23, 2007

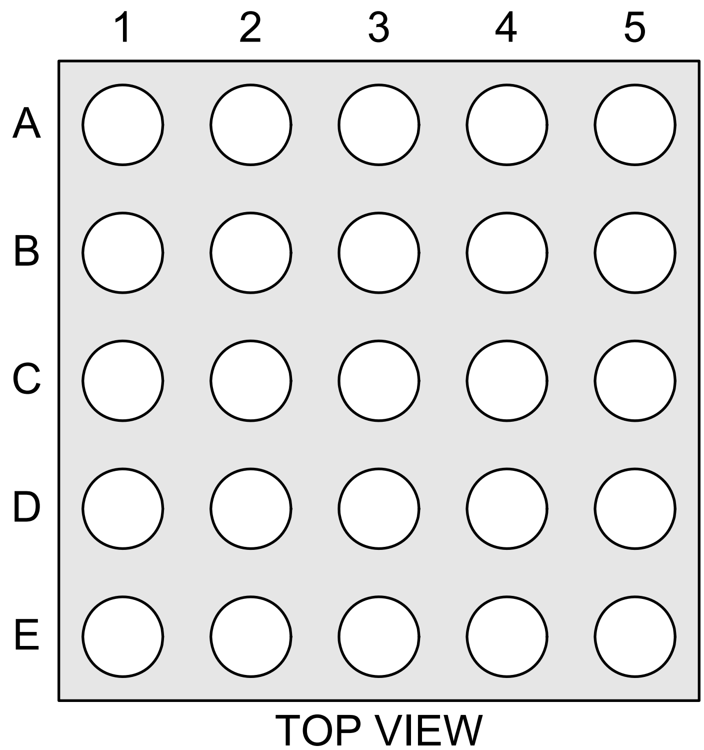
1. I^2C is a registered trademark of Philips Corporation.

3.0 USB3803 PIN DEFINITIONS

3.1 Pin Configuration

The illustration below shows the package diagram.

FIGURE 3-1: USB3803 25-BALL PACKAGE



3.2 Signal Definitions

WLCSP Pin	Name	Description
E2	USBUP_DP	Upstream D+ data pin of the USB Interface
E1	USBUP_DM	Upstream D- data pin of the USB Interface
A5	BYPASS_N	Control signal to select between HUB MODE and BYPASS MODE
C4	I2C_ASEL0	I^2C Address Select Bit 0
B4	I2C_ASEL1	I^2C Address Select Bit 1
A1	USBDN1_DP	USB downstream Port 1 D+ data pin
B1	USBDN1_DM	USB downstream Port 1 D- data pin
C2	USBDN2_DP	USB downstream Port 2 D+ data pin

WLCSP Pin	Name	Description
D2	USBDN2_DM	USB downstream Port 2 D- data pin
C1	USBDN3_DP	USB downstream Port 3 D+ data pin
D1	USBDN3_DM	USB downstream Port 3 D- data pin
E5	SCL	I^2C clock input
D5	SDA	I^2C bi-directional data pin
E3	RESET_N	Active low reset signal
B5	HUB_CONNECT	Hub Connect
C5	INT_N	Active low interrupt signal
D4	REF_SEL1	Reference Clock Select 1 input
E4	REF_SEL0	Reference Clock Select 0 input
B3	REFCLK	Reference Clock input
A4	RBIAS	Bias Resistor pin
D3	VDD12_BYP	1.2 V Regulator
A2	VDD33_BYP	3.3 V Regulator
B2	VBAT	Voltage input from the battery supply
A3	VDD_CORE_REG	Power supply input to 1.2V regulator for digital logic core
C3	VSS	Ground

3.3 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The terms assertion and negation are used. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term “assert”, or “assertion” indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term “negate”, or “negation” indicates that a signal is inactive.

3.3.1 PIN DEFINITION

TABLE 3-1: PIN DESCRIPTIONS

Name	Symbol	Type	Description
Upstream USB 2.0 / Bypass Interface			
USB Bus Data	USBUP_DP USBUP_DM	A-I/O	These pins connect to the upstream USB bus data signals (Host port, or upstream hub)

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Type	Description
Bypass Select for Analog Switch	BYPASS_N	I	Control signal to select between Hub Mode and Bypass Mode. When asserted low, the device transitions to Bypass Mode, connects the Bypass Port to the upstream USB Port, places Port 1 and Port 2 in high impedance state, and places the core logic in a reduced power state. When negated high, the device transitions to HUB MODE and enables operation as a USB hub.
Downstream USB 2.0 / Bypass Interface			
High-Speed USB Data & Port Disable Strap Option	USBDN_DP[2:1] & USBDN_DM[2:1]	A-I/O	These pins connect to the downstream USB peripheral devices attached to the hub's ports
			Downstream Port Disable Strap option: This pin will be sampled at RESET_N negation to determine if the port is disabled. Both USB data pins for the corresponding port must be tied to VDD33_BYP to disable the associated downstream port.
HS USB Data & Bypass Port	USBDN_DP[3] & USBDN_DM[3]	A-I/O	When BYPASS_N is negated high, these pins connect to the downstream USB peripheral devices attached to the hub's ports.
			There is no downstream Port Disable Strap option on these ports. When BYPASS_N is asserted low, USBDN_DP[3] and USBDN_DM[3] respectively are connected through the analog switch to the upstream port USBUP_DP and USBUP_DM. PortSwap setting has no effect in Bypass Mode.
Serial Port Interface			
Serial Data	SDA	I/OD	I^2C Serial Data
Serial Clock	SCL	I	Serial Clock (SCL)

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Type	Description
Interrupt	INT_N	OD	Interrupt The function of this pin is determined by the setting in the CFGP.INTSUSP configuration register. When CFGP.INTSUSP = 0 (General Interrupt) A transition from high to low identifies when one of the interrupt enabled status registers has been updated. SOC must update the Serial Port Interrupt Status Register to reset the interrupt pin high. When CFGP.INTSUSP = 1 (Suspend Interrupt) Indicates USB state of the hub. ‘Asserted’ low = Unconfigured or configured and in USB Suspend ‘Negated’ high = Hub is configured, and is active (i.e., not in suspend) The Suspend Interrupt can be used by the system to determine whether the full current based on the USB descriptor can be drawn on VBUS or whether a reduced current should be drawn in accordance with the USB specification for unconfigured or suspend mode. If unused, this pin must be tied to **VDD33_BYP**.
Serial Address Select	I2C_ASEL[1:0]	I	Address Select – the USB3803 has the ability to be programmed with four different I^2C slave addresses as part of the configuration in order to provide flexibility. When sharing the serial bus in the system with another part that conflicts with one of the address settings, these pins may be used to change the selection to a non-conflicting I^2C address. The customer should tie these pins to ground or VDD33_BYP. This input is latched during HUB.Init stage. I2C_ASEL[1] selects between the I2C addresses defined in registers I2CADD0 and I2CADD1. I2C_ASEL[0] determines the LSB of the I2C address.
Misc			
Reference Clock Input	REFCLK	I	Reference clock input.
Reference Clock Select	REF_SEL[1:0]	I	The reference select input must be set to correspond to the frequency applied to the REFCLK input. The customer should tie these pins to ground or VDD33_BYP. This input is latched during HUB.Init stage. Selects input reference clock frequency per Table 3-3.
RESET Input	RESET_N	I	This active low signal is used by the system to reset the chip and hold the chip in low power STANDBY MODE.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Type	Description
USB Transceiver Bias	RBIAS	A-I/O	A 12.0kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
Hub Connect	HUB_CONNECT	I	Hub will transition to the Hub Communication Stage when this pin is asserted high. It can be used in three different ways: Tied to Ground - Hub will not transition to the Hub Communication Stage until connect_n bit of the SP_ILOCK register is negated. Tied to **VDD33_BYP** - Hub will automatically transition to the Hub Communication Stage regardless of the setting of the connect_n bit and without pausing for the SOC to reference status registers. Transition from low to high - Hub will transition to the Hub Communication Stage after this pin transitions from low to high. HUB_CONNECT should never be driven high when USB3803 is in Standby Mode.
Power			
1.2V VDD Power	VDD12_BYP	Power	1.2 V Regulator. A 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the USB3803.
3.3V VDD Power	VDD33_BYP	Power	3.3V Regulator. A 4.7µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the USB3803.
Core Power Supply Input	VDD_CORE_REG	Power	Power supply to 1.2V regulator. This power pin should be connected to VDD33_BYP for single supply applications. Refer to Section 9.0, Integrated Power Regulators for power supply configuration options.
Battery Power Supply Input	VBAT	Power	Battery power supply. Refer to Section 9.0 for power supply configuration options.
VSS	VSS	Ground	Ground

3.3.2 I/O TYPE DESCRIPTIONS

TABLE 3-2: USB3803 I/O TYPE DESCRIPTIONS

I/O Type	Description
I	Digital Input
OD	Digital Output. Open Drain.
I/O	Digital Input or Output.
A-I/O	Analog Input or Output.
Power	DC input or Output.
Ground	Ground.

3.3.3 REFERENCE CLOCK

The REFCLK input is can be driven with a square wave from 0 V to VDD33_BYP. The USB3803 only uses the positive edge of the clock. The duty cycle is not critical.

The USB3803 is tolerant to jitter on the reference clock. The REFCLK jitter should be limited to a peak to peak jitter of less than 1 nS over a 10 µS time interval. If this level of jitter is exceeded the USB3803 high speed eye diagram may be degraded.

To select the REFCLK input frequency, the REF_SEL pins must be set according to Table 3-3.

TABLE 3-3: USB3803 REFERENCE CLOCK FREQUENCIES

REF_SEL[1:0]	Frequency (MHz)
‘00’	38.4
‘01’	26.0
‘10’	19.2
‘11’	12.0

3.3.4 INTERRUPT

The general interrupt pin (INT_N) is intended to communicate a condition change within the hub. The conditions which may cause an interrupt are captured within a register mapped to the serial port (Register E8h: Serial Port Interrupt Status - INT_STATUS.) The conditions which cause the interrupt to assert can be controlled through use of an interrupt mask register (Register E9h: Serial Port Interrupt Mask - INT_MASK.)

The general interrupt and all interrupt conditions are functionally latched and event driven. Once the interrupt or any of the conditions have asserted, the status bit will remain asserted until the SOC negates the bit using the serial port. The bits will then remain negated until a new event condition occurs. The latching nature of the register causes the status to remain even if the condition that caused the interrupt ceases to be active. The event driven nature of the register causes the interrupt to only occur when a new event occurs- when a condition is removed and then is applied again. (e.g. if the battery charger detection routine has completed and the SOC negates the interrupt status, it will not cause an interrupt just because the charger detection is still completed- a new charger detection routine has to run before its associated interrupt will assert again.)

The function of the interrupt and the associated status and masking registers are illustrated in Figure 3-2, "INT_N Operation". Registers & Register bits shown in the figure are defined in Table 5-2, “Serial Interface Registers,” on page 20 and Section 5.3, "Serial Interface Register Definitions," on page 30.

FIGURE 3-2: INT_N OPERATION

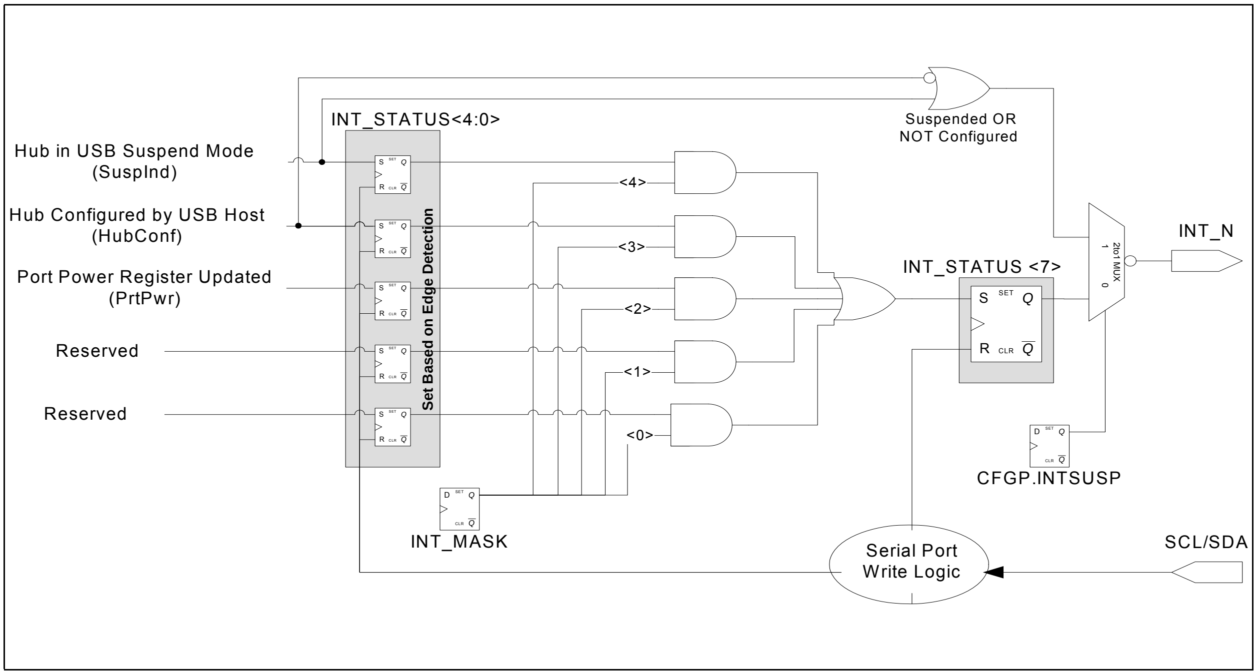


Figure 3-2 also shows an alternate configuration option (CFGP.INTSUSP) for a suspend interrupt. This option allows the user to change the behavior of the INT_N pin to become a direct level indication of configuration and suspend status.

When selected, the INT_N indicates that the entire hub has entered the USB suspend state and that VBUS current consumption should be reduced in accordance with the USB specification. Selective suspend set by the host on downstream hub ports have no effect on this signal because there is no requirement to reduce current consumption from the upstream VBUS. It can be used by the system to monitor INT_N to dynamically adjust how much current the PMIC draws from VBUS to charge the battery in the system during a USB session. Because it is a level indication, it will assert or negate to reflect the current status of suspend without any interaction through the serial port.

When negated high this means no level suspend interrupt and device has been configured by the USB Host. The full configured current can be drawn from the USB VBUS pin on the USB connector for charging - up to 500mA depending on descriptor setting. When asserted low, this indicates a suspend interrupt or device not yet configured by USB Host. The current draw can be limited by the system according to the USB specification. The USB specification limits current to 100mA before configuration, and up to 12.5mA in USB suspend mode.

Note:	Because INT_N is driven low when active, care must be taken when selecting the external pullup resistor value for this open drain output. A sufficiently large resistor must be selected to insure suspend current requirements can be satisfied for the system.

4.0 MODES OF OPERATION

The USB3803 has modes of operation - Standby Mode, Bypass Mode and Hub Mode which balance power consumption with functionality. The operating mode of the USB3803 is selected by setting values on primary inputs according to the table below.

TABLE 4-1: CONTROLLING MODES OF OPERATION

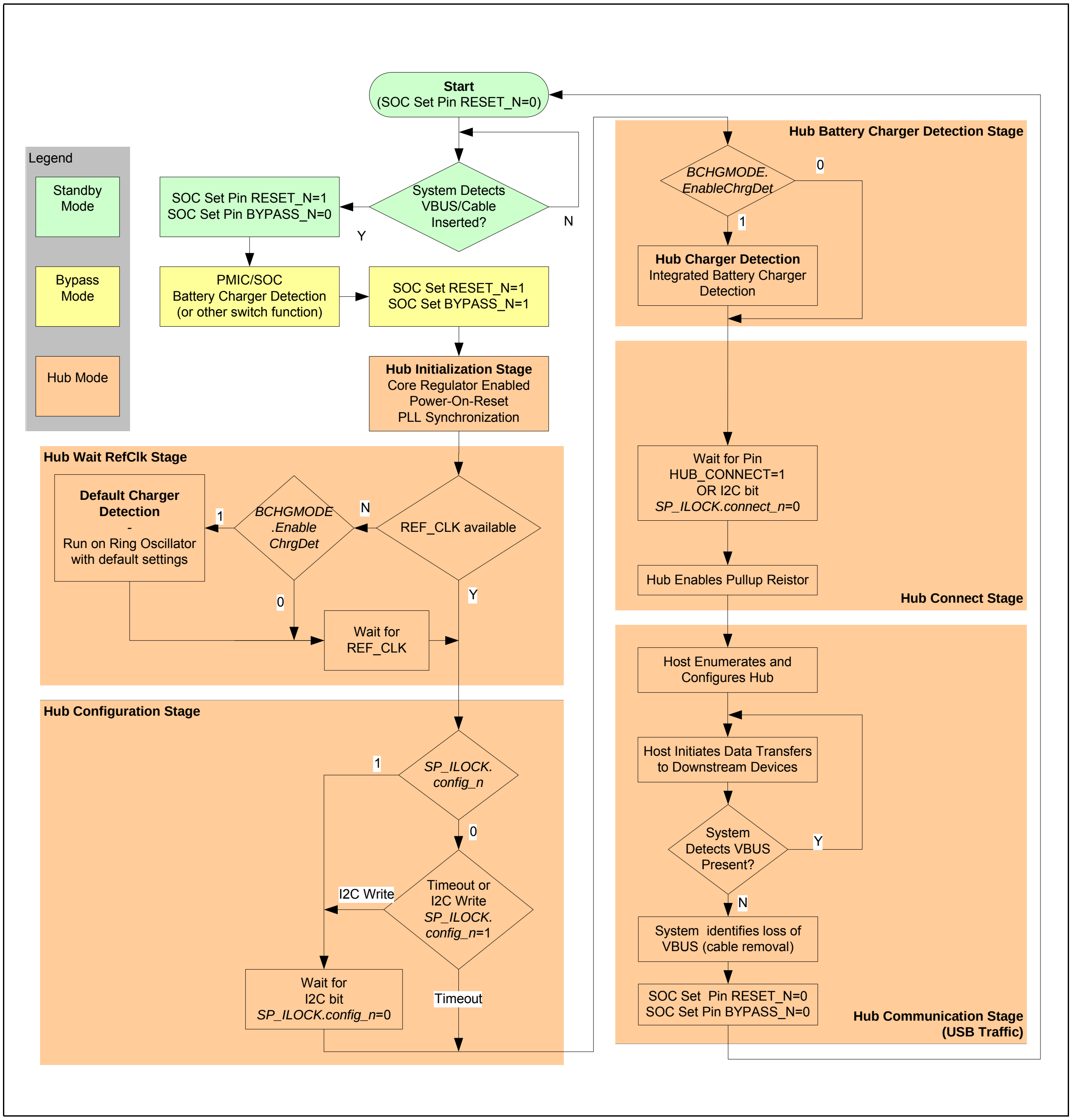
RESET_N input	BYPASS_N Input	Resulting Mode	Summary
0	0	Standby	Lowest Power Mode – no function other than monitoring RESET_N and BYPASS_N inputs to move to higher states. Switch Resistance is R_{STDBY}. All regulators are powered off.
1	0	Bypass	Low Power Mode - Bypass Switch connects bypass port (downstream port 3) to upstream port with low switch resistance R_{ON}.
1	1	Hub	Full Feature Mode - Operates as a configurable USB hub with battery charger detection. Switch is disabled and assumes high switch resistance R_{OFF}. Power consumption based on how many ports are active, at what speeds they are running and amount of data transferred (refer to Table 10-3 and Table 10-4).

4.1 Operational Mode Flowchart

The flowchart in Figure 4-1 shows the modes of operation. It also shows how the USB3803 traverses through the Hub mode stages (shown in bold.) The flow of control is dictated by control register bits shown in Italics as well as other events such as availability of reference clock. Refer to Section 5.3, "Serial Interface Register Definitions," on page 30 for the detailed definition of the control register bits. In this specification register bits are referenced using the syntax <Register>.<RegisterBit>. A summary of all registers can be found in Table 5-2, “Serial Interface Registers,” on page 20.

The remaining sections in this chapter provide more detail on each stage and mode of operation.

FIGURE 4-1: MODES OF OPERATION FLOWCHART



4.2 Standby Mode

Standby Mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all internal regulators are powered off, the bypass switch resistance is unconstrained, the PLL is not running, and core logic is powered down in order to reduce power. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after RESET_N is negated high.

4.2.1 EXTERNAL HARDWARE RESET_N

A valid hardware reset is defined as an assertion of RESET_N low for a minimum of 100us after all power supplies are within operating range. While reset is asserted, the Hub (and its associated external circuitry) enters STANDBY MODE and consumes extremely lowcurrent as defined in Table 10-3 and Table 10-4.

Assertion of RESET_N (external pin) causes the following:

- All downstream ports are disabled.
- The switch assumes resistance R_{STDBY}.
- All transactions immediately terminate; no states are saved.
- All internal registers return to the default state.
- The PLL is halted.

After RESET_N is negated high in the Hub.Init stage, the Hub reads customer-specific data from the ROM.

4.3 Bypass Mode

Bypass Mode combines low power operation with the function of an integrated bypass switch. This mode allows a bypass port (Downstream Port 3) to be electrically connected to the upstream port through use of a pass gate as illustrated in Figure 1-1. Compliant full speed USB signals may be successfully passed through the switch.

There are several applications for this mode. The bypass port can be used to provide connectivity to a PMIC to implement battery charger detection. In this configuration any special signaling is replicated on the line as if the hub were not in series. Another application is for a downstream device on Port 3 to assume a full speed host role for an application such as USB OTG or embedded usb host. It can also be used to provide audio signaling (must be offset to avoid negative signal swing.)

To insure that Bypass mode entered, RESET_N must be asserted and then de-asserted prior to asserting BYPASS_N (refer to Table 4-1). In Bypass Mode the 1.2V regulator is powered off, PLL is not running and core logic is powered down in order to reduce power. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized when BYPASS_N is negated to a high value.

4.3.1 VOLTAGE RANGE

The switch shall operate in a voltage range as specified by V_{switch} in Table 10-9, “Analog Switch Characteristics,” on page 84. Negative voltage swing is not supported.

4.3.2 SWITCH BANDWIDTH

The switch shall support compliant operation with an external full speed USB Port and with external battery charger detection. Under certain conditions with short cables it may be possible to pass high speed USB signals. However, due to physical design constraints, the switch is not necessarily intended to pass a fully compliant high speed USB eye.

4.4 Hub Mode

Hub Mode provides functions of configuration, upstream battery charger detection, and high speed USB hub operation including connection and communication. Upon entering Hub Mode and initializing internal logic, the device passes through several sequential stages based on a fixed time interval. In Hub Mode the bypass switch is disabled.

Note:	In order to adhere to the USB 2.0 Specification the system must not consume more than 100mA from the upstream VBUS until the Hub is configured by the host.

4.4.1 HUB INITIALIZATION STAGE (HUB.INIT)

The first stage is the initialization stage and occurs when Hub mode is entered based on the conditions in Table 4-1. In this stage the 1.2V regulator is enabled and stabilizes, internal logic is reset, and the PLL locks if a valid REFCLK is supplied. Configuration registers are initialized to their default state and I2C_ASEL[1:0] and REF_SEL[1:0] input values are latched. The USB3803 will complete initialization and automatically enter the next stage after $T_{hubinit}$. Because the digital logic within the device is not yet stable, no communication with the device using the serial port is possible. Configuration registers are initialzed to their default state.

4.4.2 HUB WAIT REFCLK STAGE (HUB.WAITREF)

In this stage the reference clock is checked for activity. If the reference clock is active the part will continue to the Hub configuration stage. If the reference clock is not active but the default ROM has enabled battery charger detection, the detection sequence will begin while operating on an internal ring oscillator.

If the PLL locks while battery charger detection is still in progress, the sequence will be aborted until the battery charger detection stage is complete. If aborted, no results are captured. If battery charger detection completes, the results of the battery charger detection may be communicated through the INT_N pin.

During this stage the serial port is not functional.

If the reference clock is provided before entering hub mode, the USB3803 will transition to the Hub Configuration stage without pausing in the Hub Wait RefClk stage. Otherwise, the USB3803 will transition to the Hub configuration stage once a valid reference clock is supplied and the PLL has locked.

4.4.3 HUB CONFIGURATION STAGE (HUB.CONFIG)

The next stage is the configuration stage. In this stage, the SOC has an opportunity to control the configuration of the USB3803 and modify any of the default configuration settings specified in the integrated ROM such as USB device descriptors, or port electrical settings such as PHY BOOST, and control features such as battery charging detection. The SOC implements the changes using the serial slave port interface to write configuration & control registers.

See Section 5.3.30, "Register E7h: Serial Port Interlock Control - SP_ILOCK," on page 40 for definition of SP_ILOCK register and how it controls progress through hub stages. If the SP_ILOCK.config_n bit has its default asserted low and the bit is not written by the serial port, then the USB3803 completes configuration and automatically enters the Battery Charger Detection Stage after $T_{hubconfig}$ without any I2C intervention.

If the SP_ILOCK.config_n bit has its default negated high or the SOC negates the bit high using the serial port during $T_{hubconfig}$, the USB3803 will remain in the Hub Configuration Stage indefinitely. This will allow the SOC to update other configuration and control registers without any remaining time-out restrictions. Once the SP_ILOCK.config_n bit is asserted low by the SOC the device will transition to the next stage.

4.4.4 HUB BATTERY CHARGER DETECTION STAGE (HUB.CHGDET)

After configuration, the device enters Battery Charger Detection Stage. If the battery charger detection feature was disabled during the Hub Configuration Stage, the USB3803 will immediately transition to the Hub Connect Stage. If the battery charger detection feature remains enabled, the battery charger detection sequence is started automatically and the USB3803 will transition to the Hub Connect Stage after $T_{hubchgdet}$.

4.4.5 HUB CONNECT STAGE (HUB.CONNECT)

Next, the USB3803 enters the Hub Connect Stage. See Section 5.3.37, "Register EEh: Configure Portable Hub - CFGP," on page 44 and Section 5.3.30, "Register E7h: Serial Port Interlock Control - SP_ILOCK," on page 40 for definition of control registers which affect how the device transitions through the hub stages.

By using the appropriate controls, the USB3803 can be set to immediately transition, or instead to remain in the Hub Connect Stage indefinitely until one of the SOC handshake events occur. When set to wait on the handshake, the SOC may read or update any of the serial port registers. Once the SOC is finished accessing any registers and is ready for USB communication to start, it can perform one of the selected handshakes which will cause the USB3803 to assert its pull-up on the USBUP_DP pin and connect within $T_{hubconnect}$ and transition to the Hub Communication Stage.

4.4.6 HUB COMMUNICATION STAGE (HUB.COM)

Once it exits the Hub Connect Stage, the USB3803 enters Hub Communication Stage. In this stage full USB operation is supported under control of the USB Host on the upstream port. The USB3803 will remain in the Hub Communication Stage until the operating mode is changed by the system asserting RESET_N or BYPASS_N low.

While in the Hub Communication Stage, communication over the serial port is no longer supported and the resulting behavior of the serial port if accessed is undefined. In order to re-enable the serial port interface, the device must exit Hub Communication Stage. Exiting this stage is only possible by entering Standby or Bypass mode.

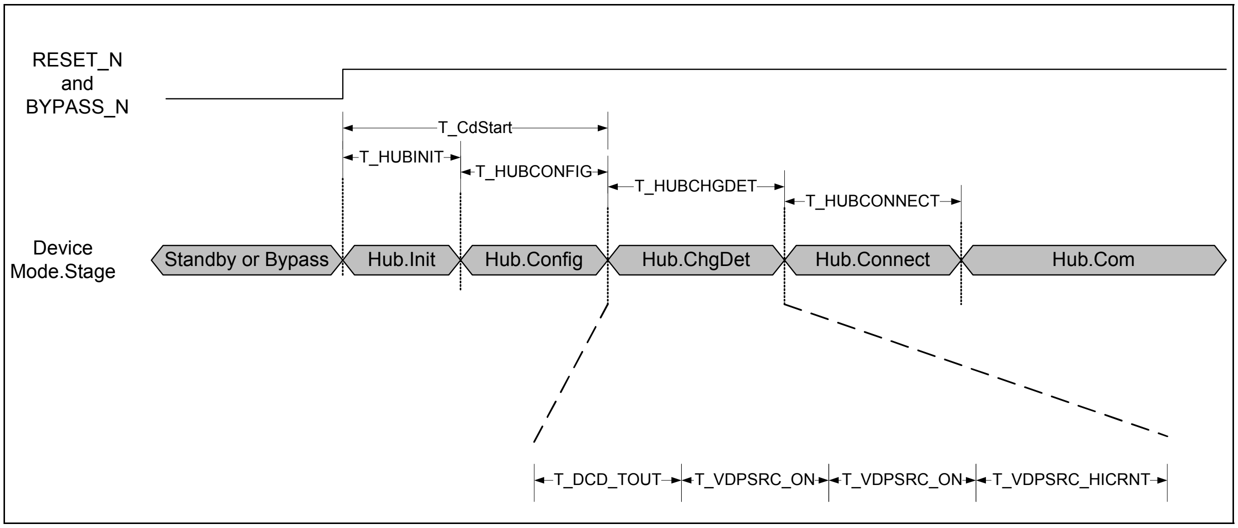
4.4.7 HUB MODE TIMING DIAGRAM

The following timing diagram shows the progression through the stages of Hub Mode and the associated timing parameters.

$T_{CdStart}$ is the amount of time from entering Hub Mode to the end of the Hub Configuration stage and the start of Hub Charger Detection stage. It is not a unique parameter but will equal the sum of the $T_{HUBINIT}$ and $T_{HUBCONFIG}$.

$T_{HUBCHGDET}$ is the amount of time to perform the battery charger detection sequence. It is likewise a sum of several timing parameters defined in Section 8.0, "Battery Charging".

FIGURE 4-2: TIMING DIAGRAM FOR HUB STAGES



The following table lists the timing parameters associated with the stages of the Hub Mode.

TABLE 4-2: TIMING PARAMETERS FOR HUB STAGES

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Hub Initialization Time	$T_{HUBINIT}$		3	4	mS	
Hub Configuration Time-out	$T_{HUBCONFIG}$	399	400	401	mS	
Charger Detection Start Time delay	$T_{CDSTART}$	$T_{HUBINIT}$	$T_{HUBINIT}$ + $T_{HUBCONFIG}$	$T_{HUBINIT}$ + $T_{HUBCONFIG}$	mS	
Hub Charger Detection Duration	$T_{HUBCHGDET}$	T_{DCD_TOUT}	T_{DCD_TOUT} + 2*T_{VDPSRC_ON} + T_{VDPSRC_HICRNT}			See Table 8-2
Data Contact Detect Time-out	T_{DCD_TOUT}		See Table 8-2			
Vdat_src and Idat_sink Enable Time	T_{VDPSRC_ON}		See Table 8-2			
Delay from Vdat_det to end of charger detection sequence	T_{VDPSRC_HICRNT}		See Table 8-2			
Hub Connect Time	$T_{HUBCONNECT}$	0	1	10	uS	

5.0 CONFIGURATION OPTIONS

5.1 Hub Configuration Options

The Hub supports a number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub: by writing to configuration registers using the serial slave port, or by internal default settings. Any configuration registers which are not written by the serial slave retain their default settings.

5.1.1 MULTI/SINGLE TT

The USB 2.0 Hub is fully specification compliant to the Universal Serial Bus Specification Revision 2.0 April 27,2000 (12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub Specification) for general details regarding Hub operation and functionality.

For performance reasons, the Hub provides 1 Transaction Translator (TT) per port (defined as Multi-TT configuration), and each TT has 1512 bytes of periodic buffer space and 272 Bytes of non- periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for each Transaction Translator.

When configured as a Single-TT Hub (required by USB 2.0 Specification), the Single Transaction Translator will have 1512 bytes of periodic buffer space and 272 bytes of non-periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for the entire Transaction Translator. **Each Transaction Translator's buffer is divided as shown in** Table 5-1, "Transaction Translator Buffer Chart".

TABLE 5-1: TRANSACTION TRANSLATOR BUFFER CHART

Periodic Start-Split Descriptors	256 Bytes
Periodic Start-Split Data	752 Bytes
Periodic Complete-Split Descriptors	128 Bytes
Periodic Complete-Split Data	376 Bytes
Non-Periodic Descriptors	16 Bytes
Non-Periodic Data	256 Bytes
Total for each Transaction Translator	1784 Bytes

5.1.2 VBUS DETECT

According to Section 7.2.1 of the USB 2.0 Specification, a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. Depending on input tie-offs and values in the configuration registers, the USB3803 may automatically enable the D+ pull-up resistor once it enters the Hub.Connect stage of Hub Mode (after RESET_N and BYPASS_N are both negated high.) To fully adhere to the USB specification, the system should not cause the part to enter Hub.Com Hub Mode until VBUS has been detected on the upstream port and a connection is desired.

5.2 Default Serial Interface Register Memory Map

The Serial Interface Registers are used to customize the USB3803 for specific applications. Reserved registers or reserved bits within a defined register should not be written to non-default values or undefined behavior may result.

TABLE 5-2: SERIAL INTERFACE REGISTERS

Reg Addr	R/W	Register Name	Abbrevation	Section
00h	R/W	VID LSB	VIDL	5.3.1, page 22
01h	R/W	VID MSB	VIDM	5.3.2, page 23

TABLE 5-2: SERIAL INTERFACE REGISTERS (CONTINUED)

Reg Addr	R/W	Register Name	Abbrevation	Section
02h	R/W	PID LSB	PIDL	5.3.3, page 23
03h	R/W	PID MSB	PIDM	5.3.4, page 23
04h	R/W	DID LSB	DIDL	5.3.5, page 23
05h	R/W	DID MSB	DIDM	5.3.6, page 23
06h	R/W	Config Data Byte 1	CFG1	5.3.7, page 24
07h	R/W	Config Data Byte 2	CFG2	5.3.8, page 25
08h	R/W	Config Data Byte 3	CFG3	5.3.9, page 25
09h	R/W	Non-Removable Devices	NRD	5.3.10, page 26
0Ah	R/W	Port Disable (Self)	PDS	5.3.11, page 26
0Bh	R/W	Port Disable (Bus)	PDB	5.3.12, page 27
0Ch	R/W	Max Power (Self)	MAXPS	5.3.13, page 27
0Dh	R/W	Max Power (Bus)	MAXPB	5.3.14, page 27
0Eh	R/W	Hub Controller Max Current (Self)	HCMCS	5.3.15, page 28
0Fh	R/W	Hub Controller Max Current (Bus)	HCMCB	5.3.16, page 28
10h	R/W	Power-on Time	PWRT	5.3.17, page 28
11h	R/W	LANG_ID_H	LANGIDH	5.3.18, page 28
12h	R/W	LANG_ID_L	LANGIDL	5.3.19, page 29
13h	R/W	MFR_STR_LEN	MFRSL	5.3.20, page 29
14h	R/W	PRD_STR_LEN	PRDSL	5.3.21, page 29
15h	R/W	SER_STR_LEN	SERSL	5.3.22, page 29
16h-53h	R/W	MFR_STR	MANSTR	5.3.23, page 29
54h-91h	R/W	PROD_STR	PRDSTR	5.3.24, page 29
92h-CFh	R/W	SER_STR	SERSTR	5.3.25, page 30
D0h	R/W	Downstream Battery Charging	BC_EN	5.3.26, page 30
D1-E1h	R/W	Reserved	N/A	
E2h	R/W	Upstream Battery Charger Detection	BATT_CHG	5.3.27, page 31
E3-E4h	R/W	Reserved	N/A	
E5h	R	Port Power Status	PRTPWR	5.3.28, page 32

TABLE 5-2: SERIAL INTERFACE REGISTERS (CONTINUED)

Reg Addr	R/W	Register Name	Abbrevation	Section
E6h	R/W	Over Current Sense Control	OCS	5.3.29, page 32
E7h	R/W	Serial Port Interlock Control	SP_ILOCK	5.3.30, page 32
E8h	R/W	Serial Port Interrupt Status	INT_STATUS	5.3.31, page 33
E9h	R/W	Serial Port Interrupt Mask	INT_MASK	5.3.32, page 34
EAh	R	I2C Address 0	I2CADD0	5.3.33, page 34
EBh	R	I2C Address 1	I2CADD1	5.3.34, page 35
ECh	R/W	Battery Charger Mode	BCHGMODE	5.3.35, page 35
EDh	R/W	Charger Detect Mask	CHGDETMASK	5.3.36, page 35
EEh	R/W	Configure Portable Hub	CFGP	5.3.37, page 36
EFh-F3h	R	Reserved	N/A	
F4h	R/W	Varisense_Up3	VSNSUP3	5.3.38, page 36
F5h	R/W	Varisense_21	VSNS21	5.3.39, page 37
F6h	R/W	Boost_Up3	BSTUP3	5.3.40, page 37
F7h	R/W	Reserved	N/A	
F8h	R/W	Boost_21	BST21	5.3.41, page 38
F9h	R/W	Reserved	N/A	
FAh	R/W	Port Swap	PRTSP	5.3.42, page 39
FBh	R/W	Port Remap 12	PRTR12	5.3.43, page 40
FCh	R/W	Port Remap 34	PRTR34	5.3.44, page 41
FDh	R/W	Reserved	N/A	
FEh	R/W	Reserved	N/A	
FFh	R/W	I2C Status/Command	STCD	5.3.45, page 42

5.3 Serial Interface Register Definitions

5.3.1 REGISTER 00H: VENDOR ID (LSB) - VIDL

Default = 0x24h - Corresponds to MCHP Vendor ID.

Bit Number	Bit Name	Description
7:0	VID_LSB	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the customer using the serial interface options.

5.3.2 REGISTER 01H: VENDOR ID (MSB) - VIDM

Default = 0x04h - Corresponds to MCHP Vendor ID.

Bit Number	Bit Name	Description
7:0	VID_MSB	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the customer using serial interface options.

5.3.3 REGISTER 02H: PRODUCT ID (LSB) - PIDL

Default = 0x03h - Corresponds to MCHP USB part number for 3-port device.

Bit Number	Bit Name	Description
7:0	PID_LSB	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by customer). This field is set by the customer using the serial interface options.

5.3.4 REGISTER 03H: PRODUCT ID (MSB) - PIDM

Default = 0x38h Corresponds to MCHP 3803 device.

Bit Number	Bit Name	Description
7:0	PID_MSB	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by customer). This field is set by the customer using the serial interface options.

5.3.5 REGISTER 04H: DEVICE ID (LSB) - DIDL

Default = 0xA1h

Bit Number	Bit Name	Description
7:0	DID_LSB	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by customer). This field is set by the customer using the serial interface options.

5.3.6 REGISTER 05H: DEVICE ID (MSB) - DIDM

Default = 0xB1h

Bit Number	Bit Name	Description
7:0	DID_MSB	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by customer). This field is set by the customer using the serial interface options.

5.3.7 REGISTER 06H: CONFIG_BYTE_1 - CFG1

Default = 0x1Bh - Corresponds to Bus Powered, Individual Port Power

Bit Number	Bit Name	Description
7	SELF_BUS_PWR	Self or Bus Power: Selects between Self- and Bus-Powered operation. The Hub is either Self-Powered (draws less than 2mA of upstream bus power) or Bus-Powered (limited to a 100mA maximum of upstream power prior to being configured by the host controller). When configured as a Bus-Powered device, the Microchip Hub consumes less than 100mA of current prior to being configured. After configuration, the Bus-Powered Microchip Hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100mA per externally available down-stream port) must consume no more than 500mA of upstream VBUS current. The current consumption is system dependent, and the customer must ensure that the USB 2.0 specifications are not violated. When configured as a Self-Powered device, <1mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500mA of current. This field is set by the customer using the serial interface options. 0 = Bus-Powered operation. 1 = Self-Powered operation.
6	Reserved	Reserved
5	HS_DISABLE	High Speed Disable: Disables the capability to attach as either a High/Full-speed device, and forces attachment as Full-speed only i.e. (no High-Speed support). 0 = High-/Full-Speed. 1 = Full-Speed-Only (High-Speed disabled!)
4	MTT_ENABLE	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT) {Note: The host may force Single-TT mode only}. 0 = single TT for all ports. 1 = one TT per port (multiple TT's supported)
3	EOP_DISABLE	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the Hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a Host controller (operating in FS mode) from placing the USB bus in suspend. 0 = An EOP is generated at the EOF1 point if no traffic is detected. 1 = EOP generation at EOF1 is disabled (note: this is normal USB operation). **Note:** This is a rarely used feature in the PC environment, existing drivers may not have been thoroughly debugged with this feature enabled. It is included because it is a permitted feature in Chapter 11 of the USB specification.

Bit Number	Bit Name	Description
2:1	CURRENT_SNS	Over Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs) The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together). 01 = Individual port-by-port. 1x = Over current sensing not supported. (must only be used with Bus- Powered configurations!)
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching.

5.3.8 REGISTER 07H: CONFIGURATION DATA BYTE 2 - CFG2

Default = 0x28h

Bit Number	Bit Name	Description
7:4	Reserved	Reserved
3	COMPOUND	Compound Device: Allows the customer to indicate that the Hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a “Non-Removable Device”. 0 = No. 1 = Yes, Hub is part of a compound device.
2:0	Reserved	Reserved

5.3.9 REGISTER 08H: CONFIGURATION DATA BYTE 3 - CFG3

Default = 0x03h

Bit Number	Bit Name	Description
7:4	Reserved	Reserved
3	PRTMAP_EN	Port Re-Mapping enable: Selects the method used by the hub to assign port numbers and disable ports ‘0’ = Standard Mode. The following registers are used to define which ports are enabled, and the ports are mapped as Port “n” on the hub is reported as Port ‘n’ to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. Section 5.3.11 Register 0A Section 5.3.12 Register 0B ‘1’ = Port Re-Map mode. The mode enables remapping via the registers defined below. Section 5.3.43 Register FB Section 5.3.44 Register FC

2:1	Reserved	Reserved
0	STRING_EN	Enables String Descriptor Support ‘0’ = String Support Disabled ‘1’ = String Support Enabled

5.3.10 REGISTER 09H: NON-REMOVABLE DEVICE - NRD

Default = 0x06h

Bit Number	Bit Name	Description
7:0	NR_DEVICE	Non-Removable Device: Indicates which port(s) include non- removable devices. ‘0’ = port is removable ‘1’ = port is non- removable. Informs the Host if one of the active physical ports has a permanent device that is undetachable from the Hub. (Note: The device must provide its own descriptor data.) Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Port 3 non-removable. Bit 2= Port 2 non-removable. Bit 1= Port 1 non removable. Bit 0= Reserved

5.3.11 REGISTER 0AH: PORT DISABLE FOR SELF POWERED OPERATION - PDS

Default = 0x00h

Bit Number	Bit Name	Description
7:0	PORT_DIS_SP	Port Disable Self-Powered: Disables 1 or more ports. ‘0’ = port is available ‘1’ = port is disabled. During Self-Powered operation, when PRTMAP_EN = ‘0’, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Port 3 Disable. Bit 2= Port 2 Disable. Bit 1= Port 1 Disable. Bit 0= Reserved

5.3.12 REGISTER 0BH: PORT DISABLE FOR BUS POWERED OPERATION - PDB

Default = 0x00h

Bit Number	Bit Name	Description
7:0	PORT_DIS_BP	Port Disable Bus-Powered: Disables 1 or more ports. ‘0’ = port is available ‘1’ = port is disabled. During Bus-Powered operation, when PRTMAP_EN = ‘0’, this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB Host, and will reorder the active ports in order to ensure proper function. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Port 3 Disable. Bit 2= Port 2 Disable. Bit 1= Port 1 Disable. Bit 0= Reserved

5.3.13 REGISTER 0CH: MAX POWER FOR SELF POWERED OPERATION - MAXPS

Default = 0x01h

Bit Number	Bit Name	Description
7:0	MAX_PWR_SP	Max Power Self_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors. Example: A value of 8mA would be written to this register as 0x04h The USB 2.0 Specification does not permit this value to exceed 100mA

5.3.14 REGISTER 0DH: MAX POWER FOR BUS POWERED OPERATION - MAXPB

Default = 0xFAh- Corresponds to 500mA.

Bit Number	Bit Name	Description
7:0	MAX_PWR_BP	Max Power Bus_Powered: Value in 2mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0mA in its descriptors. Example: A value of 8mA would be written to this register as 0x04h

5.3.15 REGISTER 0EH: HUB CONTROLLER MAX CURRENT FOR SELF POWERED OPERATION - HCMCS

Default = 0x02h Corresponds to 2mA.

Bit Number	Bit Name	Description
7:0	HC_MAX_C_SP	Hub Controller Max Current Self-Powered: Value in 1mA increments that the Hub consumes from an upstream port (VBUS) when operating as a self- powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. Example: A value of 8mA would be written to this register as 0x08h **Note:** The USB 2.0 Specification does not permit this value to exceed 100mA

5.3.16 REGISTER 0FH: HUB CONTROLLER MAX CURRENT FOR BUS POWERED OPERATION - HCMCB

Default = 0x64h- Corresponds to 100mA.

Bit Number	Bit Name	Description
7:0	HC_MAX_C_BP	Hub Controller Max Current Bus-Powered: Value in 1mA increments that the Hub consumes from an upstream port (VBUS) when operating as a bus- powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. Example: A value of 8mA would be written to this register as 0x08h

5.3.17 REGISTER 10H: POWER-ON TIME - PWRT

Default = 0x00h - Corresponds to 0ms. Required for a hub with no power switches

Bit Number	Bit Name	Description
7:0	POWER_ON_TIME	Power On Time: The length of time that is takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is good on that port. System software uses this value to determine how long to wait before accessing a powered-on port. Setting affects only the hub descriptor field "PwrOn2PwrGood" see Section 7.6, "Class-Specific Hub Descriptor," on page 78.

Note: This register represents time from when a host sends a SetPortFeature(PORT_POWER) request to the time power is supplied through an external switch to a downstream port. It should be set to 0 if no power switch is used- for instance within a compound device. If external power switch is used, this value must encompass time for the system to detect an interrupt, read the PRTPWR status register using the serial port, and then close an external power switch and charge the USB VBUS line to the downstream port. Setting to max value is recommended for external power switch implementations.

5.3.18 REGISTER 11H: LANGUAGE ID HIGH - LANGIDH

Default = 0x04h - Corresponds to US English code 0x0409h

Bit Number	Bit Name	Description
7:0	LANG_ID_H	USB LANGUAGE ID (Upper 8 bits of a 16 bit ID field)

5.3.19 REGISTER 12H: LANGUAGE ID LOW - LANGIDL

Default = 0x09h - Corresponds to US English code 0x0409h

Bit Number	Bit Name	Description
7:0	LANG_ID_L	USB LANGUAGE ID (lower 8 bits of a 16 bit ID field)

5.3.20 REGISTER 13H: MANUFACTURER STRING LENGTH - MFRSL

Default = 0x00h

Bit Number	Bit Name	Description
7:0	MFR_STR_LEN	Manufacturer String Length

5.3.21 REGISTER 14H: PRODUCT STRING LENGTH - PRDSL

Default = 0x00h

Bit Number	Bit Name	Description
7:0	PRD_STR_LEN	Product String Length

5.3.22 REGISTER 15H: SERIAL STRING LENGTH - SERSL

Default = 0x00h

Bit Number	Bit Name	Description
7:0	SER_STR_LEN	Serial String Length

5.3.23 REGISTER 16H-53H: MANUFACTURER STRING - MANSTR

Default = 0x00h

Bit Number	Bit Name	Description
7:0	MFR_STR	Manufacturer String, UNICODE UTF-16LE per USB 2.0 Specification **Note:** The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Please pay careful attention to the Byte ordering or your selected programming tools.

5.3.24 REGISTER 54H-91H: PRODUCT STRING - PRDSTR

Default = 0x00h

Bit Number	Bit Name	Description
7:0	PRD_STR	Product String, UNICODE UTF-16LE per USB 2.0 Specification **Note:** The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Please pay careful attention to the Byte ordering or your selected programming tools.

5.3.25 REGISTER 92H-CFH: SERIAL STRING - SERSTR

Default = 0x00h

Bit Number	Bit Name	Description
7:0	SER_STR	Serial String, UNICODE UTF-16LE per USB 2.0 Specification **Note:** The String consists of individual 16 Bit UNICODE UTF-16LE characters. The Characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Please pay careful attention to the Byte ordering or your selected programming tools.

5.3.26 REGISTER D0: DOWNSTREAM BATTERY CHARGING ENABLE - BC_EN

Default = 0x00h

Bit Number	Bit Name	Description
7:0	BC_EN	Battery Charging Enable: Enables the battery charging feature for the corresponding downstream port. ‘0’ = Downstream Battery Charging support is not enabled. ‘1’ = Downstream Battery charging support is enabled Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Port 3 Battery Charging Enable. Bit 2= Port 2 Battery Charging Enable. Bit 1= Port 1 Battery Charging Enable. Bit 0= Reserved

5.3.27 REGISTER E2H: UPSTREAM BATTERY CHARGER DETECTION - BATT_CHG

Default = 0x02h

Bit Number	Bit Name	Description
7:5	ChargerType	Read Only. This register indicates the result of the automatic charger detection. Values reported depend on EnhancedChrgDet setting in Battery Charger Mode Register. If EnhancedChrgDet=1 000 = Charger Detection is not complete. 001 = DCP - Dedicated Charger Port 010 = CDP – Charging Downstream Port 011 = SDP – Standard Downstream Port 100 = Reserved 101 = Reserved 110 = Reserved 111 = Charger Detection Disabled If EnhancedChrgDet=0 000 = Charger Detection is not complete. 001 = DCP/CDP – Dedicated Charger or Charging Downstream Port 010 = Reserved 011 = SDP – Standard Downstream Port 100 = Reserved 101 = Reserved 110 = Reserved 111 = Charger Detection Disabled
4	ChrgDetComplete	Read Only. Indicates Charger Detection has been run and is completed. This bit is negated when START_BC_DET is asserted high.
3:2	Reserved	Reserved
1	CHG_DET_N	Single bit indication of whether an unmasked USB battery charger was detected based on the settings in CHGDETMASK register. 0 = Write: No Effect / Read: Charger detected on last charger detection sequence 1 = Write: Negate bit high / Read: No Charger was detected on last charger detection sequence
0	START_BC_DET	Manually Initiates a USB battery charger detection sequence at the time of assertion. This bit must not be set while hub is in operation. Bit is cleared automatically when the manual battery charger detection sequence is completed. 0 = Write: No Effect / Read: Battery Charger Detection Sequence Completed or not run. 1 = Write: Start Battery Charger Detection / Read: Battery Charger Detection Sequence is running

5.3.28 REGISTER E5H: PORT POWER STATUS - PRTPWR

Default = 0x00h

Bit Number	Bit Name	Description
7:4	Reserved	Reserved.
3:1	PRTPWR[3:1]	Read Only. Optional status to SOC indicating that power to the downstream port was enabled by the USB Host for the specified port. Not required for an embedded application. This is a read-only status bit. Actual control over port power is implemented by the USB Host, OCS register and Downstream Battery Charging logic if enabled. See Section 8.2.2, "Special Behavior of PRTPWR Register Bits," on page 88 for more information. 0 = USB Host has not enabled port to be powered or in downstream battery charging and corresponding OCS bit has been set. 1 = USB Host has enabled port to be powered
0	Reserved	Reserved.

5.3.29 REGISTER E6H: OVER CURRENT SENSE CONTROL - OCS

Default = 0x00h

Bit Number	Bit Name	Description
7:4	Reserved	Reserved. **Note:** Software must never write a ‘1’ to these bits.
3	OCS[3]	Optional control from SOC on indicating external current monitor indicating an over-current condition on port 3 for HUB status reporting to USB host. Also resets corresponding PRTPWR status register bit. Not required for an embedded application. 0 = No Over Current Condition 1 = Over Current Condition
2:1	OCS[2:1]	Optional control from SOC on indicating external current monitor indicating an over-current condition on the specified port for HUB status reporting to USB host. Also resets corresponding PRTPWR status register bit. Not required for an embedded application. 0 = No Over Current Condition 1 = Over Current Condition
0	Reserved	Reserved.

5.3.30 REGISTER E7H: SERIAL PORT INTERLOCK CONTROL - SP_ILOCK

Default=0x02h - Corresponds to I2C_ASEL pins & pausing to connect until write from I2C

Bit Number	Bit Name	Description
7:6	Reserved	Reserved
5:4	Reserved	Reserved
3:2	Reserved	Reserved

Bit Number	Bit Name	Description
1	connect_n	The SOC can utilize this bit to control when the hub attempts to connect to the upstream host. (Alternatively, HUB_CONNECT is used to proceed through Hub Connect Stage, as shown in Figure 4-1.) 1 = Device will remain in Hub Mode.Connect Stage indefinitely until bit is cleared by the SOC. 0 = Device will transition to the Hub Mode.Communication Stage after this bit is asserted low by default or through a serial port write.
0	config_n	If the SOC intends to update the default configuration using the serial port, this register should be the first register updated by the SOC. In this way the timing dependency between configuration and device operation can be minimized- the SOC is only required to write to Serial Port Interlock Register within $T_{hubconfig}$ and not all the registers it is attempting to configure. Once all registers have been written for the desired configuration, the SOC must clear this bit to '0' for the device to resume normal operation using the new configuration. It may be desirable for the device to initiate autonomous operation (i.e. battery charger detection, dead battery) with no SOC intervention at all. This is why the default setting is to allow the device to initiate automatic operation if the SOC does not intervene by writing the interlock register within the allotted configuration timeout. 1 = Device will remain in Hub Mode.Configuration Stage indefinitely, and allow SOC to write through the serial port to set any desired configuration. 0 = Device will transition out of Hub.Configuration Stage and into the Hub Mode.Charger Detection Stage immediately after this bit is asserted low through a serial port write. (A default low assertion results in transition after a timeout.)

5.3.31 REGISTER E8H: SERIAL PORT INTERRUPT STATUS - INT_STATUS

Default = 0x00h

Bit Number	Bit Name	Description
7	Interrupt	Read: 1 = INT_N pin has been asserted low due to unmasked interrupt 0 = INT_N pin has not been asserted low due to unmasked interrupt Write: 1 = No Effect – INT_N pin and register retains its current value 0 = Negate INT_N pin high
6:5	Reserved	Reserved
4	HubSuspInt	Read: 1 = Hub has entered USB suspend 0 = Hub has not entered USB suspend since last HubSuspInt reset Write: 1 = No Effect 0 = Negate HubSuspInt status low
3	HubCfgInt	Read: 1 = Hub has been configured by USB Host 0 = Hub has not been configured by USB Host since last HubConfInt reset Write: 1 = No Effect 0 = Negate HubConfInt status low

Bit Number	Bit Name	Description
2	PrtPwrInt	Read: 1 = Port Power register has been updated 0 = Port Power register has not been updated since last PrtPwrInt reset Write: 1 = No Effect 0 = Negate PrtPwrInt status low
1	ChrgDetInt	Read: 1 = CHG_DET_N bit in Charger Detect Register has been asserted low 0 = CHG_DET_N bit has not been updated since last ChrgDetInt reset Write: 1 = No Effect 0 = Negate ChrgDetInt status low
0	ChrgDetComp-Int	Read: 1 = ChrgDetComplete bit in Charger Detect Register has been asserted high 0 = ChrgDetComplete bit in Charger Detect Register has not been updated since last ChrgDetCompInt reset Write: 1 = No Effect 0 = Negate ChrgDetCompInt status low

5.3.32 REGISTER E9H: SERIAL PORT INTERRUPT MASK - INT_MASK

Default = 0x00h

Bit Number	Bit Name	Description
7:5	Reserved	Reserved
4	HubSuspMask	1 = INT_N pin is asserted low when Hub enters suspend 0 = INT_N pin is not affected by Hub entering suspend
3	HubCfgMask	1 = INT_N pin is asserted low when Hub configured by USB Host 0 = INT_N pin is not affected by Hub configuration event
2	PrtPwrMask	1 = INT_N pin is asserted low when Port Power register has been updated by USB Host 0 = INT_N pin is not affected by Port Power register
1	ChrgDetMask	1 = INT_N pin is asserted low when CHG_DET_N bit in Charger Detect Register is asserted low 0 = INT_N pin is not affected by CHG_DET_N
0	ChrgDetComp-Mask	1 = INT_N pin is asserted low when ChrgDetComplete bit in Charger Detect Register is asserted high 0 = INT_N pin is not affected by ChrgDetComplete

5.3.33 REGISTER EAH: I^2C ADDRESS 0 - I2CADD0

Default = 0x08h - Corresponds to I2C Address on USB3803 with I2C_ASEL='00'.

Bit Number	Bit Name	Description
7	Reserved	Reserved (serial port interface only uses a 7-bit address)
6:1	I2C_ADDR0	Read Only. The six most significant bits of I2C Address when I2C_ASEL1 input pin is set to '0'
0	Reserved	Reserved (LSB of I2C Address controlled by I2C_ASEL0 Pin)

5.3.34 REGISTER EBH: I^{2}C ADDRESS 1 - I2CADD1

Default = 0x28h - Corresponds to I2C Address on USB3803 with I2C_ASEL ='10'.

Bit Number	Bit Name	Description
7	Reserved	Reserved (serial port interface only uses a 7-bit address)
6:1	I2C_ADDR1	Read Only. The six most significant bits of I2C Address when I2C_ASEL1 input pin is set to '1'
0	Reserved	Reserved (LSB of I2C Address controlled by I2C_ASEL0 Pin)

5.3.35 REGISTER ECH: BATTERY CHARGER MODE - BCHGMODE

Default = 0x14h - Corresponds to Charge detection enabled for SDP, CDP and DCP

Bit Number	Bit Name	Description
7:6	Reserved	Reserved
5	Reserved	Reserved
4	EnableChrgDet	If enabled the charger detection routine will be executed automatically once HUB.ChgDet stage is entered or during Hub.WaitRefClk stage if no reference clock is available.
3	Reserved	Reserved
2	EnhancedChrg-Det	When enabled the charger detection routine will reverse Vdat SRC to differentiate between a CDP and a DCP.
1:0	Reserved	Reserved

5.3.36 REGISTER EDH: CHARGER DETECT MASK - CHGDETMASK

Default = 0x0Fh - Any enabled charger detected causing interrupt status to toggle.

Bit Number	Bit Name	Description
7:4	Reserved	Reserved
3	Reserved	Reserved
2	Reserved	Reserved
1	CDPMask	1 = BATT_CHG.CHG_DET_N is asserted low when a CDP Charger is detected 0 = BATT_CHG.CHG_DET_N is not affected by detection of a CDP Charger This mask bit should only be enabled if EnhancedChrgDet in is asserted in Section 5.3.35, "Register ECh: Battery Charger Mode - BCHGMODE" because without it, the charger detection is unable to identify a CDP.
0	DCPMask	1 = BATT_CHG.CHG_DET_N is asserted low when a DCP Charger is detected 0 = BATT_CHG.CHG_DET_N is not affected by detection of a DCP Charger

5.3.37 REGISTER EEH: CONFIGURE PORTABLE HUB - CFGP

Default = 0x10h - Corresponds to 400ms startup & Phone RefClks available

Bit Number	Bit Name	Description
7	ClkSusp	(Read/Write) 1 = Force device to run internal clock even during USB suspend (will cause device to violate USB suspend current limit - intended for test or self-powered applications which require use of serial port during USB session.) 0 = Allow device to gate off its internal clocks during suspend mode in order to meet USB suspend current requirements.
6	IntSusp	(Read/Write) 1 = INT_N pin function is a level sensitive USB suspend interrupt indication. Allows system to adjust current consumption to comply with USB specification limits when hub is in the USB suspend state. 0 = INT_N pin function retains event sensitive role of a general serial port interrupt. See Section 3.4.4, "Interrupt and Charger Detect," on page 26 for more information.
5:4	CfgTout	(Read Only) Specifies timeout value for allowing SOC to configure the device. Corresponds to the $T_{hubconfig}$ parameter. See Table 4-2, “Timing Parameters for Hub Stages,” on page 19. ‘01’ = 400ms - Use to meet 1s connect timing with charger detection
3	Reserved	Reserved
2:0	Reserved	Reserved

5.3.38 REGISTER F4H: VARISENSE_UP3 - VSNSUP3

Default = 0x00h

Bit Number	Bit Name	Description
7	Reserved	Reserved
6:4	UP_SQUELCH	These two bits control the Squelch setting of the upstream PHY. ‘000’ = Nominal value ‘001’ = 90% of Nominal value ‘010’ = 80% of Nominal value ‘011’ = 70% of Nominal value ‘100’ = 60% of Nominal value ‘101’ = 50% of Nominal value ‘110’ = 120% of Nominal value ‘111’ = 110% of Nominal value

Bit Number	Bit Name	Description
3	Reserved	Reserved
2:0	DN3_SQUELCH	These two bits control the Squelch setting of the downstream port 3. ‘000’ = Nominal value ‘001’ = 90% of Nominal value ‘010’ = 80% of Nominal value ‘011’ = 70% of Nominal value ‘100’ = 60% of Nominal value ‘101’ = 50% of Nominal value ‘110’ = 120% of Nominal value ‘111’ = 110% of Nominal value

5.3.39 REGISTER F5H: VARISENSE_21 - VSNS21

Default = 0x00h

Bit Number	Bit Name	Description
7	Reserved	Reserved
6:4	DN2_SQUELCH	These two bits control the Squelch setting of the downstream port 2. ‘000’ = Nominal value ‘001’ = 90% of Nominal value ‘010’ = 80% of Nominal value ‘011’ = 70% of Nominal value ‘100’ = 60% of Nominal value ‘101’ = 50% of Nominal value ‘110’ = 120% of Nominal value ‘111’ = 110% of Nominal value
3	Reserved	Reserved
2:0	DN1_SQUELCH	These three bits control the Squelch setting of the downstream port 1. ‘000’ = Nominal value ‘001’ = 90% of Nominal value ‘010’ = 80% of Nominal value ‘011’ = 70% of Nominal value ‘100’ = 60% of Nominal value ‘101’ = 50% of Nominal value ‘110’ = 120% of Nominal value ‘111’ = 110% of Nominal value

5.3.40 REGISTER F6H: BOOST_UP3 - BSTUP3

Default = 0x30h

Bit Number	Bit Name	Description
7	Reserved	Reserved
6:4	BOOST_IOUT_A	USB electrical signaling drive strength Boost Bit for Upstream Port ‘A’. Boosts USB High Speed Current. 3’b000: Nominal 3’b001: -5% 3’b010: +10% 3’b011: +5% 3’b100: +20% 3’b101: +15% 3’b110: +30% 3’b111: +25%

Bit Number	Bit Name	Description
3	Reserved	Reserved
2:0	BOOST_IOUT_3	USB electrical signaling drive strength Boost Bit for Downstream Port ‘3’. Boosts USB High Speed Current. 3’b000: Nominal 3’b001: -5% 3’b010: +10% 3’b011: +5% 3’b100: +20% 3’b101: +15% 3’b110: +30% 3’b111: +25%

5.3.41 REGISTER F8H: BOOST_21 - BST21

Default = 0x00h

Bit Number	Bit Name	Description
7	Reserved	Reserved
6:4	BOOST_IOUT_2	USB electrical signaling drive strength Boost Bit for Downstream Port ‘2’. Boosts USB High Speed Current. 3’b000: Nominal 3’b001: -5% 3’b010: +10% 3’b011: +5% 3’b100: +20% 3’b101: +15% 3’b110: +30% 3’b111: +25%
3	Reserved	Reserved
2:0	BOOST_IOUT_1	USB electrical signaling drive strength Boost Bit for Downstream Port ‘1’. Boosts USB High Speed Current. 3’b000: Nominal 3’b001: -5% 3’b010: +10% 3’b011: +5% 3’b100: +20% 3’b101: +15% 3’b110: +30% 3’b111: +25%

5.3.42 REGISTER FAH: PORT SWAP - PRTSP

Default = 0x00h

Bit Number	Bit Name	Description
7:0	PRTSP	Port Swap: Swaps the Upstream and Downstream USB DP and DM Pins for ease of board routing to devices and connectors. ‘0’ = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. The setting affects only HUB mode - it has no impact in BYPASS mode. ‘1’ = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. The setting affects only HUB mode - it has no impact in BYPASS mode. Bit 7= Reserved Bit 6= Reserved Bit 5= Reserved Bit 4= Reserved Bit 3= Port 3 DP/DM Swap. Bit 2= Port 2 DP/DM Swap. Bit 1= Port 1 DP/DM Swap. Bit 0= Upstream Port DP/DM Swap

5.3.43 REGISTER FBH: PORT REMAP 12 - PRTR12

Default = 0x21h - Physical Port is mapped to the corresponding logical port.

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th colspan="3">Description</th></tr>
<tr><td rowspan="13">7:0</td><td rowspan="13">PRTR12</td><td colspan="3">Port remap register for ports 1 & 2.

When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has, the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number ‘1’, up to the number of ports that the hub reported having.

The host’s port number is referred to as “Logical Port Number” and the physical port on the hub is the Physical Port Number”. When remapping mode is enabled (see PRTMAP_EN in Section 5.3.9) the hub’s downstream port numbers can be remapped to different logical port numbers (assigned by the host.)

Note: The customer must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports, this ensures that the hub’s ports are numbered in accordance with the way a Host will communicate with the ports.</td></tr>
<tr><td>Bit [7:4] =</td><td>‘0000’</td><td>Physical Port 2 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 2 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 2 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 2 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Reserved, will default to ‘0000’ value</td></tr>
<tr><td></td><td>‘0101’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
<tr><td>Bit [3:0] =</td><td>‘0000’</td><td>Physical Port 1 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 1 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 1 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 1 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’</td><td>Reserved, will default to ‘0000’ value</td></tr>
<tr><td></td><td>‘0101’ to ‘1111’</td><td>Reserved, will default to ‘0000’ value</td></tr>
</table>

5.3.44 REGISTER FCH: PORT REMAP 34 - PRTR34

Default = 0x03h - Physical port is mapped to corresponding logical port.

Bit Number	Bit Name	Description		
7:0	PRTR34	Port remap register for ports 3. When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has, the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number ‘1’, up to the number of ports that the hub reported having. The host’s port number is referred to as “Logical Port Number” and the physical port on the hub is the Physical Port Number”. When remapping mode is enabled (see PRTMAP_EN in Section 5.3.9) the hub’s downstream port numbers can be remapped to different logical port numbers (assigned by the host). Note: the customer must ensure that Contiguous Logical Port Numbers are used, starting from #1 up to the maximum number of enabled ports, this ensures that the hub’s ports are numbered in accordance with the way a Host will communicate with the ports.		
		Bit [7:4] =	‘0000’	Reserved – software must not write ‘1’ to any of these bits.
			‘0001’ to ‘1111’	Reserved, will default to ‘0000’ value
		Bit [3:0] =	‘0000’	Physical Port 3 is Disabled
			‘0001’	Physical Port 3 is mapped to Logical Port 1
			‘0010’	Physical Port 3 is mapped to Logical Port 2
			‘0011’	Physical Port 3 is mapped to Logical Port 3
			‘0100’	Reserved, will default to ‘0000’ value Physical Port 3 is mapped to Logical Port 4
			‘0101’ to ‘1111’	Reserved, will default to ‘0000’ value

5.3.45 REGISTER FFH: STATUS/COMMAND - STCD

Default = 0x00h

Bit Number	Bit Name	Description
7:2	Reserved	Reserved **Note:** Software must never write a ‘1’ to these bits
1	RESET	Reset the Serial Interface and internal memory registers in address range 00h-E1h and EFh-FFh back to RESET_N assertion default settings. **Note:** During this reset, this bit is automatically cleared to its default value of 0.} 0 = Normal Run/Idle State. 1 = Force a reset of the registers to their default state.
0	CONFIG_PROTECT	Protect the Configuration 0 = serial slave interface is active. 1 = The internal configuration memory (address range 00h-E1h and EFh-FFh) is “write-protected” to prevent unintentional data corruption. **Note:** This bit is write once and is only cleared by assertion of the external RESET_N pin.

6.0 SERIAL SLAVE INTERFACE

6.1 Overview

The serial slave interface on USB3803 is implemented as I^2C. It is a standard I^2C slave interface that operates at the standard (100Kbps), fast (400Kbps), and the fast mode plus (1Mbps) modes.

The USB3803 I^2C slave interface supports four 7-bit slave addresses. Address selection is done through values set on the I2C_ASEL1 and I2C_ASEL0 pins during the HUB.INIT stage as shown in Table 6-1, "Serial Slave Address Selection".

REFCLK must be running for I^2C to operate. The register map is outlined in section Section 5.3.

Two I^2C Slave Base Addresses will be programmed into ROM and selected with the I2C_ASEL1 pin. The LSB of the serial slave address is selected with the I2C_ASEL0 pin. Table 6-1, "Serial Slave Address Selection" shows resulting I^2C address based on I2C_ASEL pin settings and default ROM programmed register values. In the table bits a_{6-1} represent bits programmed into register I2CADD0 and bits b_{6-1} represent bits programmed into register I2CADD1. Detailed definition can be found in Section 5.3.33, "Register EAh: I2C Address 0 - I2CADD0," on page 42 and Section 5.3.34, "Register EBh: I2C Address 1 - I2CADD1," on page 43. Table 6-2 shows a specific example of the resulting addresses with two specific examples of default control register values. The addresses are shown both in binary and hexadecimal format in parenthesis for clarity.

TABLE 6-1: SERIAL SLAVE ADDRESS SELECTION

I2C_ASEL1	I2C_ASEL0	I2CADD0 Register Value	I2CADD1 Register Value	Functional I2C Address Result
0	0	$0a_6a_5a_4a_3a_2a_10$	don't care	$a_6a_5a_4a_3a_2a_10$
0	1	$0a_6a_5a_4a_3a_2a_10$	don't care	$a_6a_5a_4a_3a_2a_11$
1	0	don't care	$0b_6b_5b_4b_3b_2b_10$	$b_6b_5b_4b_3b_2b_10$
1	1	don't care	$0b_6b_5b_4b_3b_2b_10$	$b_6b_5b_4b_3b_2b_11$

TABLE 6-2: EXAMPLE SERIAL SLAVE ADDRESSES

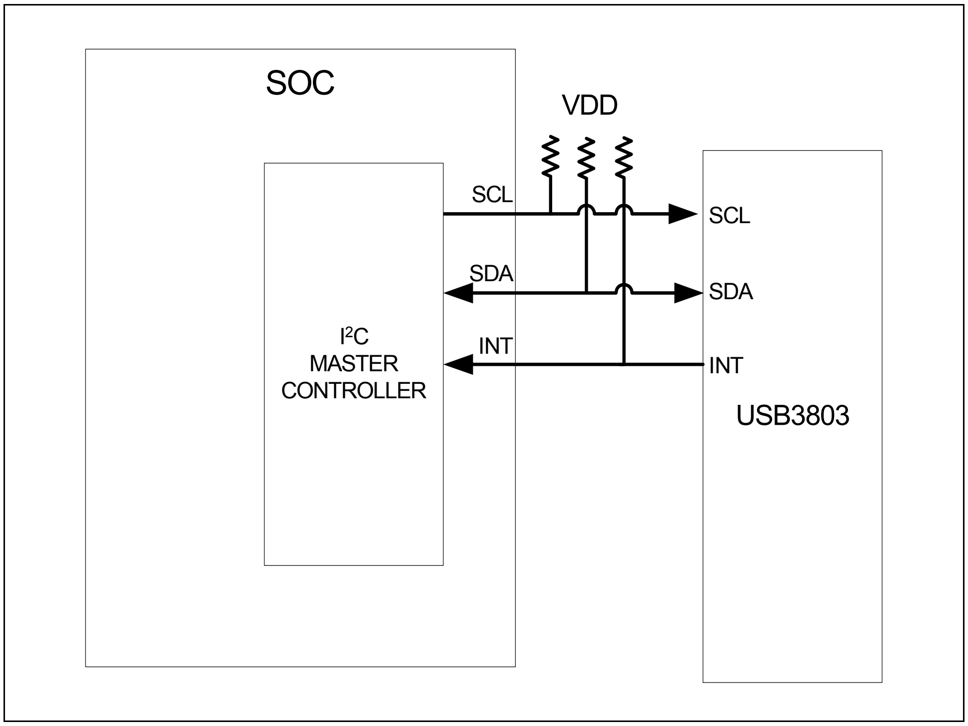
I2C_ASEL1	I2C_ASEL0	Example I2CADD0 Register Value	Example I2CADD1 Register Value	Functional I2C Address Result
0	0	0001000 (0x08)	00101000 (0x28)	0001000 (0x08)
0	1	0001000 (0x08)	00101000 (0x28)	0001001 (0x09)
1	0	0001000 (0x08)	00101000 (0x28)	0101000 (0x28)
1	1	0001000 (0x08)	00101000 (0x28)	0101001 (0x29)

The interrupt pin INT_N is used to communicate status changes on selected events which are mapped into the Serial Port Interrupt Status Register. The SOC can mask events to not cause the interrupt pin to transition by updating the Serial Port Interrupt Mask Register- the status events will still be captured in the status register even if the interrupt pin is not asserted. The serial port has limited speed and latency capability so events mapped into the serial ports and its interrupt are not expected to be latency critical.

INT_N is asserted low whenever an unmasked bit is set in the Serial Port Interrupt Status Register. SOC must update the Serial Port Interrupt Status Register to negate the interrupt high.

6.2 Interconnecting the USB3803 to an I^{2}C Master

FIGURE 6-1: I^{2}C CONNECTIONS



Note:	The largest pullup values which meet the customer application should be selected in order to minimize power consumption. Pullup values must also have low enough resistance to support the desired i^{2}C operating speed with the expected total capacitance in the application. Typical applications are expected to use pullup values between 220Ω and 2.7kΩ for operation at 1MHz on SCL and SDA. Larger pullup resistors may be acceptable for operation at 400KHz or 100KHz.

6.3 I^{2}C Message Format

6.3.1 SEQUENTIAL ACCESS WRITES

The I^{2}C interface will support sequential writing of the register address space of the USB3803. This mode is useful for configuring contiguous blocks of registers. Please see section on SOC interface for address definitions. Figure 6-2 shows the format of the sequential write operation. Where color is visible in the figure, blue indicates signaling from the I^{2}C master, and gray indicates signaling from the USB3803 slave:

FIGURE 6-2: I^{2}C SEQUENTIAL ACCESS WRITE FORMAT

S	7-Bit Slave Address	0	A	xxxxxxxx	A	nnnnnnnn	A	...	nnnnnnnn	A	P
				Register Address (bits 7-0)		Data value for XXXXXX			Data value for XXXXXX + y		

In this operation, following the 7-bit slave address, 8-bit register address is written indicating the start address for sequential write operation. Every data access after that is a data write to a data register where the register address increments after each access and ACK from the slave must occur. Sequential write access is terminated by a Stop condition.

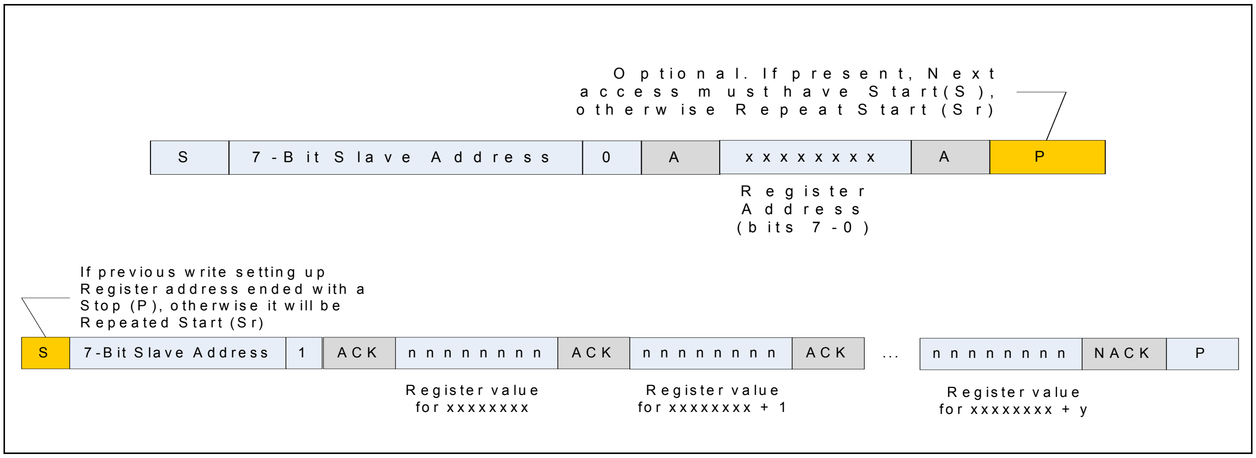
6.3.2 SEQUENTIAL ACCESS READS

The I^2C interface will support direct reading of the USB3803 registers. In order to read one or more register addresses, the starting address must be set by using a write sequence followed by a read. The read register interface supports auto-increment mode. The master should send a NACK instead of an ACK when the last byte has been transferred.

In this operation, following the 7-bit slave address, 8-bit register address is written indicating the start address for sequential read operation to be followed. In the read sequence, every data access is a data read from a data register where the register address increments after each access. Write sequence can end with optional Stop (P). If so the Read sequence must start with a Start (S) otherwise it must start with Repeated Start (Sr).

Figure 6-3 shows the format of the read operation. Where color is visible in the figure, blue and gold indicate signaling from the I^2C master, and gray indicates signaling from the USB3803 slave.

FIGURE 6-3: SEQUENTIAL ACCESS READ FORMAT



6.3.3 I^2C TIMING

Below is the timing diagram and timing specifications for the different I2C modes that the USB3803 supports.

FIGURE 6-4: I^2C TIMING DIAGRAM

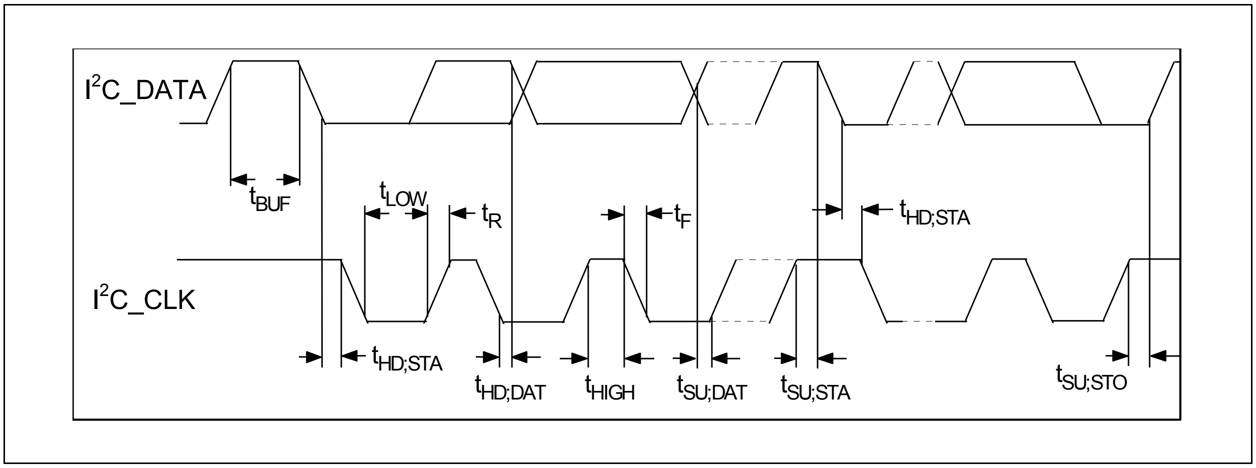


TABLE 6-3: I²C TIMING SPECIFICATIONS

Symbol	Parameter	Standard-Mode		Fast-Mode		Fast-Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
$t_{HD;STA}$	Hold time START condition	4		0.6		0.26		µs
t_{LOW}	LOW period of the SCL clock	4.7		1.3		0.5		µs
t_{HIGH}	HIGH period of the SCL clock	4		0.6		0.26		µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7		0.6		0.26		µs
$t_{HD;DAT}$	DATA hold time	0		0		0		ns
$t_{SU;DAT}$	DATA set-up time	250		100		50		ns
t_R	Rise time of both SDA and SCL signals		1000		300		120	ns
t_F	Fall time of both SCL and SDA lines		300		300		120	ns
$t_{SU;STO}$	Set-up time for a STOP condition	4		0.6		0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		0.5		µs

7.0 USB DESCRIPTORS

A customer can indirectly affect which descriptors are reported via one of two methods. The two methods are: Internal Default ROM Configuration, or direct load through the serial port interface.

The Microchip Hub will not electrically attach to the USB until after it has loaded valid data for all user- defined descriptor fields (either through Internal Default ROM, or serial port).

7.1 USB Bus Reset

In response to the upstream port signaling a reset to the Hub, the Hub does the following:

- The Hub does not propagate the upstream USB reset to downstream devices.
- Sets default address to 0.
- Sets configuration to: Unconfigured.
- Negates PRTPWR[3:1] register for all downstream ports.
- Clears all TT buffers.
- Moves device from suspended to active (if suspended).
- Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

The Host then configures the Hub and the Hub's downstream port devices in accordance with the USB Specification.

7.2 Hub Attached as a Full-Speed Device, (High-Speed Disabled)

When High-Speed capability is disabled via customer configuration options, the hub will only be able to attach as a Full-Speed device, and the following descriptor information applies.

7.2.1 STANDARD DEVICE DESCRIPTOR

The following table provides the descriptor values for Full-Speed operation.

TABLE 7-1: DEVICE DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	12h	Size of this Descriptor.
1	DescriptorType	1	01h	Device Descriptor Type.
2	USB	2	0200h	USB Specification Release Number.
4	DeviceClass	1	09h	Class code assigned by USB-IF for Hubs.
5	DeviceSubClass	1	00h	Class code assigned by USB-IF for Hubs.
6	DeviceProtocol	1	00h	Protocol code.
7	MaxPacketSize0	1	40h	64-byte packet size.
8	Vendor	2	user/ default	Vendor ID; customer value defined in ROM or serial port load.
10	Product	2	user/ default	Product ID; customer value defined in ROM or serial port load.
12	Device	2	user/ default	Device ID; customer value defined in ROM or serial port load.
14	Manufacturer	1	xxh	If STRING_EN =0 Optional string is not supported, and xx = 00. If STRING_EN = 1, String support is enabled, and xx = 01

TABLE 7-1: DEVICE DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
15	Product	1	yyh	If STRING_EN =0 Optional string is not supported, and yy = 00. If STRING_EN = 1, String support is enabled, and yy = 02
16	SerialNumber	1	zzh	If STRING_EN =0 Optional string is not supported, and zz = 00. If STRING_EN = 1, String support is enabled, and zz = 03
17	NumConfigurations	1	01h	Supports 1 configuration.

7.2.2 CONFIGURATION DESCRIPTORS

The following table provides the configuration descriptors for Full-Speed operation.

TABLE 7-2: CONFIGURATION DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	02h	Configuration Descriptor Type.
2	TotalLength	2	yyyyh	Total combined length of all descriptors for this configuration (configuration, interface, endpoint, and class- or vendor-specific). yyyyh = 0019h
4	NumInterfaces	1	01h	Number of interfaces supported by this configuration.
5	ConfigurationValue	1	01H	Value to use as an argument to the SetConfiguration() request to select this configuration.
6	Configuration	1	00h	Index of string descriptor describing this configuration (string not supported).
7	Attributes	1	user/ signal	Configuration characteristics: Communicates the capabilities of the hub regarding Remote Wake-up capability, and also reports the self-power status. In all cases, the value reported to the host always indicates that the hub supports Remote Wakeup. The value reported to the host is dependant upon the SELF_BUS_PWR bit (CONFIG_BYTE_1) = A0h for Bus-Powered (SELF_BUS_PWR = 0). = E0h for Self-Powered (SELF_BUS_PWR = 1). All other values are reserved.

TABLE 7-2: CONFIGURATION DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
8	MaxPower	1	user	Maximum Power Consumption of the Hub from VBUS when fully operational. This value includes all support circuitry associated with the hub (including an attached “embedded” peripheral if hub is part of a compound device), and is in 2mA increments. The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) is used to determine which of the values below are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: ‘MAX_PWR_BP’ if SELF_BUS_PWR = ‘0’ ‘MAX_PWR_SP’ if SELF_BUS_PWR = ‘1’ In all cases the reported value is sourced from the MAX POWER data field (for Self or Bus power) that was loaded by Internal Default, or serial port configuration.

7.2.3 INTERFACE DESCRIPTOR (FULL-SPEED)

The following table provides the interface descriptor values for Full-Speed operation.

TABLE 7-3: INTERFACE DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor
1	DescriptorType	1	04h	Interface Descriptor Type
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	00h	Value used to select this alternate setting for the interface.
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not including endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code
7	InterfaceProtocol	1	00h	Protocol code.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.2.4 ENDPOINT DESCRIPTOR

The following table provides the endpoint descriptor values for Full-Speed operation.

TABLE 7-4: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint's attributes (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	FFh	Interval for polling endpoint for data transfers (Maximum Possible).

7.3 Hub Attached as a Full-Speed Device, But is High-Speed Capable

When attached as a Full-Speed device (most likely due to being connected to a Host Controller or Operating System that is not High-Speed capable), the following descriptor information applies.

7.3.1 STANDARD DEVICE DESCRIPTOR

The following table provides the descriptor values for Full-Speed operation.

TABLE 7-5: DEVICE DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	12h	Size of this Descriptor.
1	DescriptorType	1	01h	Device Descriptor Type.
2	USB	2	0200h	USB Specification Release Number.
4	DeviceClass	1	09h	Class code assigned by USB-IF for Hubs.
5	DeviceSubClass	1	00h	Class code assigned by USB-IF for Hubs.
6	DeviceProtocol	1	00h	Protocol code.
7	MaxPacketSize0	1	40h	64-byte packet size.
8	Vendor	2	user/ default	Vendor ID; customer value defined in ROM or serial port load.
10	Product	2	user/ default	Product ID; customer value defined in ROM or serial port load.
12	Device	2	user/ default	Device ID; customer value defined in ROM or serial port load.
14	Manufacturer	1	xxh	If STRING_EN =0 Optional string is not supported, and xx = 00. If STRING_EN = 1, String support is enabled, and xx = 01

TABLE 7-5: DEVICE DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
15	Product	1	yyh	If STRING_EN =0 Optional string is not supported, and yy = 00. If STRING_EN = 1, String support is enabled, and yy = 02
16	SerialNumber	1	zzh	If STRING_EN =0 Optional string is not supported, and zz = 00. If STRING_EN = 1, String support is enabled, and zz = 03
17	NumConfigurations	1	01h	Supports 1 configuration.

7.3.2 DEVICE QUALIFIER DESCRIPTOR

The following table provides the device qualifier values for High-Speed operation.

TABLE 7-6: DEVICE QUALIFIER (HIGH-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	0Ah	Size of this Descriptor.
1	DescriptorType	1	06h	Device Descriptor Type.
2	USB	2	0200h	USB Specification Release Number.
4	DeviceClass	1	09h	Class code assigned by USB-IF for Hubs.
5	DeviceSubClass	1	00h	Class code assigned by USB-IF for Hubs.
6	DeviceProtocol	1	user	Protocol code (01h if customer selects Single-TT, 02h if customer selects Multiple-TT).
7	MaxPacketSize0	1	40h	64-byte packet size for the other speed.
8	NumConfigurations	1	01h	Supports 1 other speed configuration.
9	Reserved	1	00h	Reserved.

7.3.3 CONFIGURATION DESCRIPTORS

The following table provides the configuration descriptors for Full-Speed operation.

TABLE 7-7: CONFIGURATION DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	02h	Configuration Descriptor Type.
2	TotalLength	2	yyyyh	Total combined length of all descriptors for this configu-ration (configuration, interface, endpoint, and class- or vendor-specific). yyyyh = 0019h
4	NumInterfaces	1	01h	Number of interfaces supported by this configuration.

TABLE 7-7: CONFIGURATION DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
5	ConfigurationValue	1	01H	Value to use as an argument to the SetConfiguration() request to select this configuration.
6	Configuration	1	00h	Index of string descriptor describing this configuration (string not supported).
7	Attributes	1	user/ signal	Configuration characteristics: Communicates the capabilities of the hub regarding Remote Wake-up capability, and also reports the self-power status. In all cases, the value reported to the host always indicates that the hub supports Remote Wakeup. The value reported to the host is dependant upon the SELF_BUS_PWR bit (CONFIG_BYTE_1) = A0h for Bus-Powered (SELF_BUS_PWR = 0). = E0h for Self-Powered (SELF_BUS_PWR = 1). All other values are reserved.
8	MaxPower	1	user	Maximum Power Consumption of the Hub from VBUS when fully operational. This value includes all support circuitry associated with the hub (including an attached “embedded” peripheral if hub is part of a compound device), and is in 2mA increments. The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) are used to determine which of the values below are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: ‘MAX_PWR_BP’ if SELF_BUS_PWR = ‘0’ ‘MAX_PWR_SP’ if SELF_BUS_PWR = ‘1’ In all cases the reported value is sourced from the MAX POWER data field (for Self or Bus power) that was loaded by Internal Default, or serial port configuration.

7.3.4 INTERFACE DESCRIPTOR (FULL-SPEED)

The following table provides the interface descriptor values for Full-Speed operation.

TABLE 7-8: INTERFACE DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor
1	DescriptorType	1	04h	Interface Descriptor Type
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	00h	Value used to select this alternate setting for the interface.

TABLE 7-8: INTERFACE DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not including endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code
7	InterfaceProtocol	1	00h	Protocol code.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.3.5 ENDPOINT DESCRIPTOR

The following table provides the endpoint descriptor values for Full-Speed operation.

TABLE 7-9: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint's attributes (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	FFh	Interval for polling endpoint for data transfers (Maximum Possible).

7.3.6 OTHER-SPEED CONFIGURATION DESCRIPTOR

The following table provides the other-speed configuration descriptor values for High-Speed operation.

TABLE 7-10: OTHER-SPEED CONFIGURATION DESCRIPTOR (HIGH-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	07h	Other-Speed Configuration Descriptor Type.
2	TotalLength	2	zzzzh	Total combined length of all descriptors for this configuration. zzzz = 0019h if MTT_ENABLE=0 zzzz = 0029h if MTT_ENABLE=1
4	NumInterfaces	1	01h	Number of interfaces supported by this configuration.
5	ConfigurationValue	1	01H	Value to use to select configuration.
6	Configuration	1	00h	Index of String Descriptor describing this configuration (string not supported).

TABLE 7-10: OTHER-SPEED CONFIGURATION DESCRIPTOR (HIGH-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
7	Attributes	1	user/ signal	Configuration characteristics: Communicates the capabilities of the hub regarding Remote Wake-up capability, and also reports the self-power status. In all cases, the value reported to the host always indicates that the hub supports Remote Wakeup. The value reported to the host is dependant upon the SELF_BUS_PWR bit (CONFIG_BYTE_1) = A0h for Bus-Powered (SELF_BUS_PWR = 0). = E0h for Self-Powered (SELF_BUS_PWR = 1). All other values are reserved.
8	MaxPower	1	user	Maximum Power Consumption of the Hub from VBUS when fully operational. This value includes all support circuitry associated with the hub (including an attached “embedded” peripheral if hub is part of a compound device), and is in 2mA increments. The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) is used to determine which of the values below are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: ‘MAX_PWR_BP’ if SELF_BUS_PWR = ‘0’ ‘MAX_PWR_SP’ if SELF_BUS_PWR = ‘1’ In all cases the reported value is sourced from the MAX POWER data field (for Self or Bus power) that was loaded by Internal Default, or serial port configuration.

7.3.7 INTERFACE DESCRIPTOR (SINGLE-TT)

The following table provides the interface descriptor values for Single-TT, High-Speed operation.

TABLE 7-11: INTERFACE DESCRIPTOR (HIGH-SPEED, SINGLE-TT)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	04h	Interface Descriptor Type.
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	00h	Value used to select this alternate setting for the interface.
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not including endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code.

TABLE 7-11: INTERFACE DESCRIPTOR (HIGH-SPEED, SINGLE-TT) (CONTINUED)

Offset	Field	Size	Value	Description
7	InterfaceProtocol	1	xxh	Protocol xx = 00h if bNumInterfaces = 01h (Single-TT). xx = 01h if bNumInterfaces = 02h (Multi-TT).
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.3.8 ENDPOINT DESCRIPTOR (SINGLE-TT)

The following table provides the endpoint descriptor values for Single-TT operation.

TABLE 7-12: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, SINGLE-TT)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB Device.
3	Attributes	1	03h	Describes the endpoint’s attributes (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	0Ch	Interval for polling endpoint for data transfers (Maximum Possible).

7.3.9 INTERFACE DESCRIPTOR (MULTI-TT)

The following table provides interface descriptor values for High-Speed, Multi-TT operation.

Note: This is only available if Multi-TT is reported in the other Other-Speed Configuration Descriptor.

TABLE 7-13: INTERFACE DESCRIPTOR (HIGH-SPEED, MULTI-TT)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	04h	Interface Descriptor Type.
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	01h	Value used to select this alternate setting for the inter-face.
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not includ-ing endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code.
7	InterfaceProtocol	1	02h	Protocol code.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported)

7.3.10 ENDPOINT DESCRIPTOR (MULTI-TT)

The following table provides endpoint descriptor values for Multi-TT operation.

Note:	This is only available if Multi-TT is reported in the Other-Speed Configuration Descriptor.

TABLE 7-14: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, MULTI-TT)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint’s attributes (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	0Ch	Interval for polling endpoint for data transfers (Maximum Possible).

7.4 Hub Attached as a High-Speed Device (Customer-Configured for Single-TT Support Only)

The following tables provide descriptor information for Customer-Configured Single-TT-Only Hubs attached for use with High-Speed devices.

7.4.1 STANDARD DEVICE DESCRIPTOR

The following table provides device descriptor values for High-Speed operation.

TABLE 7-15: DEVICE DESCRIPTOR

Offset	Field	Size	Value	Description
0	Length	1	12h	Size of this Descriptor.
1	DescriptorType	1	01h	Device Descriptor Type.
2	USB	2	0200h	USB Specification Release Number.
4	DeviceClass	1	09h	Class code assigned by USB-IF for Hubs.
5	DeviceSubClass	1	00h	Class code assigned by USB-IF for Hubs.
6	DeviceProtocol	1	01h	Protocol Code.
7	MaxPacketSize0	1	40h	64-byte packet size.
8	Vendor	2	user/ default	Vendor ID; Customer value defined in ROM or serial port load.
10	Product	2	user/ default	Product ID; Customer value defined in ROM or serial port load.
12	Device	2	user/ default	Device ID; Customer value defined in ROM or serial port load

TABLE 7-15: DEVICE DESCRIPTOR (CONTINUED)

Offset	Field	Size	Value	Description
14	Manufacturer	1	xxh	If STRING_EN =0 Optional string is not supported, and xx = 00. If STRING_EN = 1, String support is enabled, and xx = 01
15	Product	1	yyh	If STRING_EN =0 Optional string is not supported, and yy = 00. If STRING_EN = 1, String support is enabled, and yy = 02
16	SerialNumber	1	zzh	If STRING_EN =0 Optional string is not supported, and zz = 00. If STRING_EN = 1, String support is enabled, and zz = 03
17	NumConfigurations	1	01h	Supports 1 configuration.

7.4.2 DEVICE QUALIFIER DESCRIPTOR

The following table provides device qualifier values for Full-Speed operation.

TABLE 7-16: DEVICE QUALIFIER (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	0Ah	Size of this Descriptor.
1	DescriptorType	1	06h	Device Descriptor Type.
2	USB	2	0200h	USB Specification Release Number.
4	DeviceClass	1	09h	Class code assigned by USB-IF for Hubs.
5	DeviceSubClass	1	00h	Class code assigned by USB-IF for Hubs.
6	DeviceProtocol	1	00h	Protocol code.
7	MaxPacketSize0	1	40h	64-byte packet size for the other speed.
8	NumConfigurations	1	01h	Supports 1 other speed configuration.
9	Reserved	1	00h	Reserved.

7.4.3 CONFIGURATION DESCRIPTOR

The following table provides configuration descriptor values for High-Speed, Single-TT-Only operation.

TABLE 7-17: CONFIGURATION DESCRIPTOR (HIGH-SPEED, SINGLE-TT ONLY)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	02h	Configuration Descriptor Type.

TABLE 7-17: CONFIGURATION DESCRIPTOR (HIGH-SPEED, SINGLE-TT ONLY) (CONTINUED)

Offset	Field	Size	Value	Description
2	TotalLength	2	yyyyh	Total combined length of all descriptors for this configuration (configuration, interface, endpoint, and class- or vendor-specific). yyyyh = 0019h
4	NumInterfaces	1	01h	Number of interfaces supported by this configuration.
5	ConfigurationValue	1	01H	Value to use as an argument to the SetConfiguration() request to select this configuration.
6	Configuration	1	00h	Index of string descriptor describing this configuration (string not supported).
7	Attributes	1	user/ signal	Configuration characteristics: Communicates the capabilities of the hub regarding Remote Wake-up capability, and also reports the self-power status. In all cases, the value reported to the host always indicates that the hub supports Remote Wakeup. The value reported to the host is dependant upon the SELF_BUS_PWR bit (CONFIG_BYTE_1) = A0h for Bus-Powered (SELF_BUS_PWR = 0). = E0h for Self-Powered (SELF_BUS_PWR = 1). All other values are reserved.
8	MaxPower	1	user	Maximum Power Consumption of the Hub from VBUS when fully operational. This value includes all support circuitry associated with the hub (including an attached “embedded” peripheral if hub is part of a compound device), and is in 2mA increments. The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) is used to determine which of the values below are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: ‘MAX_PWR_BP’ if SELF_BUS_PWR = ‘0’ ‘MAX_PWR_SP’ if SELF_BUS_PWR = ‘1’ In all cases the reported value is sourced from the MAX POWER data field (for Self or Bus power) that was loaded by Internal Default, or serial port configuration.

7.4.4 INTERFACE DESCRIPTOR (SINGLE-TT)

The following table provides interface descriptor values for High-Speed, Single-TT operation.

TABLE 7-18: INTERFACE DESCRIPTOR (HIGH-SPEED, SINGLE-TT)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	04h	Interface Descriptor Type.

TABLE 7-18: INTERFACE DESCRIPTOR (HIGH-SPEED, SINGLE-TT) (CONTINUED)

Offset	Field	Size	Value	Description
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	00h	Value used to select this alternate setting for the interface.
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not including endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code.
7	InterfaceProtocol	1	00h	Single-TT.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.4.5 ENDPOINT DESCRIPTOR (SINGLE-TT)

The following table provides endpoint descriptor values for Single-TT operation.

TABLE 7-19: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, SINGLE-TT)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint’s attributes. (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	0Ch	Interval for polling endpoint for data transfers (Maximum Possible).

7.4.6 OTHER-SPEED CONFIGURATION DESCRIPTOR

The following table provides other-speed configuration descriptor values for Full-Speed operation.

TABLE 7-20: OTHER-SPEED CONFIGURATION DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	07h	Other-Speed Configuration Descriptor Type.
2	TotalLength	2	yyyyh	Total combined length of all descriptors for this configuration. yyyyh = 0019h
4	NumInterfaces	1	01h	Number of Interfaces supported by this configuration.
5	ConfigurationValue	1	01H	Value to use to select configuration.
6	Configuration	1	00h	Index of String Descriptor describing this configuration (string not supported).

TABLE 7-20: OTHER-SPEED CONFIGURATION DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
7	Attributes	1	user/ signal	Configuration characteristics: Communicates the capabilities of the hub regarding Remote Wake-up capability, and also reports the self-power status. In all cases, the value reported to the host always indicates that the hub supports Remote Wakeup. The value reported to the host is dependant upon the SELF_BUS_PWR bit (CONFIG_BYTE_1) = A0h for Bus-Powered (SELF_BUS_PWR = 0). = E0h for Self-Powered (SELF_BUS_PWR = 1). All other values are reserved.
8	MaxPower	1	user	Maximum Power Consumption of the Hub from VBUS when fully operational. This value includes all support circuitry associated with the hub (including an attached “embedded” peripheral if hub is part of a compound device), and is in 2mA increments. The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) are used to determine which of the values below are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: ‘MAX_PWR_BP’ if SELF_BUS_PWR = ‘0’ ‘MAX_PWR_SP’ if SELF_BUS_PWR = ‘1’ In all cases the reported value is sourced from the MAX POWER data field (for Self or Bus power) that was loaded by Internal Default, or serial port configuration.

7.4.7 INTERFACE DESCRIPTOR (FULL-SPEED)

The following table provides interface description values for Full-Speed operation.

TABLE 7-21: INTERFACE DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	04h	Interface Descriptor Type.
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	00h	Value used to select this alternate setting for the interface.
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not including endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code.
7	InterfaceProtocol	1	00h	Protocol code.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.4.8 ENDPOINT DESCRIPTOR (FULL-SPEED)

The following table provides endpoint descriptor values for Full-Speed operation.

TABLE 7-22: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint’s attributes (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	FFh	Interval for polling endpoint for data transfers (Maximum Possible).

7.5 Hub Attached as a High-Speed Device (Customer-Configured as Multi-TT Capable)

The following tables provide descriptor information for Customer-Configured Multi-TT High-Speed devices.

7.5.1 STANDARD DEVICE DESCRIPTOR

The following table provides device descriptor values for High-Speed operation.

TABLE 7-23: DEVICE DESCRIPTOR (HIGH-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	12	Size of this Descriptor
1	DescriptorType	1	01h	Device Descriptor Type.
2	USB	2	0200h	USB Specification Release Number.
4	DeviceClass	1	09h	Class code assigned by USB-IF for Hubs.
5	DeviceSubClass	1	00h	Class code assigned by USB-IF for Hubs.
6	DeviceProtocol	1	02h	Protocol code (Multi-TTs).
7	MaxPacketSize0	1	40h	64-byte packet size.
8	Vendor	2	user	Vendor ID; Customer value defined in ROM or serial port load.
10	Product	2	user	Product ID; Customer value defined in ROM or serial port load.
12	Device	2	user	Device ID; Customer value defined in ROM or serial port load.
14	Manufacturer	1	xxh	If STRING_EN =0 Optional string is not supported, and xx = 00. If STRING_EN = 1, String support is enabled, and xx = 01

TABLE 7-23: DEVICE DESCRIPTOR (HIGH-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
15	Product	1	yyh	If STRING_EN =0 Optional string is not supported, and yy = 00. If STRING_EN = 1, String support is enabled, and yy = 02
16	SerialNumber	1	zzh	If STRING_EN =0 Optional string is not supported, and zz = 00. If STRING_EN = 1, String support is enabled, and zz = 03
17	NumConfigurations	1	01h	Supports 1 configuration.

7.5.2 DEVICE QUALIFIER DESCRIPTOR

The following table provides device qualifier values for Full-Speed operation.

TABLE 7-24: DEVICE QUALIFIER (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	0Ah	Size of this Descriptor.
1	DescriptorType	1	06h	Device Descriptor Type.
2	USB	2	0200h	USB Specification Release Number.
4	DeviceClass	1	09h	Class code assigned by USB-IF for Hubs.
5	DeviceSubClass	1	00h	Class code assigned by USB-IF for Hubs.
6	DeviceProtocol	1	00h	Protocol code.
7	MaxPacketSize0	1	40h	64-byte packet size for the other speed.
8	NumConfigurations	1	01h	Supports 1 other speed configuration.
9	Reserved	1	00h	Reserved.

7.5.3 CONFIGURATION DESCRIPTOR

The following table provides configuration descriptor values for High-Speed operation.

TABLE 7-25: CONFIGURATION DESCRIPTOR (HIGH-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	02h	Configuration Descriptor Type.
2	TotalLength	2	yyyyh	Total combined length of all descriptors for this configuration (configuration, interface, endpoint, and class- or vendor-specific). yyyyh = 0029h.
4	NumInterfaces	1	01h	Number of Interface supported by this configuration.

TABLE 7-25: CONFIGURATION DESCRIPTOR (HIGH-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
5	ConfigurationValue	1	01H	Value to use as an argument to the SetConfiguration() request to select this configuration.
6	Configuration	1	00h	Index of string descriptor describing this configuration (String not supported).
7	Attributes	1	user/ signal	Configuration characteristics: Communicates the capabilities of the hub regarding Remote Wake-up capability, and also reports the self-power status. In all cases, the value reported to the host always indicates that the hub supports Remote Wakeup. The value reported to the host is dependant upon the SELF_BUS_PWR bit (CONFIG_BYTE_1) = A0h for Bus-Powered (SELF_BUS_PWR = 0). = E0h for Self-Powered (SELF_BUS_PWR = 1). All other values are reserved.
8	MaxPower	1	user	Maximum Power Consumption of the Hub from VBUS when fully operational. This value includes all support circuitry associated with the hub (including an attached “embedded” peripheral if hub is part of a compound device), and is in 2mA increments. The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) is used to determine which of the values below are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: ‘MAX_PWR_BP’ if SELF_BUS_PWR = ‘0’ ‘MAX_PWR_SP’ if SELF_BUS_PWR = ‘1’ In all cases the reported value is sourced from the MAX POWER data field (for Self or Bus power) that was loaded by Internal Default, or serial port configuration.

7.5.4 INTERFACE DESCRIPTOR (SINGLE-TT)

The following table provides interface descriptor values for High-Speed Single-TT operation.

TABLE 7-26: INTERFACE DESCRIPTOR (HIGH-SPEED, SINGLE-TT)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	04h	Interface Descriptor Type.
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	00h	Value used to select this alternate setting for the interface.

TABLE 7-26: INTERFACE DESCRIPTOR (HIGH-SPEED, SINGLE-TT)

Offset	Field	Size	Value	Description
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not including endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code
7	InterfaceProtocol	1	01h	Single-TT.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.5.5 ENDPOINT DESCRIPTOR (SINGLE-TT)

The following table provides endpoint descriptor values for Single-TT operation.

TABLE 7-27: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, SINGLE-TT)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint’s attributes. (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	0Ch	Interval for polling endpoint for data transfers (Maximum Possible).

7.5.6 INTERFACE DESCRIPTOR (MULTI-TT)

The following table provides interface descriptor values for High-Speed Multi-TT operation.

TABLE 7-28: INTERFACE DESCRIPTOR (MULTI-TT, HIGH-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	04h	Interface Descriptor Type.
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	01h	Value used to select this alternate setting for the inter-face.
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not includ-ing endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code.

TABLE 7-28: INTERFACE DESCRIPTOR (MULTI-TT, HIGH-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
7	InterfaceProtocol	1	02h	Multiple-TTs.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.5.7 ENDPOINT DESCRIPTOR (MULTI-TT)

The following table provides endpoint descriptor values for Multi-TT operation.

TABLE 7-29: ENDPOINT DESCRIPTOR (FOR STATUS CHANGE ENDPOINT, MULTI-TT)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint’s attributes. (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	0Ch	Interval for polling endpoint for data transfers (Maximum Possible).

7.5.8 OTHER-SPEED CONFIGURATION DESCRIPTOR

The following table provides other-speed configuration descriptor values for Full-Speed operation.

TABLE 7-30: OTHER-SPEED CONFIGURATION DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	07h	Other-Speed Configuration Descriptor Type.
2	TotalLength	2	yyyyh	Total combined length of all descriptors for this configu-ration. yyyyh = 0019h
4	NumInterfaces	1	01h	Number of interfaced described by this configuration.
5	ConfigurationValue	1	01h	Value to use to select configuration.
6	Configuration	1	00h	Index of String Descriptor describing this configuration (string not supported).

TABLE 7-30: OTHER-SPEED CONFIGURATION DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
7	Attributes	1	user/ signal	Configuration characteristics: Communicates the capabilities of the hub regarding Remote Wake-up capability, and also reports the self-power status. In all cases, the value reported to the host always indicates that the hub supports Remote Wakeup. The value reported to the host is dependant upon the SELF_BUS_PWR bit (CONFIG_BYTE_1) = A0h for Bus-Powered (SELF_BUS_PWR = 0). = E0h for Self-Powered (SELF_BUS_PWR = 1). All other values are reserved.
8	MaxPower	1	user	Maximum Power Consumption of the Hub from VBUS when fully operational. This value includes all support circuitry associated with the hub (including an attached “embedded” peripheral if hub is part of a compound device), and is in 2mA increments. The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) is used to determine which of the values below are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: ‘MAX_PWR_BP’ if SELF_BUS_PWR = ‘0’ ‘MAX_PWR_SP’ if SELF_BUS_PWR = ‘1’ In all cases the reported value is sourced from the MAX POWER data field (for Self or Bus power) that was loaded by Internal Default or serial port configuration.

7.5.9 INTERFACE DESCRIPTOR (FULL-SPEED)

The following table provides interface descriptor values for Full-Speed operation.

TABLE 7-31: INTERFACE DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	04h	Interface Descriptor Type.
2	InterfaceNumber	1	00h	Number of this interface.
3	AlternateSetting	1	00h	Value used to select this alternate setting for the interface.
4	NumEndpoints	1	01h	Number of endpoints used by this interface (not including endpoint 0).
5	InterfaceClass	1	09h	Hub class code.
6	InterfaceSubclass	1	00h	Subclass code.

TABLE 7-31: INTERFACE DESCRIPTOR (FULL-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
7	InterfaceProtocol	1	00h	Protocol code.
8	Interface	1	00h	Index of the string descriptor describing this interface (strings not supported).

7.5.10 ENDPOINT DESCRIPTOR (FULL-SPEED)

The following table provides endpoint descriptor values for Full-Speed operation.

TABLE 7-32: ENDPOINT DESCRIPTOR (FULL-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	07h	Size of this Descriptor.
1	DescriptorType	1	05h	Endpoint Descriptor Type.
2	EndpointAddress	1	81h	The address of the endpoint on the USB device.
3	Attributes	1	03h	Describes the endpoint's attributes (interrupt only, no synchronization, data endpoint).
4	MaxPacketSize	2	0001h	Maximum packet size for this endpoint.
6	Interval	1	FFh	Interval for polling endpoint for data transfers (Maximum Possible).

7.6 Class-Specific Hub Descriptor

The following table provides class-specific Hub descriptor values for Full-Speed and High-Speed operation.

Note: The Hub must respond to Hub Class Descriptor type 29h (the USB 1.1 and USB 2.0 value) and 00h (the USB 1.0 value).

TABLE 7-33: CLASS-SPECIFIC HUB DESCRIPTOR (FULL-SPEED & HIGH-SPEED)

Offset	Field	Size	Value	Description
0	Length	1	09h	Size of this Descriptor.
1	DescriptorType	1	29h	Hub Descriptor Type.

TABLE 7-33: CLASS-SPECIFIC HUB DESCRIPTOR (FULL-SPEED & HIGH-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
2	NbrPorts	1	user	Number of downstream facing ports this Hub supports. See Section 11.23.2.1 of the USB Specification for additional details regarding the use of this field. The value reported is implementation dependent, and is derived from the value defined during Internal Default, or serial port load. The PORT_DIS_SP field defines the ports that are permanently disabled when in Self-Powered operation, and the PORT_DIS_BP field defines the ports that are permanently disabled when in Bus-Powered operation. Internal logic will subtract the number of ports which are disabled, from the total number available (which is 3), and will report the remainder as the number of ports supported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The field used to determine the value that is reported to the host will be: ‘PORT_DIS_BP’ if SELF_BUS_PWR = ‘0’ ‘PORT_DIS_SP’ if SELF_BUS_PWR = ‘1’
3	HubCharacteristics	2	user	Defines support for Logical power switching mode, Compound Device support, Over-current protection, TT Think Time, and Port Indicator support, See Section 11.23.2.1 in the USB Specification for additional details regarding the use of this field. The values delivered to a host are all derived from values defined during Internal Default, or serial port load, and are assigned as follows: D1:0 = ‘00’b if PORT_PWR = ‘0’ D1:0 = ‘01’b if PORT_PWR = ‘1’ D2 = ‘COMPOUND’ D4:3 = ‘CURRENT_SNS’ D6:5 = ‘00’b for 8FS (max) bit times of TT think time. D7 = hardcoded to ‘0’ (no Port Indicator Support) D15:8 = ‘00000000’b
5	PwrOn2PwrGood	1	user	Time (in 2 ms intervals) from the time the power-on sequence begins on a port until power is good on that port. See Section 11.23.2.1 in the USB Specification. The value contained in the ‘POWER_ON_TIME’ field is directly reported to the host, and is determined by Internal Default, or serial port load.

TABLE 7-33: CLASS-SPECIFIC HUB DESCRIPTOR (FULL-SPEED & HIGH-SPEED) (CONTINUED)

Offset	Field	Size	Value	Description
6	HubContrCurrent	1	user	Maximum current requirements of the Hub Controller electronics in 1 mA increments. See Section 11.23.2.1 in the USB Specification for additional details on the use of this field. This field reports the maximum current that only the hub consumes from upstream VBUS when fully operational. This value includes all support circuitry associated with the hub (but does not include the current consumption of any permanently attached peripherals if the hub is part of a compound device). The Hub supports Self-Powered and Bus-Powered operation. The SELF_BUS_PWR bit (CONFIG_BYTE_1) defined in Section 5.3.7, "Register 06h: CONFIG_BYTE_1 - CFG1," on page 31 is used to determine which of the stored values are reported. The value reported to the host must coincide with the current operating mode, and will be determined by the following rules. The value that is reported to the host will be: 'HC_MAX_C_BP' if SELF_BUS_PWR = '0' 'HC_MAX_C_SP' if SELF_BUS_PWR = '1' 'HC_MAX_C_BP/SP' are defined in Section 5.3.15, and Section 5.3.16, "Register 0Fh: Hub Controller Max Current For Bus Powered Operation - HCMCB," on page 36. In all cases the reported value is sourced from the Hub Controller Max Current data field (for Self or Bus power) that was determined by Internal Default, or serial port load.
7	DeviceRemovable	1	user	Indicates if port has a removable device attached. See Section 11.23.2.1 in the USB Specification. The value contained in the 'NR_DEVICE' field is directly reported to the host, and is determined by Internal Default, or serial port load.
8	PortPwrCtrlMask	1	FFh	Field for backwards USB 1.0 compatibility.

7.7 String Descriptors

The USB3803 supports a 30 Character Manufacturer String Descriptor, a 30 Character Product String and a 30 character Serial String.

7.7.1 STRING DESCRIPTOR ZERO (SPECIFIES LANGUAGES SUPPORTED)

TABLE 7-34: STRING DESCRIPTOR ZERO

Offset	Field	Size	Value	Description
0	Length	1	04h	Size of this Descriptor.
1	DescriptorType	1	03h	String Descriptor Type.
2	LANGID	2	xxxxh	Language ID code from LANG_ID_H and LANG_ID_L registers

7.7.2 STRING DESCRIPTOR 1 (MANUFACTURER STRING)

TABLE 7-35: STRING DESCRIPTOR 1, MANUFACTURER STRING

Offset	Field	Size	Value	Description
0	Length	1	yyh	Size of this Descriptor. The yy value is created by taking the MFR_STR_LEN{bytes} + 2{bytes}
1	DescriptorType	1	03h	String Descriptor Type.
2	String	N	string	Manufacturer String The string is located in the MFR_STR register and the size (N) is held in the MFR_STR_LEN register

7.7.3 STRING DESCRIPTOR 2 (PRODUCT STRING)

TABLE 7-36: STRING DESCRIPTOR 2, PRODUCT STRING

Offset	Field	Size	Value	Description
0	Length	1	yyh	Size of this Descriptor. The yy value is created by taking the PRD_STR_LEN{bytes} + 2{bytes}
1	DescriptorType	1	03h	String Descriptor Type.
2	String	N	string	Product String The string is located in the PROD_STR register and the size (N) is held in the PRD_STR_LEN register

7.7.4 STRING DESCRIPTOR 3 (SERIAL STRING)

TABLE 7-37: STRING DESCRIPTOR 3, SERIAL STRING

Offset	Field	Size	Value	Description
0	Length	1	yyh	Size of this Descriptor. The yy value is created by taking the SER_STR_LEN{bytes} + 2{bytes}
1	DescriptorType	1	03h	String Descriptor Type.
2	String	N	string	Serial String The string is located in the SER_STR register and the size (N) is held in the SER_STR_LEN register

8.0 BATTERY CHARGING

8.1 Upstream Battery Charger Detection

Battery Charger Detection is available on the upstream facing port. The detection sequence is intended to identify chargers which conform to the Chinese battery charger specification, chargers which conform to the USB-IF Battery Charger Specification 1.1.

DP and DM are high impedance when the charger detection block is disabled.

The device includes the circuitry required to implement battery charging detection using the Battery Charging Specification. The device will automatically perform charger detection upon entering the Hub.ChgDet stage in Hub Mode. The device includes a state machine to provide the detection of the USB chargers listed in the table below. The type of charger detected is returned in the ChargerType bits in the Battery Charger Detection Register.

TABLE 8-1: CHARGERS COMPATIBLE WITH UPSTREAM DETECTION

USB ATTACH TYPE	DP/DM PROFILE	CHARGERTYPE
DCP (Dedicated Charging Port)	Shorted < 200ohm	001
CDP (Charging Downstream Port)	VDP reflected to VDM	010 (EnhancedChrgDet = 1)
SDP (Standard Downstream Port) USB Host or downstream hub port	15Kohm pull-down on DP and DM	011

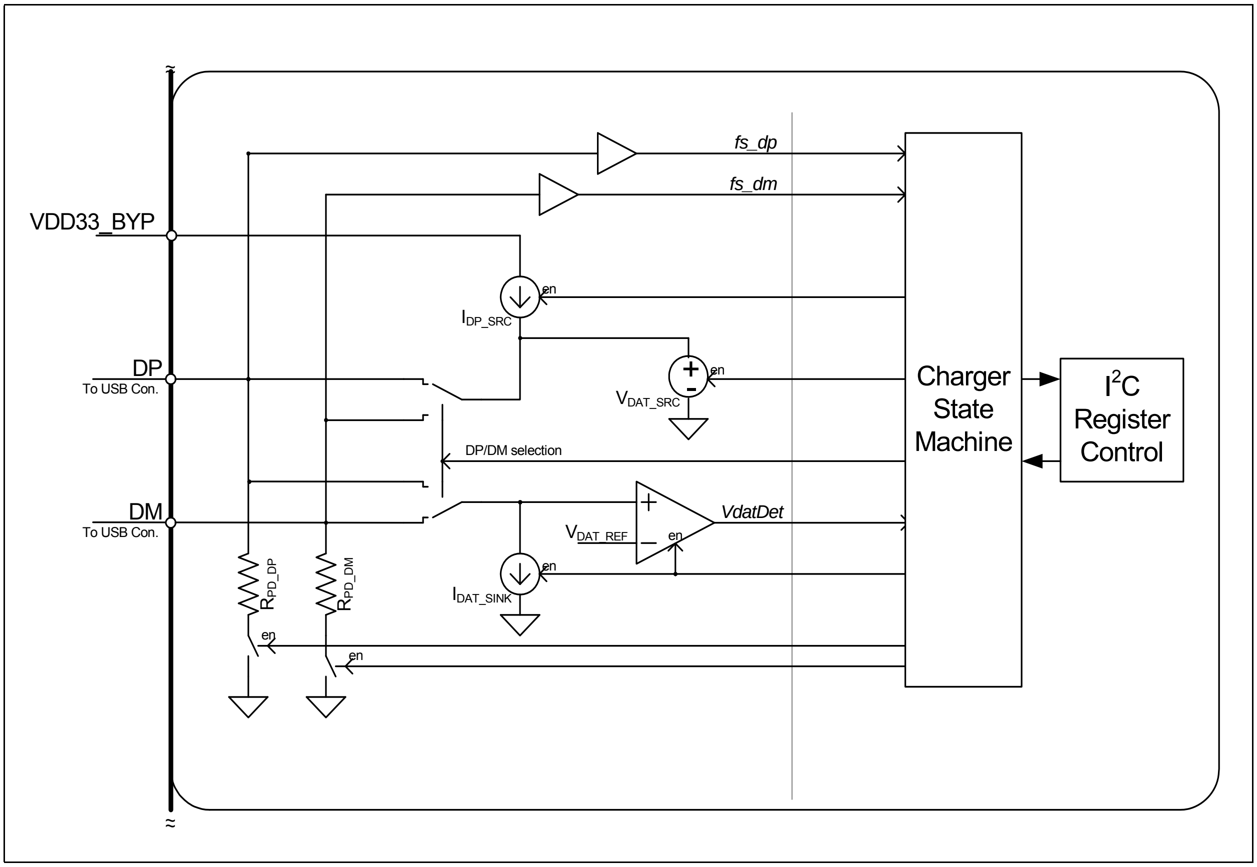
The device will automatically begin a charger detection when Hub.ChgDet stage in Hub Mode is entered. The device will provide feedback to the system through the serial port registers and the INT_Npin.

The following sections detail the sequence followed for battery charger detection.

8.1.1 CHARGER DETECTION CIRCUITRY

The charger detection circuitry shown in Figure 8-1 is used to detect the type charger attached to the upstream USB connector.

FIGURE 8-1: UPSTREAM BATTERY CHARGER DETECTION CIRCUITRY

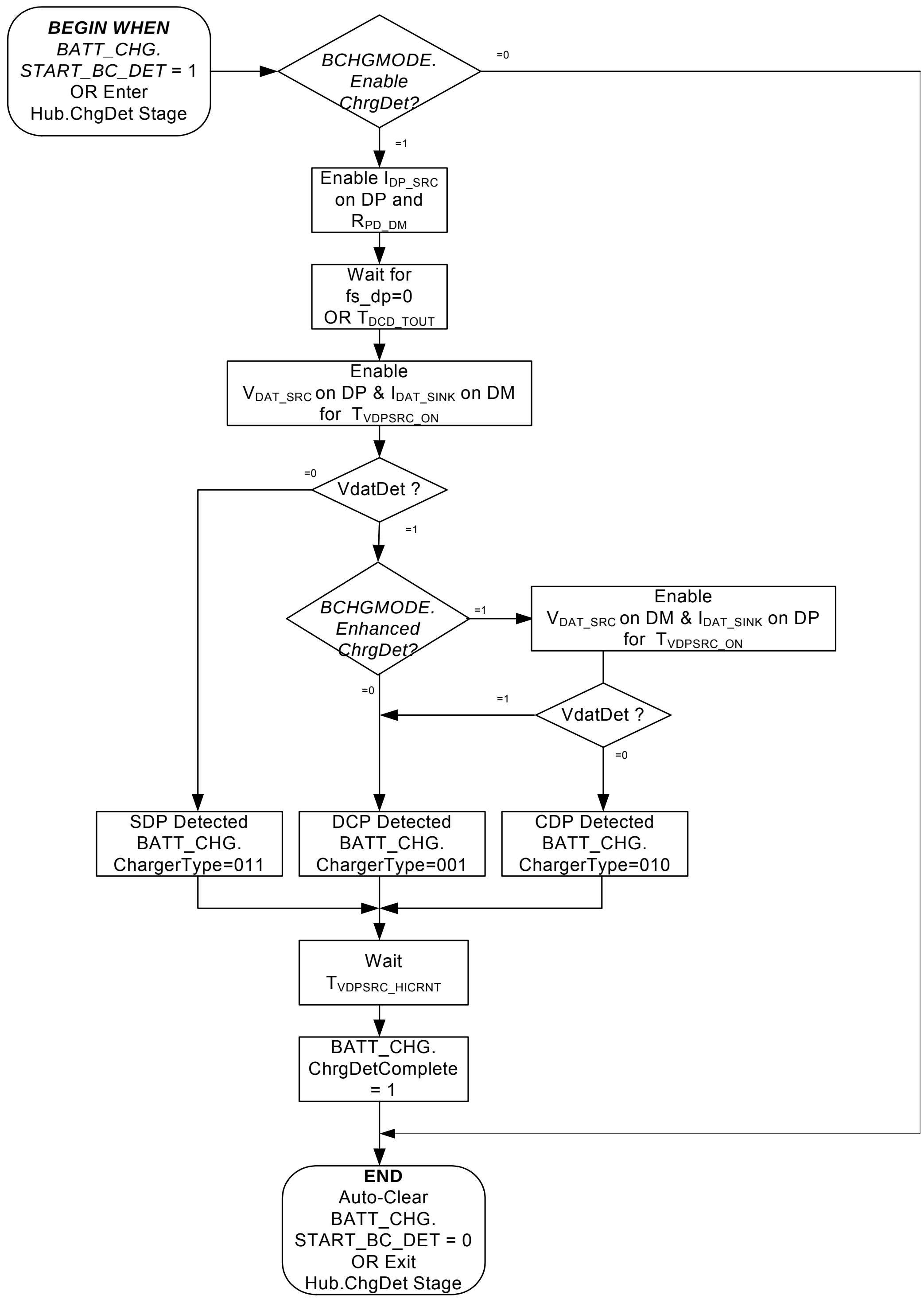


8.1.2 AUTOMATIC CHARGER DETECTION

In order to detect the charger, the device applies and monitors voltages on the USBUP_DP and USBUP_DM pins. If a voltage within the specified range is detected, the Charger Detection Register in the I^2C register space shall be updated to reflect the proper status.

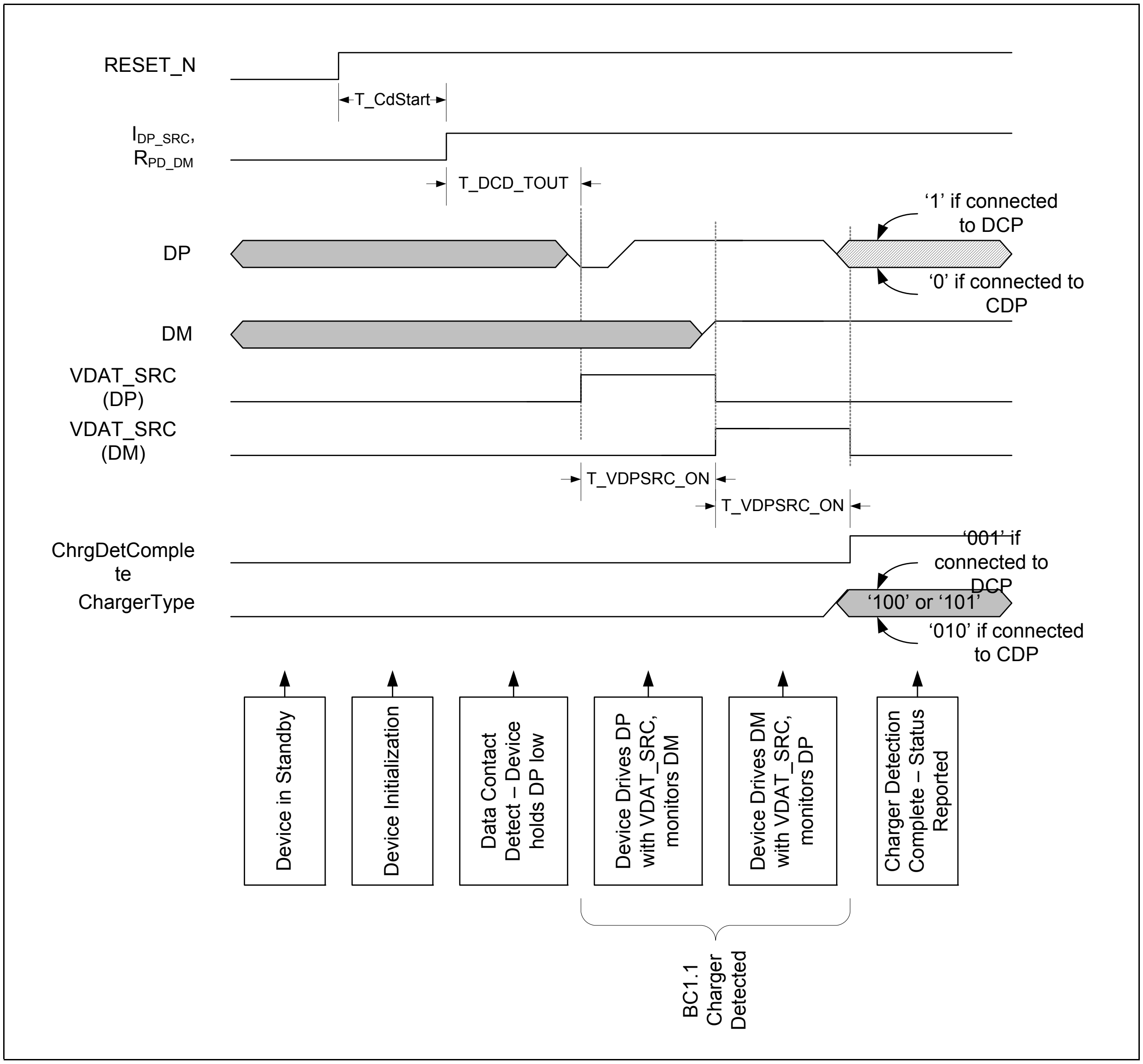
The flowchart in Figure 8-2 details the charger detection sequence and the ability of the configuration settings to control it.

FIGURE 8-2: FLOWCHART FOR BATTERY CHARGING DETECTION SEQUENCE



The diagram in Figure 8-3 illustrates automatic Battery Charging detection when enhanced battery charger detection is enabled. A USB Battery Charging 1.1 charger is discovered and the charger detection sequence continues in order to differentiate between a Dedicated Charging Port and a Charging Downstream Port.

FIGURE 8-3: ENHANCED CHARGER DETECTION TIMING - BC1.1



8.1.3 BATTERY CHARGER TIMING

Table 8-2 specifies timing parameters for the battery charging sequence.

TABLE 8-2: BATTERY CHARGING TIMING PARAMETERS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Charger Detection Start Time delay	$T_{CDSTART}$		$T_{hubinit}$ + $T_{hubconfig}$		mS	See Table 4-2
Data Contact Detect Time-out	T_{DCD_TOUT}	199	200	204	mS	HUB.ChgDet stage on pll

TABLE 8-2: BATTERY CHARGING TIMING PARAMETERS

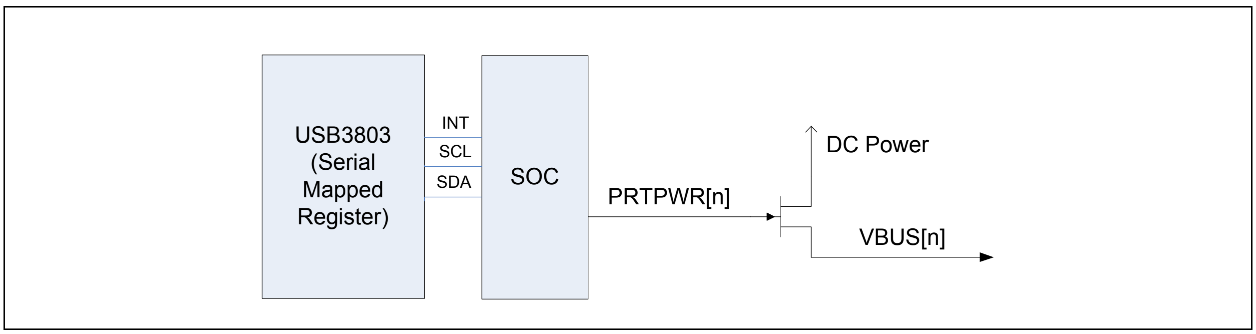
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Vdat_src and Idat_sink Enable Time	T_{VDPSRC_ON}	79	80	84	mS	HUB.ChgDet stage on pll
Delay from Vdat_det to end of detection sequence	T_{VDPSRC_HICRNT}	79	80	83	mS	HUB.ChgDet stage on pll
Charger Detection Exit time when disabled	$T_{VLO\_RELEASE}$	49	50	55	mS	HUB.ChgDet stage on pll

8.2 Downstream Port Battery Charging Support

The USB3803 can configure any of the downstream ports to support battery charger handshake.

The Hub's role in downstream battery charging is to provide an acknowledge to a device's query as to if the hub *system* supports USB battery charging. The hub *silicon* does not provide any current or power FETs or any such thing to actually charge the device. Those components would need to be provided as external components in the final Hub board design.

FIGURE 8-4: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the final Hub board design provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply to the device. This indication is on a per/ port basis. i.e. the board can configure two ports to support battery charging (thru high current power FET's) and leave the other port as a standard USB port.

8.2.1 USB BATTERY CHARGING

In the terminology of the USB battery charging specification, if the port is configured to support battery charging, the downstream port is a "Charging Host Port". All AC/DC characteristics will comply with only this type. If the port is not configured to support battery charging, the port is a "Standard Host Port". AC/DC characteristics comply with the USB 2.0 specification.

A downstream port will only behave as a "Charging Host Port" or a "Standard Host Port". The port will not switch between "Charging Host Port" or Standard Host Port" at any time after initial power-up and configuration.

8.2.2 SPECIAL BEHAVIOR OF PRTPWR REGISTER BITS

The USB Battery charging specification does not address system issues. It only defines a low level protocol for a device and host (or hub) to communicate a simple question and optional answer.

Device queries "do you support battery charging?"

Host answers "yes, I do support battery charging" or does not answer at all. There is no negative response. (A lack of response is taken as a negative response)

When ports are configured for downstream battery charging, the corresponding PRTPWR setting will be controlled by downstream battery charging logic instead of the normal hub logic.

PRTPWR setting will assert after initial hub customer configuration (Internal default/Serial register writes). PRTPWR will remain asserted and under the control of the battery charge logic until one of two events.

1. An overcurrent is detected on the corresponding OCS_N bit. In this case, PRTPWR setting will negate. The only way to re-enable the PRTPWR bit from this state is to RESET the USB3803.
2. The hub enters Hub.Communication stage, connects on its upstream port and is enumerated by a USB host. In this case control over the PRTPWR setting reverts back to the hub logic inside the USB3803 and the normal USB behavior applies. i.e the host must enable PRTPWR.

Since the enumeration process for a hub sets the PORT_POWER feature for all downstream ports, this information can be used to switch control over the PRTPWR register between the battery charge logic and the hub logic.

- When the Hub PORT_POWER feature is ‘1’, the hub logic controls the PRTPWR bits.
- When the Hub PORT_POWER feature is ‘0’, the battery charging logic controls the PRTPWR bits.

No matter which controller is controlling the PRTPWR register bits, an overcurrent event will always negate PRTPWR register bit.

8.2.3 BATTERY CHARGING CONFIGURATION

Configuration of ports to support battery charging is done through serial port configuration load.

Register D0: Downstream Battery Charging Enable - BC_EN is allocated for Battery Charging support. The register, starting from Bit 1, enables Battery charging for each down stream port when asserted. Bit 1 represents port 1 and so on. Each port with battery charging enabled asserts the corresponding PRTPWR register bit.

9.0 INTEGRATED POWER REGULATORS

9.1 Overview

The integrated power regulators are defined to provide significant flexibility to the system in providing power the device. Several different configurations are allowed in order to align the power structure to supplies available in the system.

9.1.1 3.3V REGULATOR

The device has an integrated regulator to convert from VBAT to 3.3V.

9.1.2 1.2V REGULATOR

The device has an integrated regulator to convert from a variable voltage input on VDD_CORE_REG to 1.2V. The 1.2V regulator shall be tolerant to the presence of low voltage (~0V) on the VDD_CORE_REG pin in order to support system power solutions where a 1.8V supply is not always present in low power states.

The 1.2V regulator shall support an input voltage range consistent with a 1.8V input in order to reduce power consumption in systems which provide multiple power supply levels. In addition the 1.2V regulator shall support an input voltage up to 3.3V for systems which provide only a single power supply. The device will support operation where the 3.3V regulator output can drive the 1.2V regulator input such that VBAT is the only required supply.

9.2 Power Configurations

The USB3803 support operation with no back current when power is connected in each of the following configurations.

9.2.1 SINGLE SUPPLY CONFIGURATIONS

9.2.1.1 VBAT Only

VBAT should be tied to the VBAT system supply. VDD33_BYP regulator output and VDD_CORE_REG should be tied together on the board. In this configuration the 3.3v regulator will be active, and the 3.3v to 1.2v regulator will be active.

9.2.1.2 3.3V Only

VBAT should be tied to the 3.3v system supply. VDD33_BYP and VDD_CORE_REG pins should be tied together on the board. In this configuration the 3.3v regulator will operate in dropout. The 1.2v regulator will be active.

9.2.2 DOUBLE SUPPLY CONFIGURATIONS

9.2.2.1 VBAT + 1.8V

VBAT should be tied to the VBAT system supply. VDD33_BYP regulator output requires external capacitor. VDD_CORE_REG should be tied to the 1.8v system supply. In this configuration the 3.3v regulator and the 1.2V regulator will be active.

9.2.2.2 3.3V + 1.8V

VBAT should be tied to the 3.3v system supply. VDD33_BYP should be connected to the 3.3v external capacitor. VDD_CORE_REG should be tied to the 1.8v system supply. In this configuration the 3.3v regulator will operate in dropout. The 1.2v regulator will be active.

9.3 Regulator Control Signals

The regulators are controlled by the **RESET_N** and **BYPASS_N** signals. When **RESET_N** is brought high the VDD33 regulator will turn on. When RESET_N is brought low the VDD33 regulator will turn off. When **BYPASS_N** is brought high the VDD12 regulator will turn on. When **BYPASS_N** is brought low the VDD12 regulator will turn off.

BYPASS_N should not be driven high if **RESET_N** is driven low.

10.0 SPECIFICATIONS

10.1 Absolute Maximum Ratings

TABLE 10-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Units
VBAT	V_{BAT}		-0.5	5.5	V
VDD_CORE_REG	$V_{DD\_CORE\_REG}$		-0.5	4.6	V
VDD33	V_{DD33_BYP}		-0.5	4.6	V
Maximum IO Voltage to Ground	V_{IO}		-0.5	4.6	V
REFCLK Voltage	V_{MAX_REFCLK}		-0.5	3.6	V
Voltage on USB+ and USB- pins	V_{MAX_USB}		-0.5	5.5	V
Operating Temperature	T_{MAX_OP}	Commercial	0	70	C
Operating Temperature	T_{MAX_OP}	Industrial	-40	85	C
Storage Temperature	T_{MAX_STG}		-55	150	C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

10.2 Recommended Operating Conditions

TABLE 10-2: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VBAT	V_{BAT}		2.9		5.5	V
VDD_CORE_REG	$V_{DD\_CORE\_REG}$	Note 1	1.6	1.8	2.0	V
VDD_CORE_REG	$V_{DD\_CORE\_REG}$	Note 2	3.0	3.3	3.6	V
Input Voltage on I/O Pins	V_I		-0.3	1.8	3.6	V
Input Voltage (**DP**, **DM)**	V_{IUSB}		-0.3		5.5	V
Voltage on **REFCLK**	V_{REFCLK}		-0.3		3.6	V
Ambient Temperature	T_A	Commercial	0		70	C
Ambient Temperature	T_A	Industrial	-40		85	C

Note 1: Applicable only when **VDD_CORE_REG** is supplied from external power supply.

2: Applicable only when **VDD_CORE_REG** is tied to **VDD33_BYP**.

10.3 Operating Current

The following conditions are assumed unless otherwise specified:

V_{BAT} = 3.0 to 5.5V; V_{DD_CORE} = 1.6 to 2.0V; V_{SS} = 0V;

T_A = 0C to +70C (Commercial), -40C to +85C (Industrial)

TABLE 10-3: OPERATING CURRENT (DUAL SUPPLY)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High Speed USB Operation	$I_{VBAT(HS)}$	Active USB Transfer **RESET_N =** 1**BYPASS_N =**1 3 Downstream Ports Active	67	69	72	mA
	$I_{CORE(HS)}$		29	31	35	mA
High Speed USB Operation	$I_{VBAT(HS)}$	Active USB Transfer **RESET_N =** 1**BYPASS_N =**1 2 Downstream Ports Active, 1 Port Disabled	46	49	50	mA
	$I_{CORE(HS)}$		26	28	31	mA
High Speed USB Operation	$I_{VBAT(HS)}$	Active USB Transfer **RESET_N =** 1**BYPASS_N =**1 1Downstream Ports Active, 2 Ports Disabled	24	25	28	mA
	$I_{CORE(HS)}$		22	24	28	mA
High Speed USB Operation	$I_{VBAT(HS)}$	High Speed Idle **RESET_N =** 1**BYPASS_N =**1 3 Downstream Ports Enabled, No USB Data Transfer (Idle)	24	25	27	mA
	$I_{CORE(HS)}$		24	25	28	mA
Unconfigured (High Speed)	$I_{VBAT(UNCONF)}$	**RESET_N** = 1 **BYPASS_N=** 1	12	13	14	mA
	$I_{CORE(UNCONF)}$		17	18	22	mA
Hub Bypass	$I_{VBAT(BYP)}$	**RESET_N** = 1 **BYPASS_N** = 0 Commercial Temp	26	36	60	uA
	$I_{CORE(BYP)}$		0	0	3	uA
STANDBY Mode	$I_{VBAT(STDBY)}$	**RESET_N** = 0 Commercial Temp	0	0.4	3.5	µA
	$I_{CORE(STDBY)}$		0	0	2	µA
Hub Bypass	$I_{VBAT(BYP)}$	**RESET_N** = 1 **BYPASS_N** = 0 Industrial Temp	26	36	60	uA
	$I_{CORE(BYP)}$		0	0	10	uA
STANDBY Mode	$I_{VBAT(STDBY)}$	**RESET_N** = 0 Industrial Temp	0	0.4	3.5	µA
	$I_{CORE(STDBY)}$		0	0	9	µA
SUSPEND Mode	$I_{VBAT(SPND)}$	**USB Suspend**	205	230	290	µA
	$I_{CORE(SPND)}$		35	65	385	µA

The following conditions are assumed unless otherwise specified:

V_{BAT} = 3.0 to 5.5V; V_{SS} = 0V; T_A = 0C to +70C (Commercial), -40C to +85C (Industrial)

TABLE 10-4: OPERATING CURRENT (SINGLE SUPPLY)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High Speed USB Operation	$I_{VBAT(HS)}$	Active USB Transfer **RESET_N** = 1 **BYPASS_N** =1 3 Downstream Ports Active	95	102	105	mA
High Speed USB Operation	$I_{VBAT(HS)}$	Active USB Transfer **RESET_N** = 1 **BYPASS_N** =1 2 Downstream Ports Active, 1 Port Disabled	73	77	82	mA
High Speed USB Operation	$I_{VBAT(HS)}$	Active USB Transfer **RESET_N** = 1 **BYPASS_N** =1 1 Downstream Port Active, 2 Ports Disabled	47	50	53	mA
High Speed USB Operation	$I_{VBAT(HS)}$	High Speed Idle **RESET_N** = 1**BYPASS_N** =1 3 Downstream Ports Enabled, No USB Data Transfer (Idle)	49	52	55	mA
Unconfigured (High Speed)	$I_{VBAT(UNCONF)}$	**RESET_N** = 1 **BYPASS_N**= 1	32	34	37	mA
Hub Bypass	$I_{VBAT(BYP)}$	**RESET_N** = 1 **BYPASS_N** = 0 Commercial Temp	26	28	68	uA
STANDBY Mode	$I_{VBAT(STDBY)}$	**RESET_N** = 0 Commercial Temp	0	0.6	2.4	µA
Hub Bypass	$I_{VBAT(BYP)}$	**RESET_N** = 1 **BYPASS_N** = 0 Industrial Temp	25	28	75	uA
STANDBY Mode	$I_{VBAT(STDBY)}$	**RESET_N** = 0 Industrial Temp	0	0.6	4.1	µA
SUSPEND Mode	$I_{VBAT(SPND)}$	**USB Suspend**	220	300	600	µA

10.4 DC Characteristics: Digital I/O Pins

Note: T_A = -40˚C to 85˚C

TABLE 10-5: DIGITAL I/O CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low-Level Input Voltage	V_{IL}	Note 3	-0.3		0.42	V
Low-Level Input Voltage	V_{IL}	Note 4	-0.3		0.34	V

TABLE 10-5: DIGITAL I/O CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}		1.25		VDD33_BYP + 0.3V	V
Low-Level Input Voltage **REFCLK**	V_{IL_REF}		-0.3		0.5	V
High-Level Input Voltage **REFCLK**	V_{IH_REF}		1.4			V
Clock Input Capacitance **REFCLK**	C_{IN}				2	pF
Low-Level Output Voltage	V_{OL}	@ I_{OL}=12mA sink current			0.4	V
Pin Capacitance	Cpin			2	20	pF
Output Current Capability	I_O		12	20	24	mA

Note:

3: For I2C interface using pullups to less than 2.1V.

4: For I2C interface using pullups to greater than 2.1V.

10.5 DC Characteristics: Analog I/O Pins

TABLE 10-6: DC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LS/FS FUNCTIONALITY						
Input Levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33_BYP}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
Termination						

TABLE 10-6: DC CHARACTERISTICS: ANALOG I/O PINS (DP/DM) (CONTINUED)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Driver Output Impedance for HS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 5	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 5	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	R_{PD}	Note 5	14.25	16.9	20	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}		100		150	mV
HS Disconnect Threshold	V_{HSDSC}		525		625	mV
Output Levels						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	µA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note:

5: The resistor value follows the 27% Resistor ECN published by the USB-IF.

10.6 Dynamic Characteristics: Digital I/O Pins

TABLE 10-7: DYNAMIC CHARACTERISTICS: DIGITAL I/O PINS (RESET_N)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum Active Low Pulse on **RESET_N**	T_{RESET}	**RESET_N =** ‘0’	100			µs

10.7 Dynamic Characteristics: Analog I/O Pins

TABLE 10-8: DYNAMIC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
FS Output Driver Timing						
FS Rise Time	T_{FR}	C_L = 50pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$	4		20	ns
FS Fall Time	T_{FF}	C_L = 50pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	T_{FRFM}	Excluding the first transition from IDLE state	90		111.1	%
LS Output Driver Timing						
LS Rise Time	T_{LR}	C_L = 50-600pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$	75		300	ns
LS Fall Time	T_{LF}	C_L = 50-600pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$	75		300	ns
Differential Rise/Fall Time Matching	T_{LRFM}	Excluding the first transition from IDLE state	80		125	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
High Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

10.8 USB Bypass Switch Characteristics

TABLE 10-9: ANALOG SWITCH CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
"ON" Resistance	R_{ON}	$0 < V_{switch} < V_{DD33\_BYP,}$ BYPASS_N = '0', RESET_N='1'	4	5	12	Ω
"OFF" Resistance	R_{OFF}	$0 < V_{switch} < V_{DD33\_BYP}$ BYPASS_N='1', RESET_N='1'	5	6	8	MΩ
Standby Resistance	R_{STDBY}	$0 < V_{switch} < V_{DD33\_BYP}$ RESET_N='0'	0	-	8	MΩ

10.9 USB Charger Detection Characteristics

TABLE 10-10: USB CHARGER DETECTION CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Source Voltage	V_{DAT_SRC}	I_{DAT_SRC} < 250uA	0.5		0.7	V
Data Detect Voltage	V_{DAT_REF}		0.25		0.4	V
Data Source Current	I_{DAT_SRC}		250			µA
Data Sink Current	I_{DAT_SINK}		50		150	µA
Data Connect Current	I_{DP_SRC}		7		13	µA
DP/DM Pull Down Resistors for upstream battery charging	R_{PD}		14.25	16.9	20	kΩ

10.10 Regulator Output Voltages and Capacitor Requirement

TABLE 10-11: REGULATOR OUTPUT VOLTAGES AND CAPACITOR REQUIREMENT

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Regulator Output Voltage	V_{DD33}	5.5V > **VBAT** > 2.9V	2.8	3.3	3.6	V
Regulator Capacitor	C_{BYP33}		4.7			µF
Capacitor ESR	C_{ESR33}				1	Ω
Regulator Output Voltage	V_{DD12}	3.6V > **VDD33** > 2.8V		1.2		V
Regulator Capacitor	C_{BYP12}		1.0			µF
Capacitor ESR	C_{ESR12}				1	Ω

10.11 ESD and Latch-Up Performance

TABLE 10-12: ESD AND LATCH-UP PERFORMANCE

Parameter	Conditions	Min	Typ	Max	Units	Comments
ESD Performance						
	Human Body Model			±5	kV	Device
System	EN/IEC 61000-4-2 Contact Discharge			±15	kV	3rd party system test
System	EN/IEC 61000-4-2 Air-gap Discharge			±15	kV	3rd party system test
Latch-Up Performance						
All Pins	EIA/JESD 78, Class II		150		mA	

10.12 ESD Performance

The USB3803 is protected from ESD strikes. By eliminating the requirement for external ESD protection devices, board space is conserved, and the board manufacturer is enabled to reduce cost. The advanced ESD structures integrated into the USB3803 protect the device whether or not it is powered up.

10.12.1 HUMAN BODY MODEL (HBM) PERFORMANCE

HBM testing verifies the ability to withstand the ESD strikes like those that occur during handling and manufacturing, and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event. All pins on the USB3803 provide ±5 kV HBM protection, as shown in Table 10-12.

10.12.2 EN 61000-4-2 PERFORMANCE

The EN 61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. In contrast, the HBM ESD tests are performed at the device level with the device powered down.

Microchip contracts with Independent laboratories to test the USB3803 to EN 61000-4-2 in a working system. Reports are available upon request. Please contact your Microchip representative, and request information on 3rd party ESD test results. The reports show that systems designed with the USB3803 can safely provide the ESD performance shown in without additional board level protection.

In addition to defining the ESD tests, EN 61000-4-2 also categorizes the impact to equipment operation when the strike occurs (ESD Result Classification). The USB3803 maintains an ESD Result Classification 1 or 2 when subjected to an EN 61000-4-2 (level 4) ESD strike.

Both air discharge and contact discharge test techniques for applying stress conditions are defined by the EN 61000-4-2 ESD document.

10.12.3 AIR DISCHARGE

To perform this test, a charged electrode is moved close to the system being tested until a spark is generated. This test is difficult to reproduce because the discharge is influenced by such factors as humidity, the speed of approach of the electrode, and construction of the test equipment.

10.12.4 CONTACT DISCHARGE

The uncharged electrode first contacts the pin to prepare this test, and then the probe tip is energized. This yields more repeatable results, and is the preferred test method. The independent test laboratories contracted by Microchip provide test results for both types of discharge methods.

10.13 AC Specifications

10.13.1 REFCLK

External Clock:50% duty cycle ± 10%, ± 350ppm, Jitter < 100ps rms.

10.13.2 SERIAL INTERFACE

The Microchip Hub conforms to AC specifications as set forth in the I2C Specification for Slave-Only devices.

10.13.3 USB 2.0

The Microchip Hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 Specification. Please refer to the USB 2.0 Specification which is available from the www.usb.org web site.

11.0 APPLICATION REFERENCE

11.1 Application Diagram

The USB3803 requires several external components to function and insure compliance with the USB 2.0 specification.

TABLE 11-1: COMPONENT VALUES IN APPLICATION DIAGRAMS

Reference Designator	Value	Description	Notes
$C_{VDD12BYP}$	1.0 µF	Capacitor to ground for regulator stability.	Place as close to the USB3803 as possible
$C_{VDD33BYP}$	4.7 µF	Capacitor to ground for regulator stability.	Place as close to the USB3803 as possible
C_{OUT}	0.1 µF	Bypass capacitor to ground.	Place as close to the USB3803 as possible
R_{BIAS}	12.0k	Series resistor to establish reference voltage used by analog circuits.	Place as close to the USB3803 as possible
R_{PU1}	10k or 1k	Pull-up for I2C bus. 10k for 100kHz or 400kHz operation. 1k for 1MHz operation.	
R_{PU2}	10k (or greater)	Pull-up for open-drain outputs	

TABLE 11-2: CAPACITANCE VALUES AT VBUS OF USB CONNECTOR

Port	MIN Value	MAX Value
Downstream	120µF	
Upstream	1µF	10µF

FIGURE 11-1: INTERNAL CHIP-TO-CHIP INTERFACE

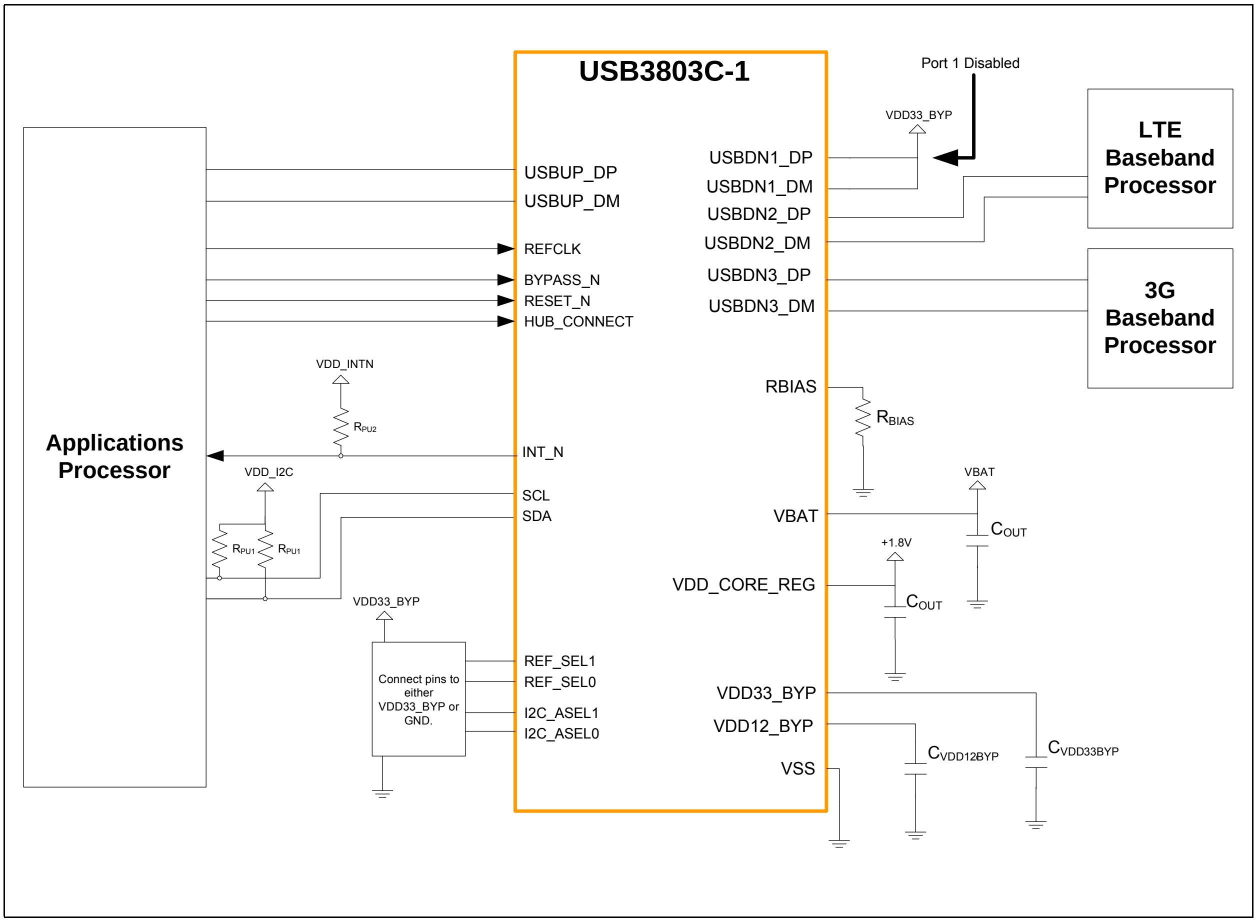
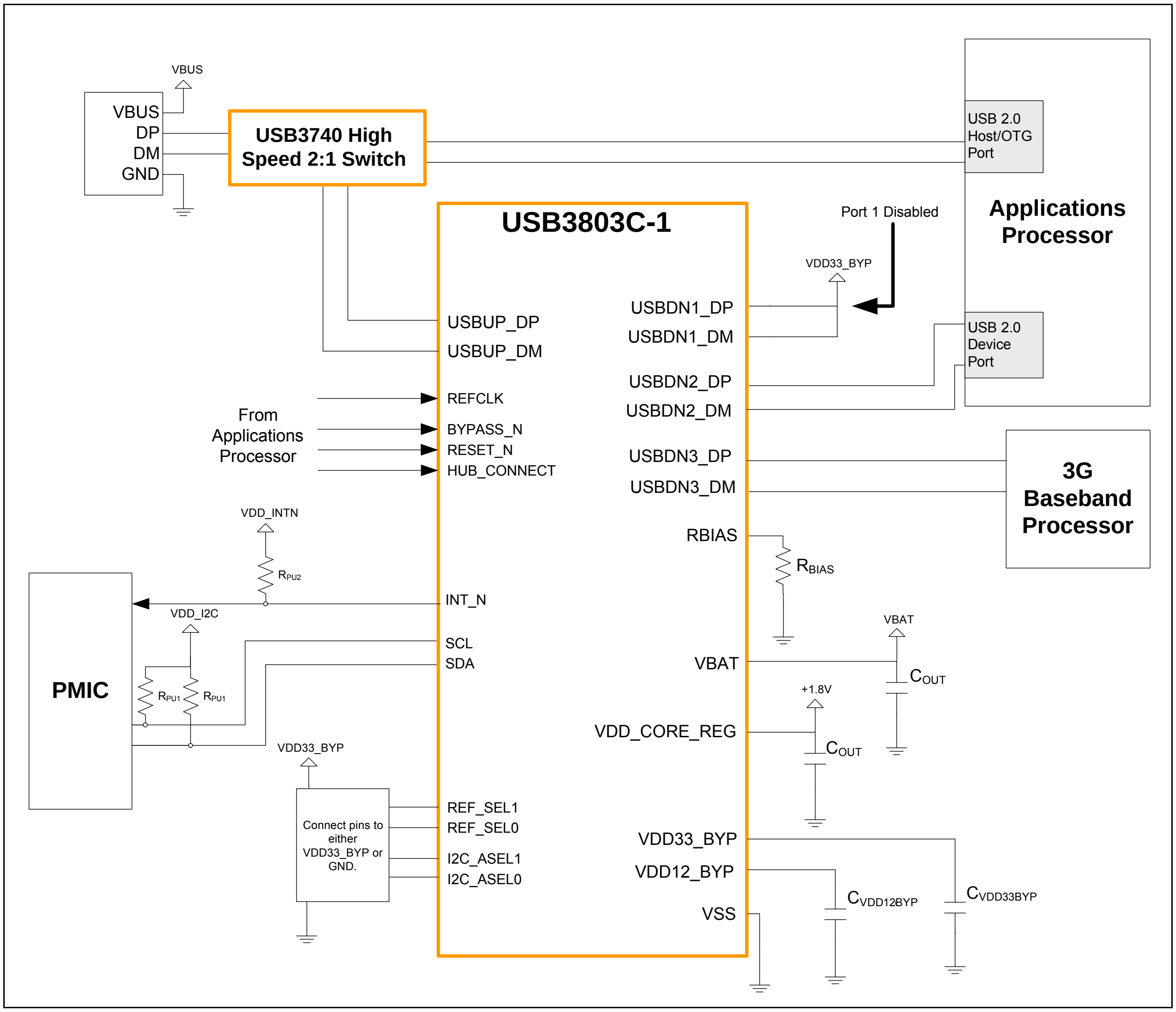
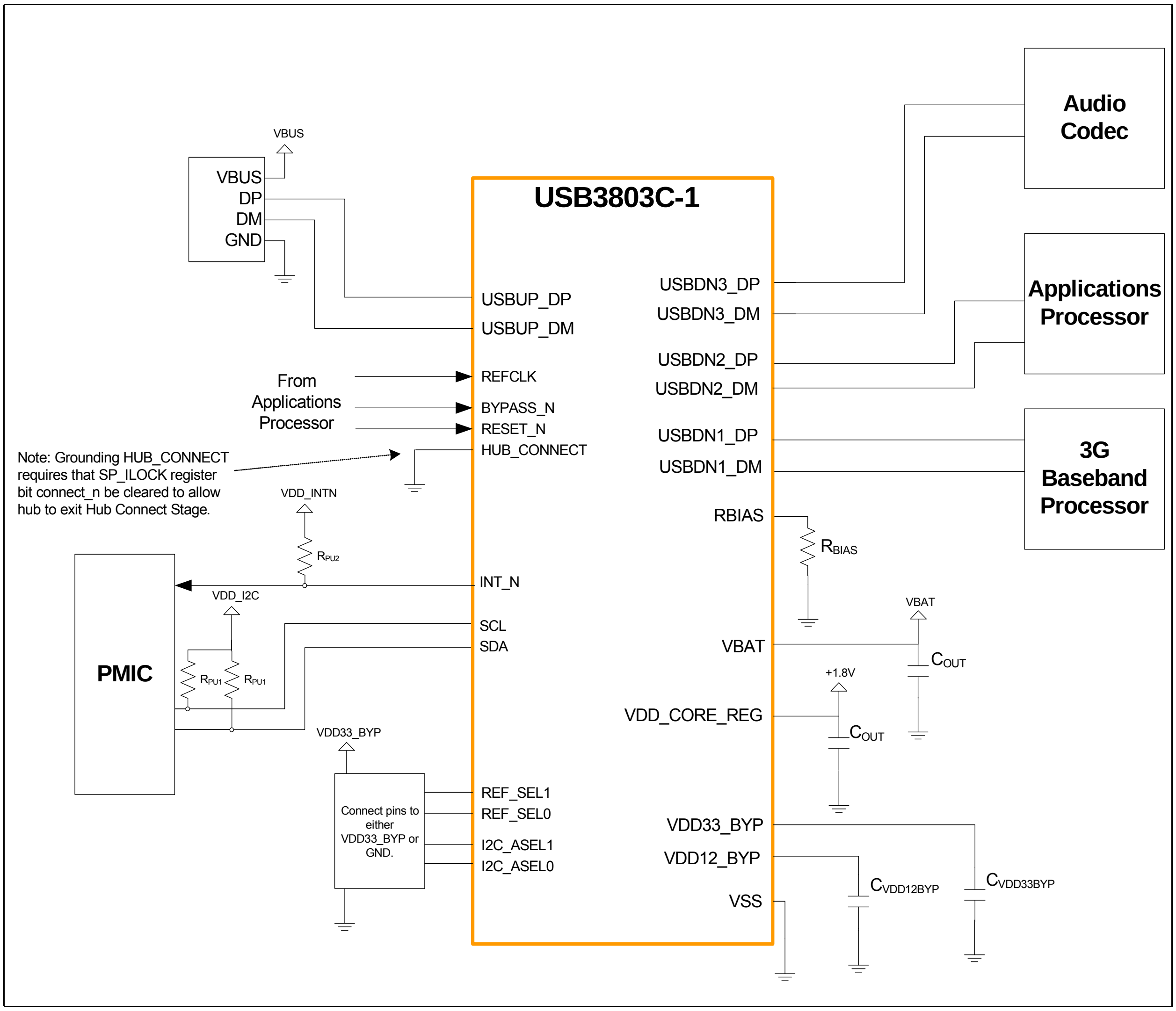


FIGURE 11-2: DUAL USB DEVICE AND HOST APPLICATION



Note:	While RESET_N is driven low, all other inputs from Applications Processor should also be driven low in order to minimize current draw. To disable a downstream port, tie DP and DM to VDD33_BYP pin of the USB3803.

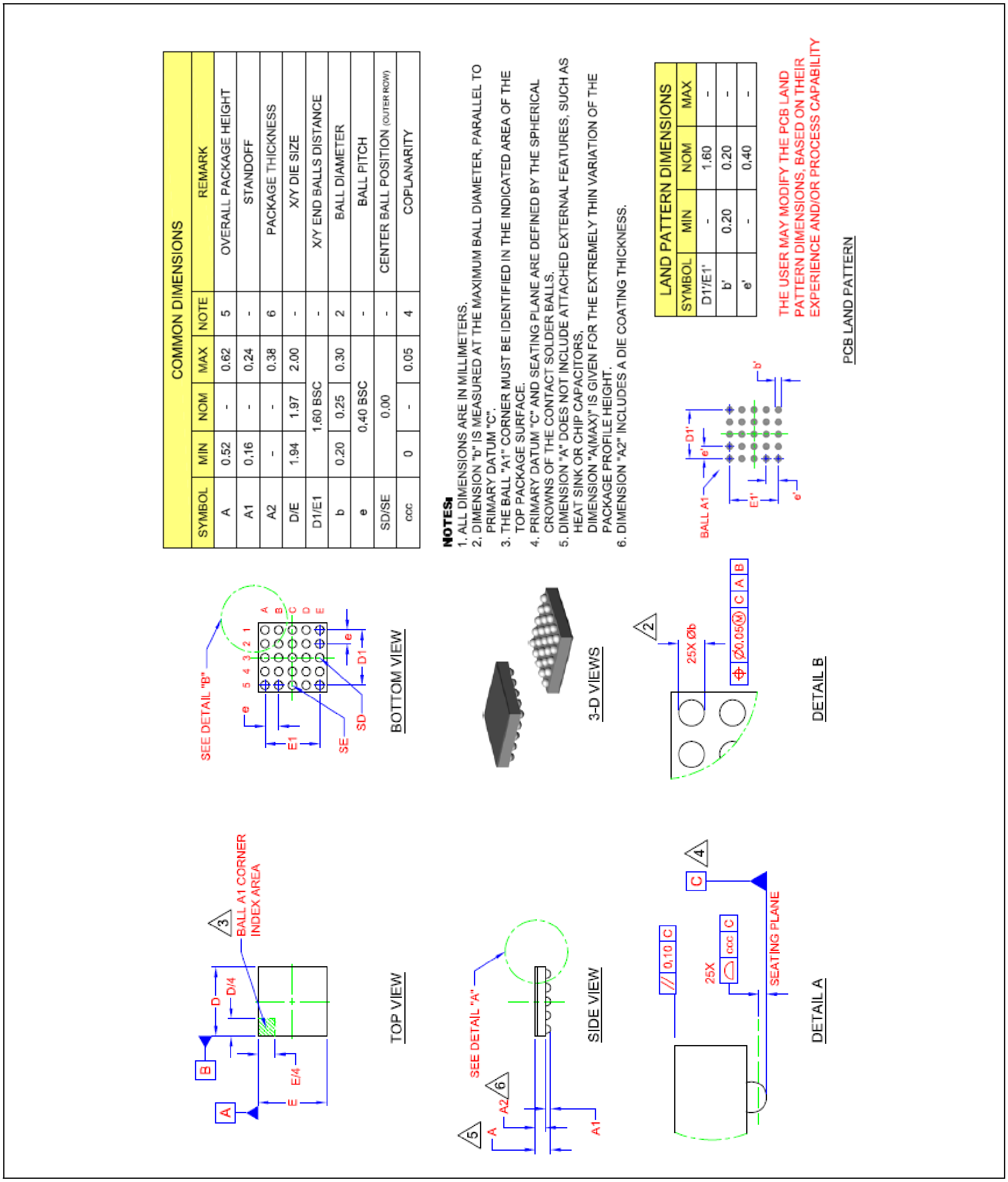
FIGURE 11-3: APPLICATION WITH USB PORT ACCESS TO THREE INTERNAL DEVICES



12.0 PACKAGE OUTLINES, TAPE & REEL DRAWINGS, PACKAGE MARKING

Note:	For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

FIGURE 12-1: 25WLCSP, 1.95X1.95MM BODY, 0.4MM PITCH



COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.52	-	0.62	5	OVERALL PACKAGE HEIGHT
A1	0.16	-	0.24	-	STANDOFF
A2	-	-	0.38	6	PACKAGE THICKNESS
D/E	1.94	1.97	2.00	-	X/Y DIE SIZE
D1/E1		1.60 BSC		-	X/Y END BALLS DISTANCE
b	0.20	0.25	0.30	2	BALL DIAMETER
e		0.40 BSC		-	BALL PITCH
SD/SE		0.00		-	CENTER BALL POSITION (OUTER ROW)
ccc	0	-	0.05	4	COPLANARITY

LAND PATTERN DIMENSIONS

SYMBOL	MIN	NOM	MAX
D1'/E1'	-	1.60	-
b'	0.20	0.20	-
e'	-	0.40	-

FIGURE 12-2: 25WLCSP, 1.95X1.95 TAPE AND REEL

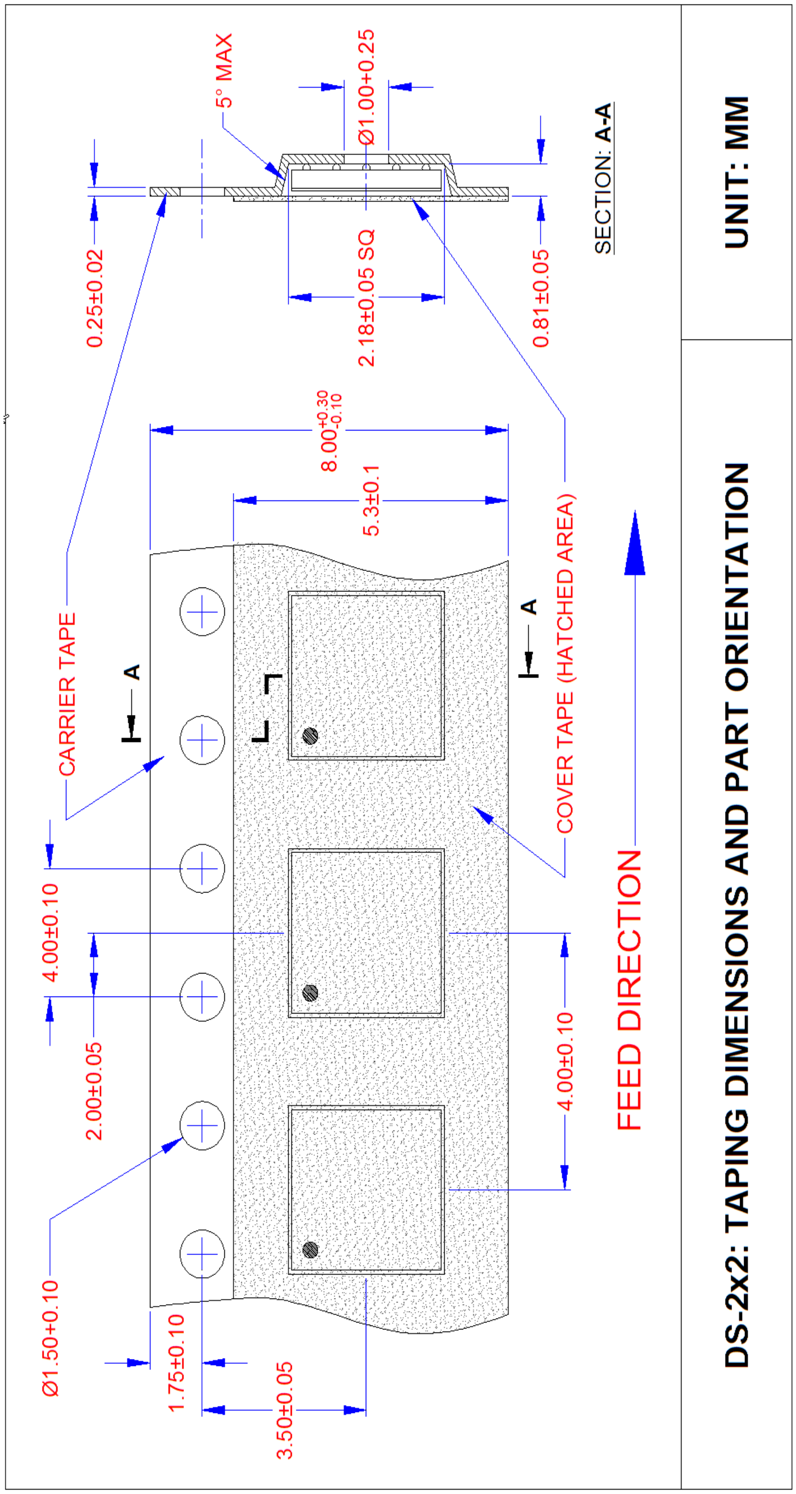
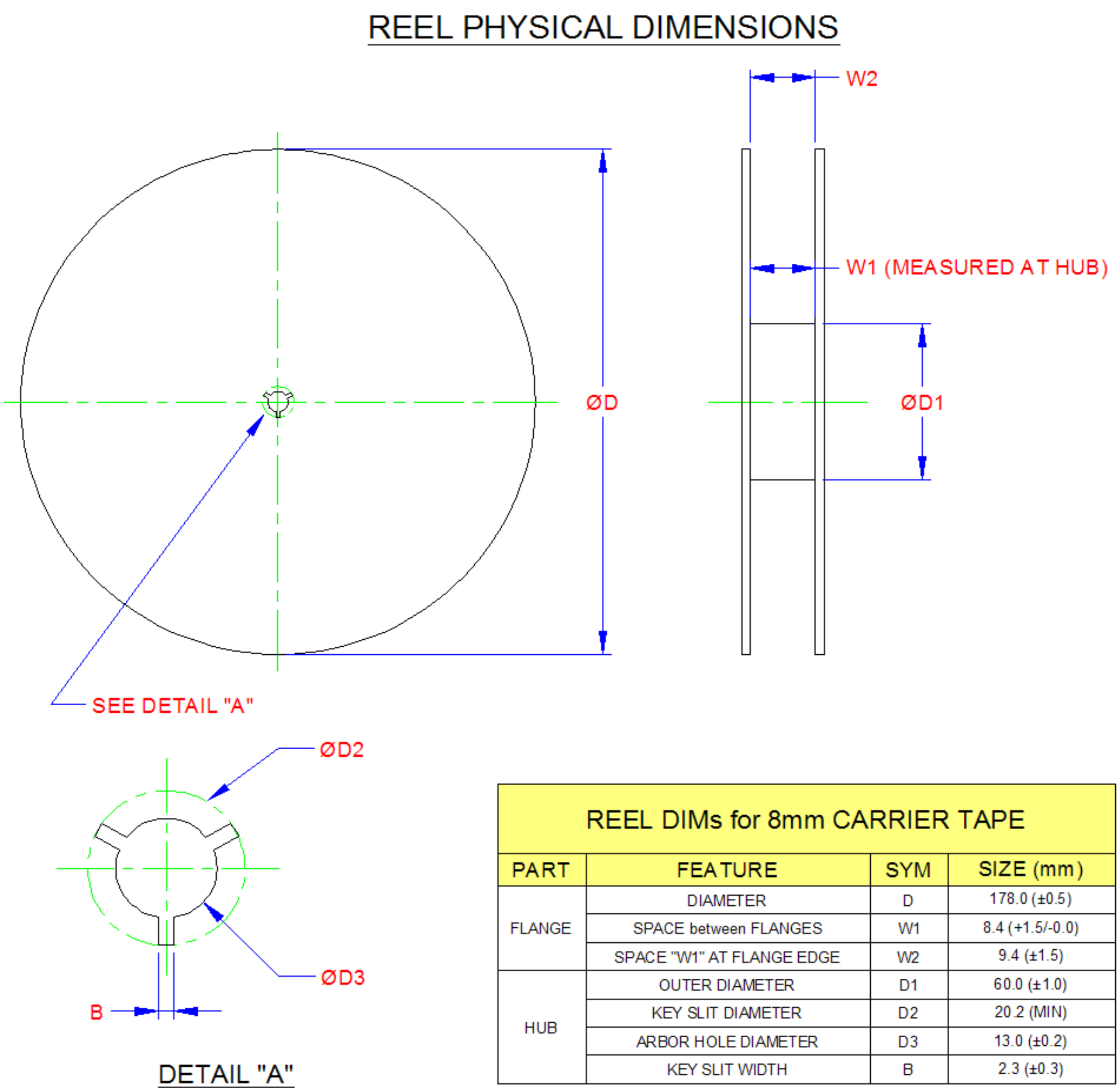
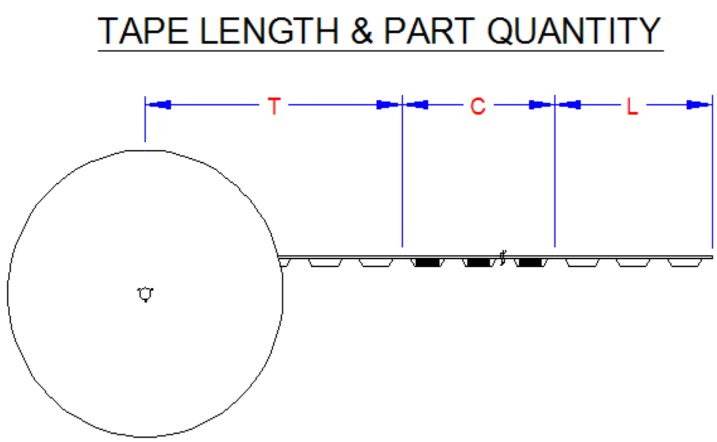


FIGURE 12-3: 25WLCSP, 1.95X1.95 REEL DIMENSIONS



REEL DIMs for 8mm CARRIER TAPE			
PART	FEATURE	SYM	SIZE (mm)
FLANGE	DIAMETER	D	178.0 (±0.5)
	SPACE between FLANGES	W1	8.4 (+1.5/-0.0)
	SPACE "W1" AT FLANGE EDGE	W2	9.4 (±1.5)
HUB	OUTER DIAMETER	D1	60.0 (±1.0)
	KEY SLIT DIAMETER	D2	20.2 (MIN)
	ARBOR HOLE DIAMETER	D3	13.0 (±0.2)
	KEY SLIT WIDTH	B	2.3 (±0.3)

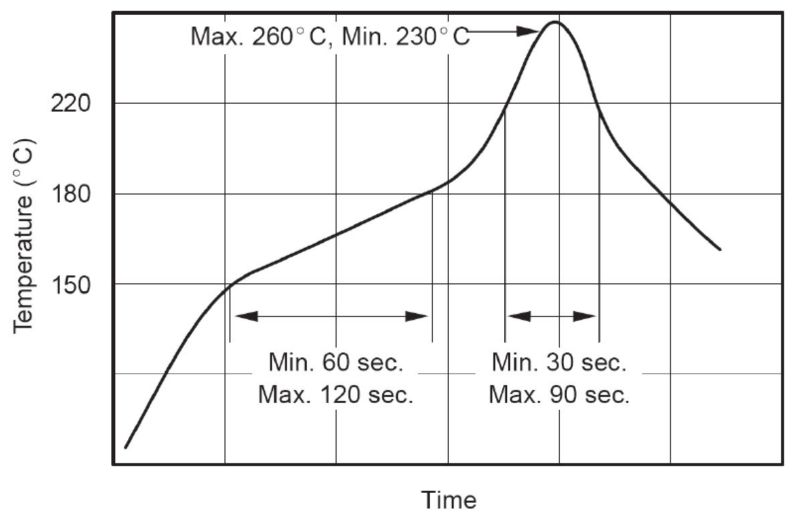
FIGURE 12-4: 25WLCSP, 1.95X1.95 TAPE SECTIONS



TAPE SECTIONS

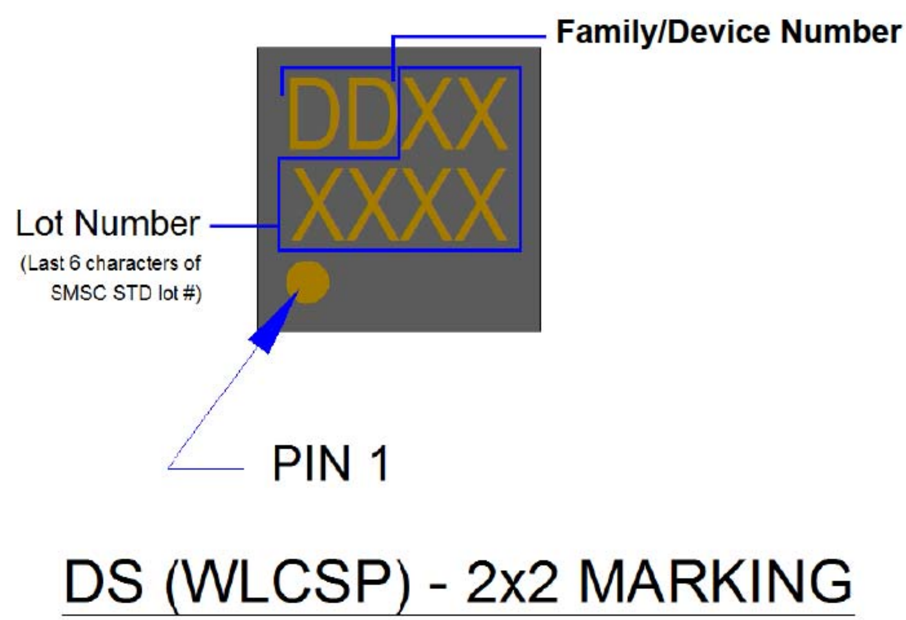
SECTION	SYM	SIZE
TRAILER	T	140 pockets
COMPONENT	C	3000 components
LEADER	L	160 pockets

FIGURE 12-5: REFLOW PROFILE AND CRITICAL PARAMETERS FOR LEAD-FREE (SNAGCU) SOLDER



Process Step	Lead-Free Solder
Ramp Rate	3°C/sec
Pre-Heat	150°C to 180°C, 60 to 180 seconds
Time above Liquidus, 220°C	30 to 90 seconds
Peak Temperature	255°C ±5°C
Time within 5°C of Peak Temperature	10 to 20 seconds
Ramp Down Rate	6°C/sec Maximum

FIGURE 12-6: PACKAGE MARKING



13.0 REVISION HISTORY

TABLE 13-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
USB3803C Revision A replaces the previous SMSC version, Revision 1.1		

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
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Technical support is available through the web site at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]	-	XXX	-	[X][1]
Device	Temperature Range		Package		Tape and Reel Option

Device:	USB3803C
Temperature Range:	Blank = 0°C to +70°C (Extended Commercial) i = -40°C to +85°C (Industrial)
Package:	WLCSP= 25-Ball
Tape and Reel Option:	Blank = Standard packaging (tray) TR = Tape and Reel[1]

Examples:

a) USB3803Ci-1-GL-TR
Industrial temperature,
25-Ball WLCSP
Tape & Reel

b) USB3803C-1-GL-TR
Extended commercial temperature,
25-Ball WLCSPTape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 3,000.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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