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## Full-Featured, Low Pin Count Microcontrollers with XLP Product Brief

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### Description

PIC16(L)F183XX microcontrollers feature Analog, Core Independent Peripherals and communication peripherals, combined with eXtreme Low Power (XLP) for a wide range of general purpose and low-power applications. The Peripheral Pin Select (PPS) functionality enables pin mapping when using the digital peripherals (CLC, CWG, CCP, PWM and communications) to add flexibility to the application design.

### Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- Up to Three 16-Bit Timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Extended Watchdog Timer (WDT) with Dedicated On-Chip Oscillator for Reliable Operation
- Programmable Code Protection

### Memory

- Up to 14KB Program Flash Memory (PFM)
- Up to 1KB Data SRAM Memory
- 256B of EEPROM Data Flash Memory (DFM)
- Direct, Indirect and Relative Addressing modes

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF183XX)
  - 2.3V to 5.5V (PIC16F183XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

### Power-Saving Functionality

- Doze mode: Ability to run the CPU core slower than the system clock used by the internal peripherals
- Idle mode: Ability to put the CPU core to sleep while internal peripherals continue operating from the system clock
- Sleep mode: Lowest Power Consumption
- Peripheral Module Disable: Peripheral power disable hardware module to minimize power consumption of unused peripherals

### Digital Peripherals

- Configurable Logic Cell (CLC):
  - Up to four CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Up to two CWGs
  - Multiple signal sources
- Up to Four Capture/Compare/PWM (CCP) modules
- PWM: Two 10-bit Pulse-Width Modulators
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock:  $0 \text{ Hz} < F_{NCO} < 32 \text{ MHz}$
  - Resolution:  $F_{NCO}/2^{20}$
- Serial Communications:
  - SPI, I<sup>2</sup>C™, EUSART
  - RS-232, RS-485, LIN compatible
- Data Signal Modulator (DSM):
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms.

# PIC16(L)F183XX

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- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Up to 18 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select

## Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 17 external channels
  - Conversion available during Sleep
- Comparator:
  - Up to two comparators
  - Low and High-Speed modes
  - Fixed Voltage Reference at inverting/non-inverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

## Clocking Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 32 MHz
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External High-Speed Crystal Oscillators

**TABLE 1: PIC16(L)F183XX Family Types**

Device	Data Sheet Index	Program Flash Memory (K words)	Program Memory Flash (K bytes)	Data Memory (bytes)	Data SRAM (bytes)	I/Os <sup>(1)</sup>	10-bit ADC (ch)	5-bit DAC	Comparators	CWG	Clock Ref	Timers (8/16-bit)	CCP	PWM	NCO	EUSART	MSSP (I <sup>2</sup> C™/SPI)	CLC	DSM	PPS	XLP	PMD	Idle & Doze	Debug <sup>(2)</sup>
PIC16(L)F18313	(A)	2	3.5	256	256	6	9	1	1	1	1	2/1	2	2	1	1	1	2	1	Y	Y	Y	Y	I/E
PIC16(L)F18323	(A)	2	3.5	256	256	12	15	1	2	1	1	2/1	2	2	1	1	1	2	1	Y	Y	Y	Y	I/E
PIC16(L)F18324	(B)	4	7	256	512	12	15	1	2	2	1	4/3	4	2	1	1	1	4	1	Y	Y	Y	Y	I/E
PIC16(L)F18325	(C)	8	14	256	1K	12	15	1	2	2	1	4/3	4	2	1	1	2	4	1	Y	Y	Y	Y	I/E
PIC16(L)F18344	(B)	4	7	256	512	18	21	1	2	2	1	4/3	4	2	1	1	1	4	1	Y	Y	Y	Y	I/E
PIC16(L)F18345	(C)	8	14	256	1K	18	21	1	2	2	1	4/3	4	2	1	1	2	4	1	Y	Y	Y	Y	I/E

**Note 1:** One pin is input-only.

**Note 2:** Debugging Methods: (I) – Integrated on Chip; E – using Emulation Header.

**Data Sheet Index:** (Unshaded devices are described in this document.)

**Note A:** Future Release [PIC16\(L\)F18313/18323 Data Sheet](#), [Full-Featured, Low Pin Count Microcontrollers with XLP](#)  
**Note B:** Future Release [PIC16\(L\)F18324/18344 Data Sheet](#), [Full-Featured, Low Pin Count Microcontrollers with XLP](#)  
**Note C:** Future Release [PIC16\(L\)F18325/18345 Data Sheet](#), [Full-Featured, Low Pin Count Microcontrollers with XLP](#)

**Note:** For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

# PIC16(L)F183XX

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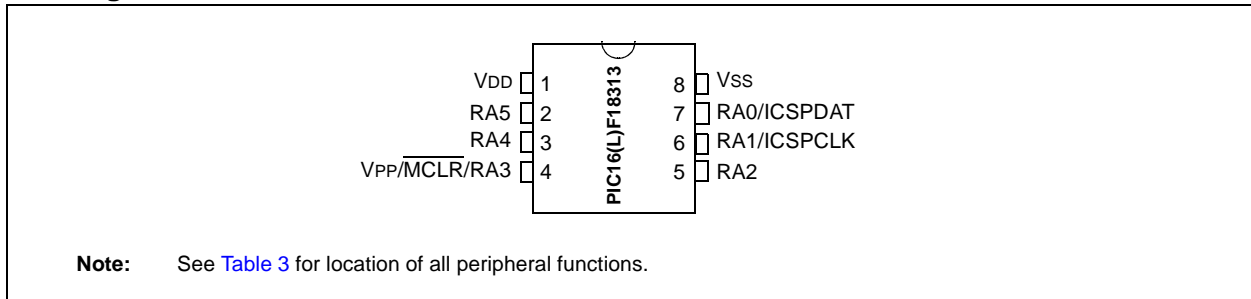
**TABLE 2: PACKAGES**

Packages	PDIP	SOIC	DFN/UDFN	TSSOP	QFN/UQFN	SSOP
PIC16(L)F18313	X	X	X			
PIC16(L)F18323	X	X		X	X	
PIC16(L)F18324	X	X		X	X	
PIC16(L)F18325	X	X		X	X	
PIC16(L)F18344	X	X			X	X
PIC16(L)F18345	X	X			X	X

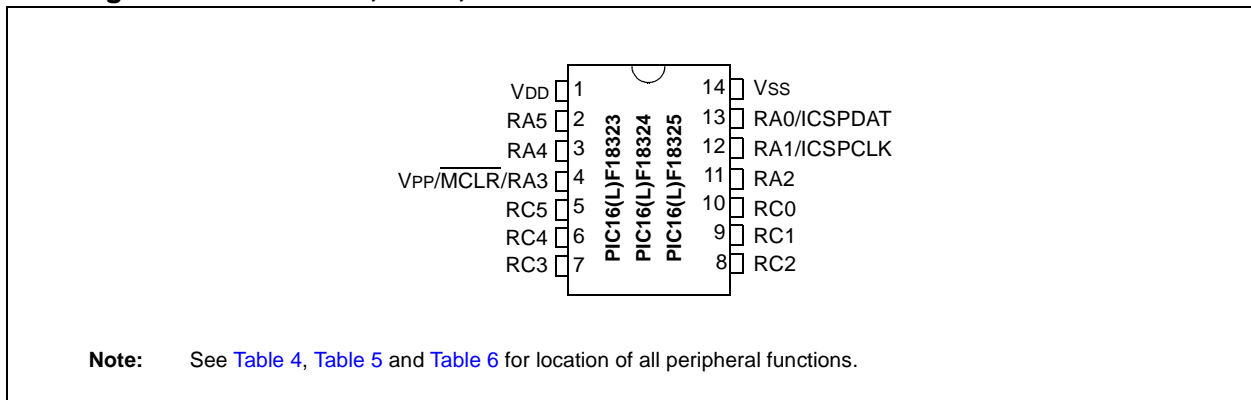
**Note:** Pin details are subject to change.

## PIN DIAGRAMS

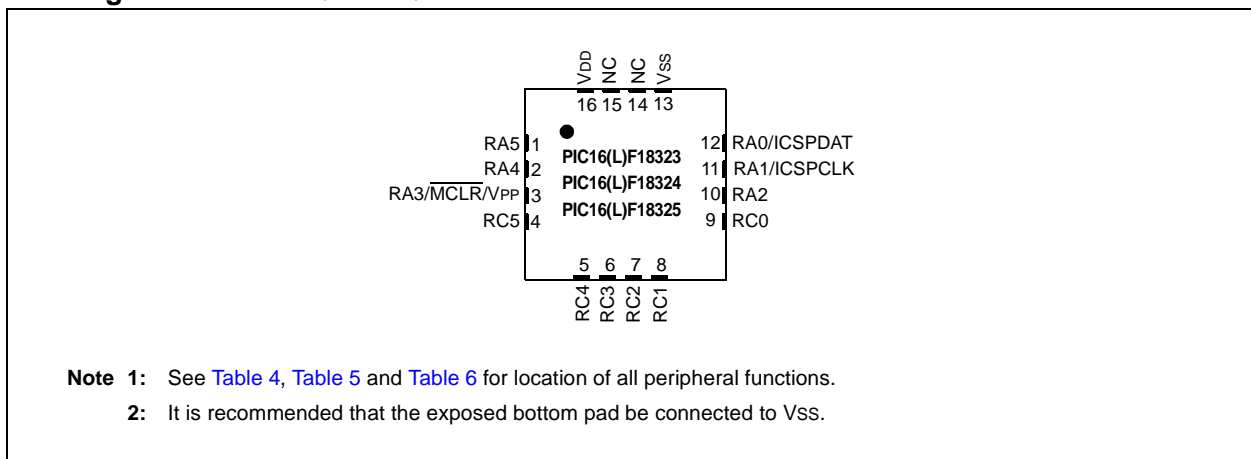
### Pin Diagram – 8-Pin PDIP, SOIC, DFN/UDFN



### Pin Diagram – 14-Pin PDIP, SOIC, TSSOP

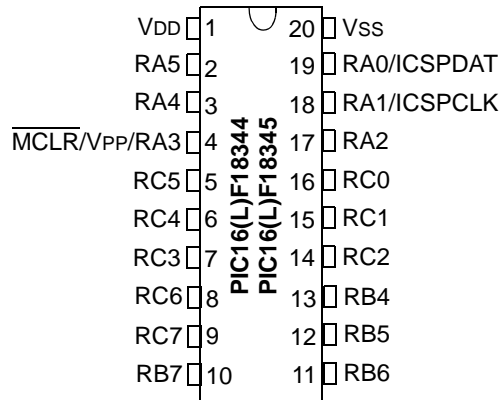


### Pin Diagram – 16-Pin QFN/UQFN



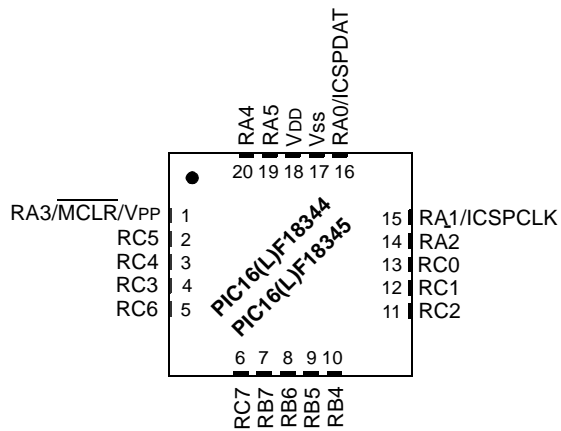
# PIC16(L)F183XX

## Pin Diagram – 20-Pin PDIP, SOIC, SSOP



**Note:** See [Table 7](#) and [Table 8](#) for location of all peripheral functions.

## Pin Diagram – 20-Pin QFN/UQFN (4x4)



- Note 1:** See [Table 7](#) and [Table 8](#) for location of all peripheral functions.
- 2:** It is recommended that the exposed bottom pad be connected to VSS.

## PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F18313)

I/O <sup>(2)</sup>	8-Pin PDIP/SOIC/DFN/UDFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	7	ANA0	—	C1IN0+	—	DAC1OUT	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	6	ANA1	VREF+	C1IN0-	—	DAC1REF+	MDMIN <sup>(1)</sup>	—	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	CLCIN2 <sup>(1)</sup>	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	5	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	—	—	CWG1 <sup>(1)</sup>	SDA <sup>(1,3,4)</sup> SDO <sup>(1)</sup>	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	—	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCA3	Y	MCLR VPP
RA4	3	ANA4	—	C1IN1-	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	ANA5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T1CKI <sup>(1)</sup> SOSCIN SOSCI	CCP1 <sup>(1)</sup> CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1
VDD	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT <sup>(2)</sup>	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	—	—	—	—	CCP2	PWM6	CWG1B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/JUQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	TOCKI <sup>(1)</sup>	—	—	CWG1 <sup>(1)</sup>	—	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	2	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	CLCIN3 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	—	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	SDI <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN1 <sup>(1)</sup>	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	—	—	IOCC5	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
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  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.



**TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
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TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324)

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR V <sub>PP</sub>
RA4	3	2	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	CLCIN3 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI <sup>(1)</sup>	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4 <sup>(1)</sup>	—	—	SDI <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCC1	Y	—
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	T5G <sup>(1)</sup>	CCP2 <sup>(1)</sup>	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G <sup>(1)</sup>	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN1 <sup>(1)</sup>	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T3CKI <sup>(1)</sup>	CCP1 <sup>(1)</sup>	—	—	—	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	—	—	IOCC5	Y	—
V <sub>DD</sub>	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V <sub>DD</sub>
V <sub>SS</sub>	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V <sub>SS</sub>

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324) (CONTINUED)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325)

(2) I/O	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/QFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic	
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	SS2 <sup>(1)</sup>	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT	
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK	
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	—	—	INT <sup>(1)</sup> IOCA2	Y	—	
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP	
RA4	3	2	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2	
RA5	2	1	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	CLCIN3 <sup>(1)</sup>	—	IOCA5	Y	CLKIN OSC1	
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI <sup>(1)</sup>	—	—	—	SCK1 <sup>(1)</sup> SCL1 <sup>(1,3,4)</sup>	—	—	—	IOCC0	Y	—	
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4 <sup>(1)</sup>	—	—	SDI1 <sup>(1)</sup> SDA1 <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCC1	Y	—	
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—	
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	T5G <sup>(1)</sup>	CCP2 <sup>(1)</sup>	—	—	SS1 <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—	IOCC3	Y	—	
RC4	6	5	ANC4	—	—	—	—	—	T3G <sup>(1)</sup>	—	—	—	SCK2 <sup>(1)</sup> SCL2 <sup>(1,3,4)</sup>	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN1 <sup>(1)</sup>	—	IOCC4	Y	—	
RC5	5	4	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T3CKI <sup>(1)</sup>	CCP1 <sup>(1)</sup>	—	—	SDI2 <sup>(1)</sup> SDA2 <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	—	—	IOCC5	Y	—	
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD	
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325) (Continued)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	DDS	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	CK	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO1 SDO2	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK1 SCK2	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 7: 20-PIN ALLOCATION TABLE (PIC16(L)F18344)

I/O/I	20-Pin PDIP/SOIC/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	CLCIN0 <sup>(1)</sup>	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> T3G <sup>(1)</sup> T5G <sup>(1)</sup> SOSCO	CCP4 <sup>(1)</sup>	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> T3CKI <sup>(1)</sup> T5CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	—	—	IOCA5	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	—	RX <sup>(1)</sup> DT <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 7: 20-PIN ALLOCATION TABLE (PIC16(L)F18344) (Continued)**

I/O <sup>(2)</sup>	20-Pin PDIP/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO	DT <sup>(3)</sup>	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL <sup>(3)</sup>	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA <sup>(3)</sup>	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C™ logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	SS2 <sup>(1)</sup>	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	CLCIN0 <sup>(1)</sup>	—	INT <sup>(1)</sup> IOCA2	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	MCLR VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> T3G <sup>(1)</sup> T5G <sup>(1)</sup> SOSCO	CCP4 <sup>(1)</sup>	—	—	—	—	—	—	IOCA4	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI <sup>(1)</sup> T3CKI <sup>(1)</sup> T5CKI <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	—	—	IOCA5	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI1 <sup>(1)</sup> SDA1 <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	SDI2 <sup>(1)</sup> SDA2 <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1 <sup>(1)</sup> SCL1 <sup>(1,3,4)</sup>	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	SCK2 <sup>(1)</sup> SCL2 <sup>(1,3,4)</sup>	TX <sup>(1)</sup> CK <sup>(1)</sup>	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—	IOCC2	Y	—

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**TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)**

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin QFN/UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1 SDO2	DT <sup>(3)</sup>	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK1 SCK2	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	—	CLC4OUT	—	—	—	—

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