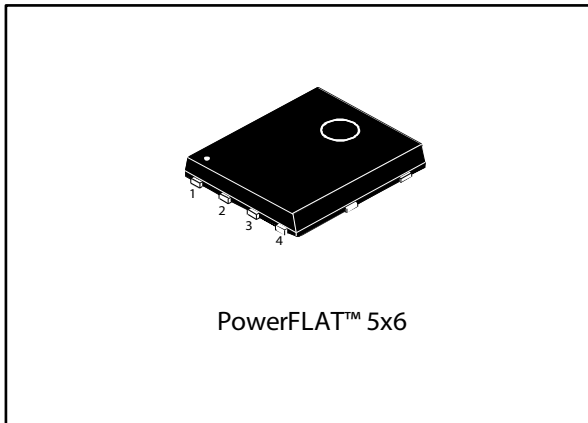
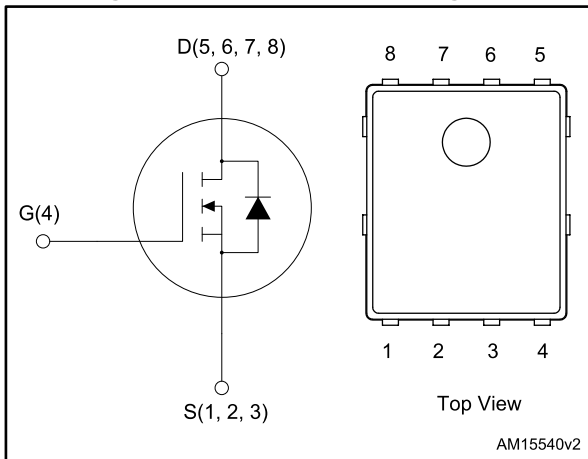


## N-channel 60 V, 0.0024 $\Omega$ typ., 140 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data


**Figure 1: Internal schematic diagram**


### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STL140N6F7	60 V	0.0028 $\Omega$	140 A	125 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

**Table 1: Device summary**

Order code	Marking	Package	Packing
STL140N6F7	140N6F7	PowerFLAT™ 5x6	Tape and reel

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## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves).....	5
<b>3</b>	<b>Test circuits .....</b>	<b>7</b>
<b>4</b>	<b>Package information .....</b>	<b>8</b>
	4.1 PowerFLAT™ 5x6 type C package information .....	9
	4.2 PowerFLAT™ 5x6 packing information.....	11
<b>5</b>	<b>Revision history .....</b>	<b>13</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	140	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	107	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	560	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	30	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	21	
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	116	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	125	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Maximum junction temperature	175	

**Notes:**

- <sup>(1)</sup> This value is rated according to  $R_{thj-c}$ .
- <sup>(2)</sup> Pulse width is limited by safe operating area.
- <sup>(3)</sup> This value is rated according to  $R_{thj-pcb}$ .

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case	1.2	

**Notes:**

- <sup>(1)</sup> When mounted on a 1-inch<sup>2</sup> FR-4 board, 2oz Cu,  $t < 10\text{ s}$

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	60			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$		0.0024	0.0028	$\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	3110	-	pF
$C_{oss}$	Output capacitance		-	1520	-	
$C_{rss}$	Reverse transfer capacitance		-	193	-	
$Q_g$	Total gate charge	$V_{DD} = 30\text{ V}$ , $I_D = 30\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Gate charge test circuit"</a> )	-	55	-	nC
$Q_{gs}$	Gate-source charge		-	19	-	
$Q_{gd}$	Gate-drain charge		-	18	-	

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 15\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	24	-	ns
$t_r$	Rise time		-	68	-	
$t_{d(off)}$	Turn-off delay time		-	39	-	
$t_f$	Fall time		-	20	-	

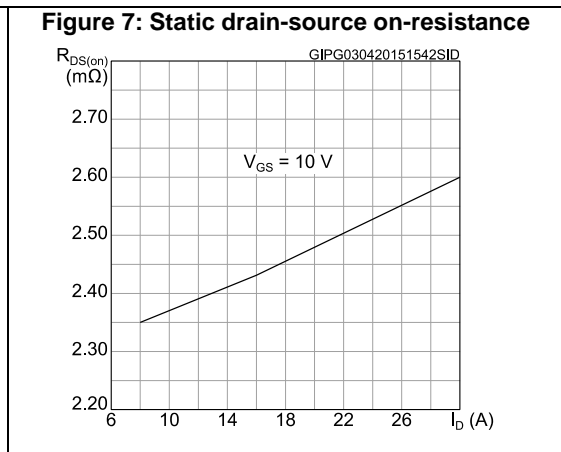
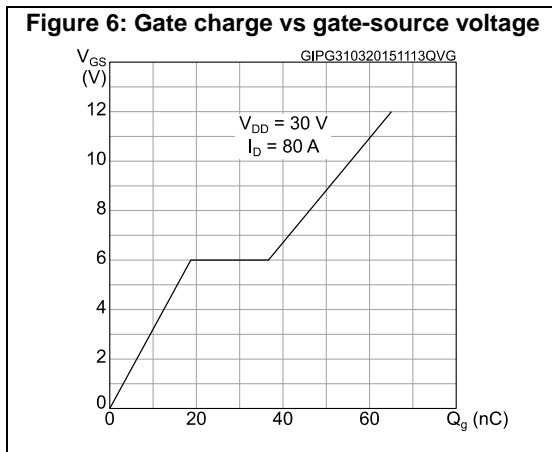
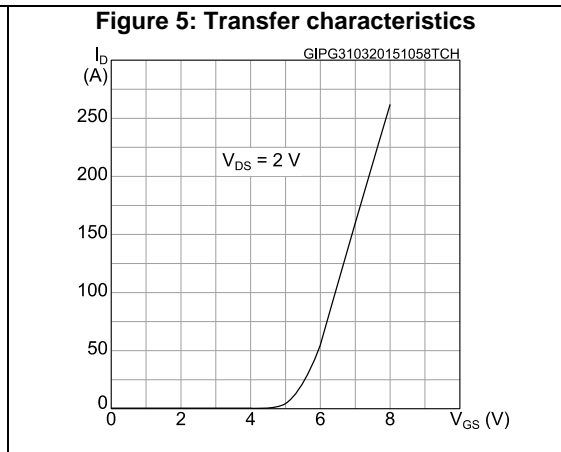
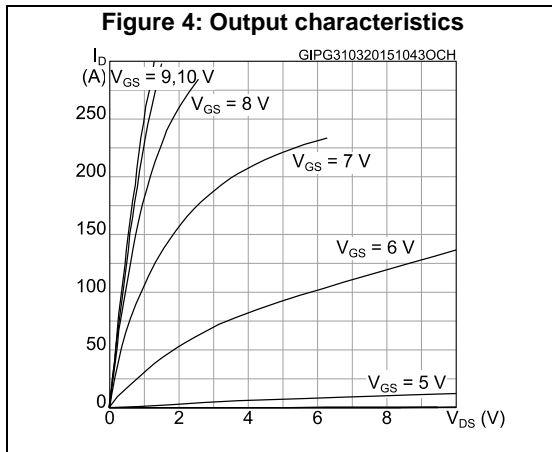
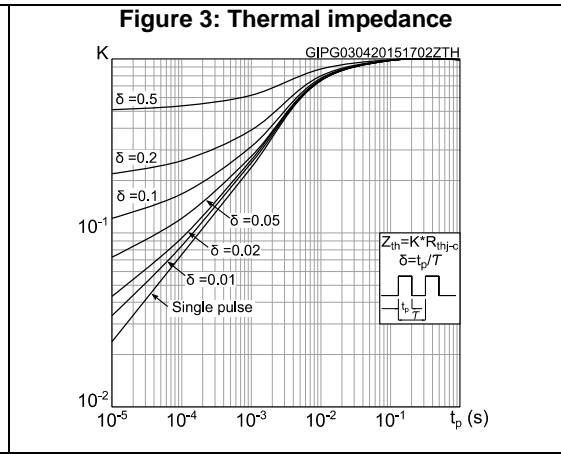
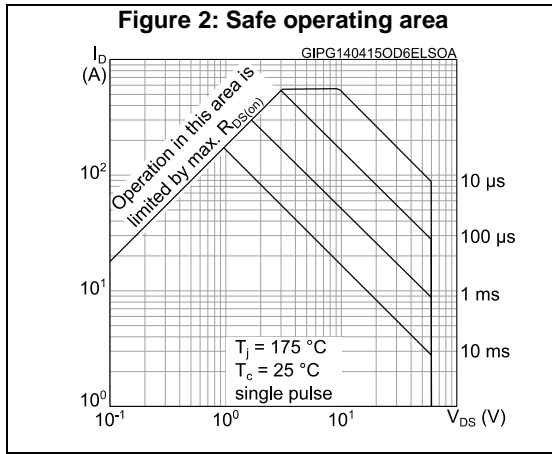
**Table 7: Source-drain diode**

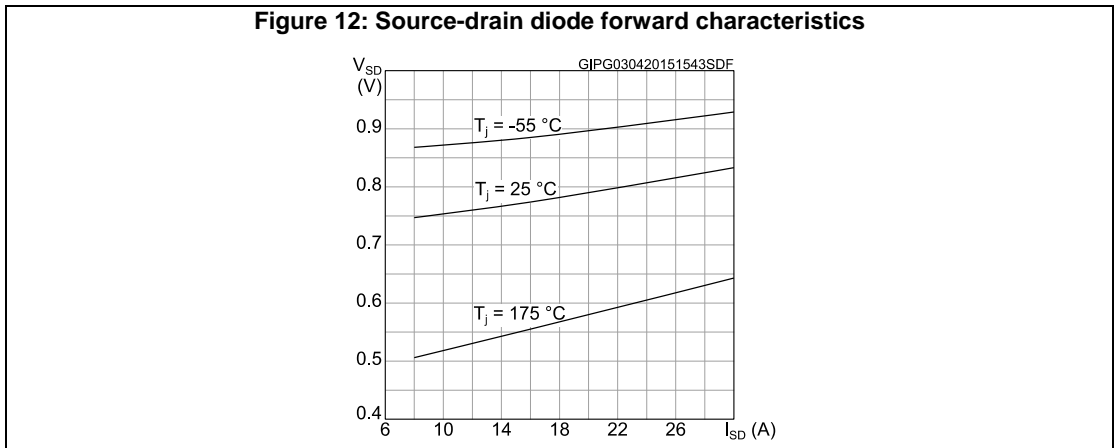
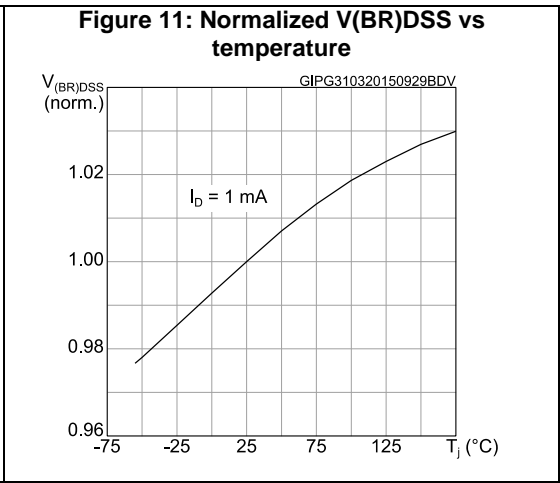
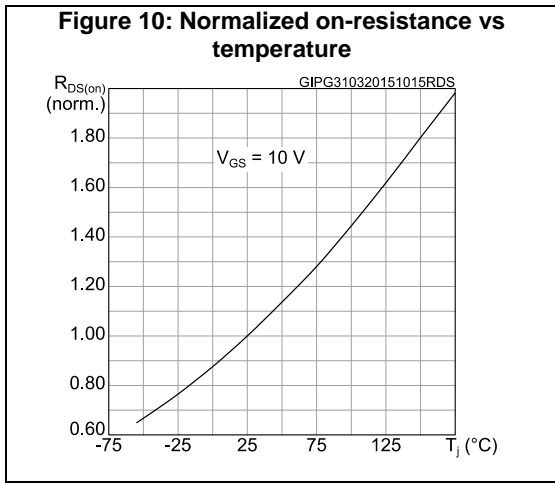
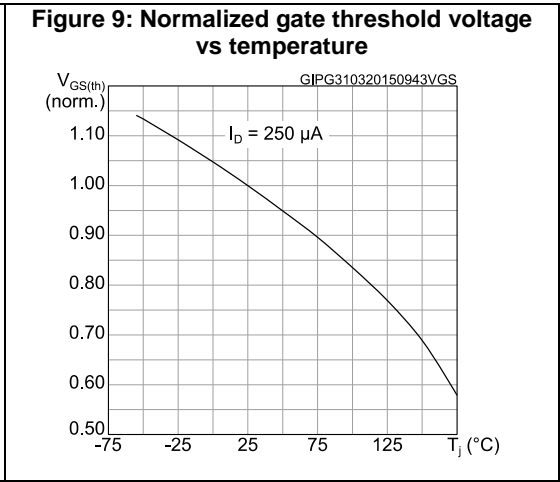
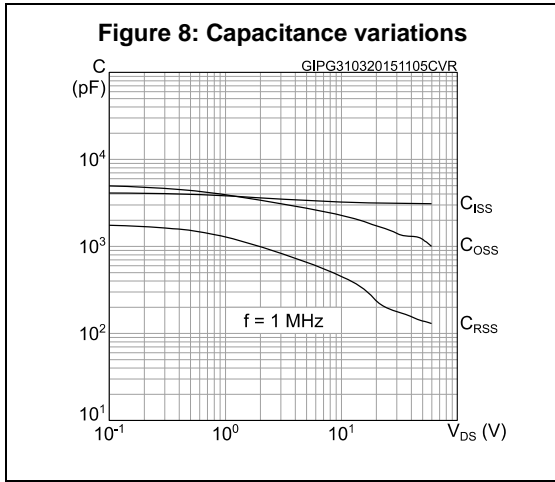
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 30\text{ A}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 30\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 48\text{ V}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	42.4		ns
$Q_{rr}$	Reverse recovery charge		-	38.2		nC
$I_{RRM}$	Reverse recovery current		-	1.8		A

**Notes:**

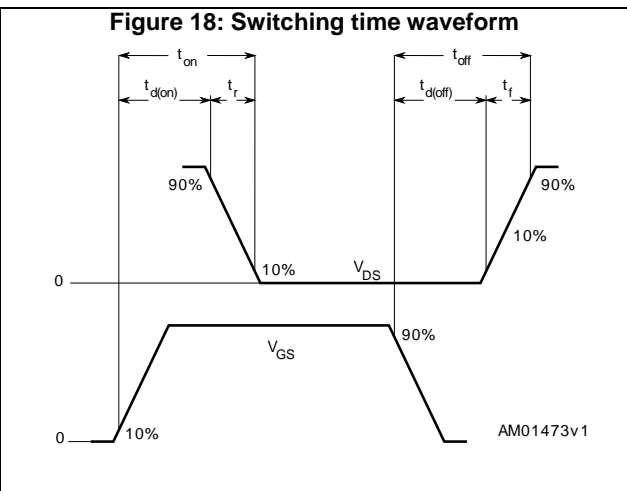
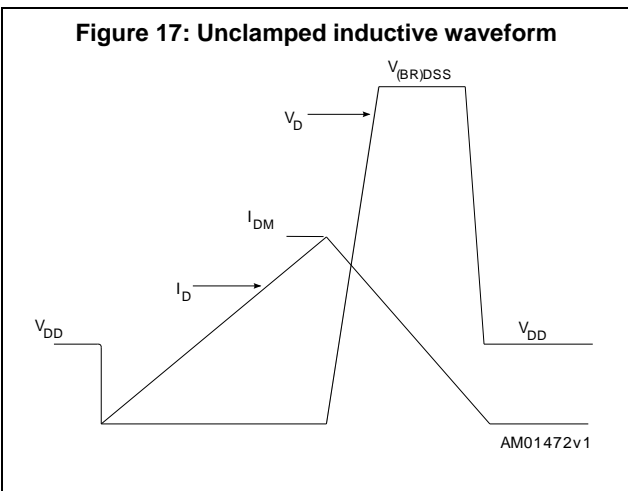
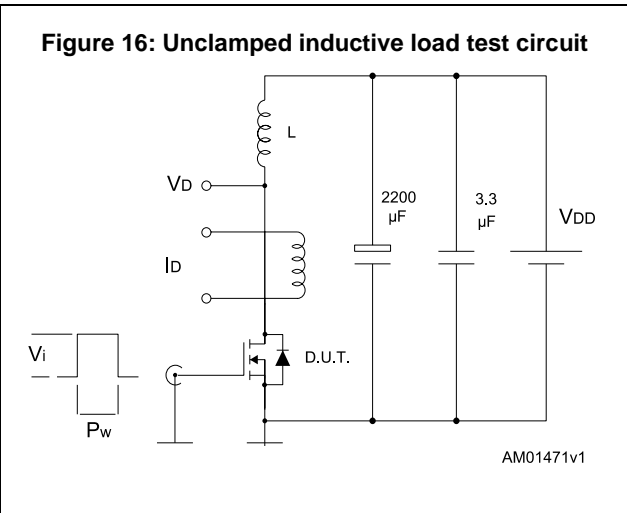
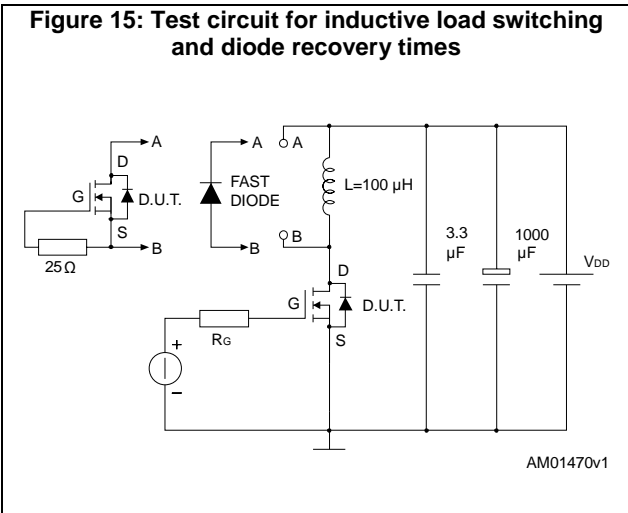
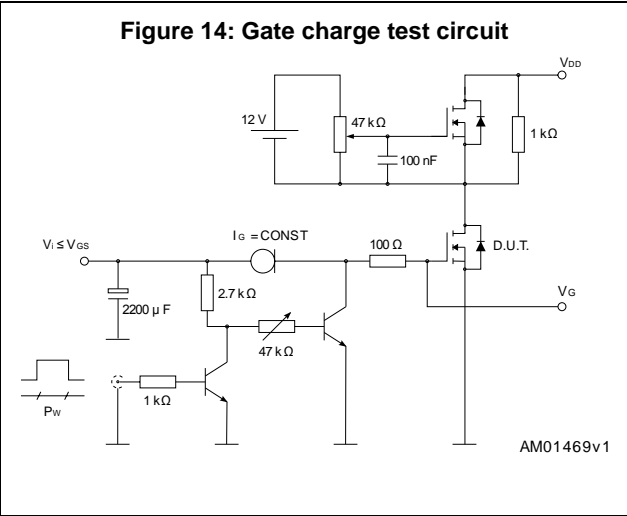
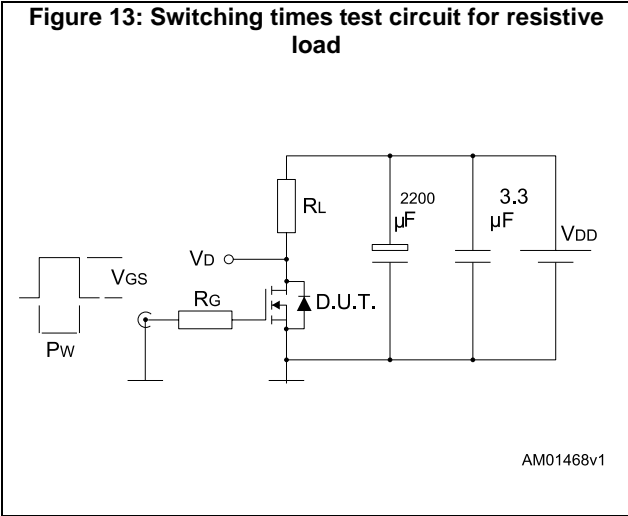
<sup>(1)</sup> Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)





### 3 Test circuits



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



### 4.1 PowerFLAT™ 5x6 type C package information

Figure 19: PowerFLAT™ 5x6 type C package outline

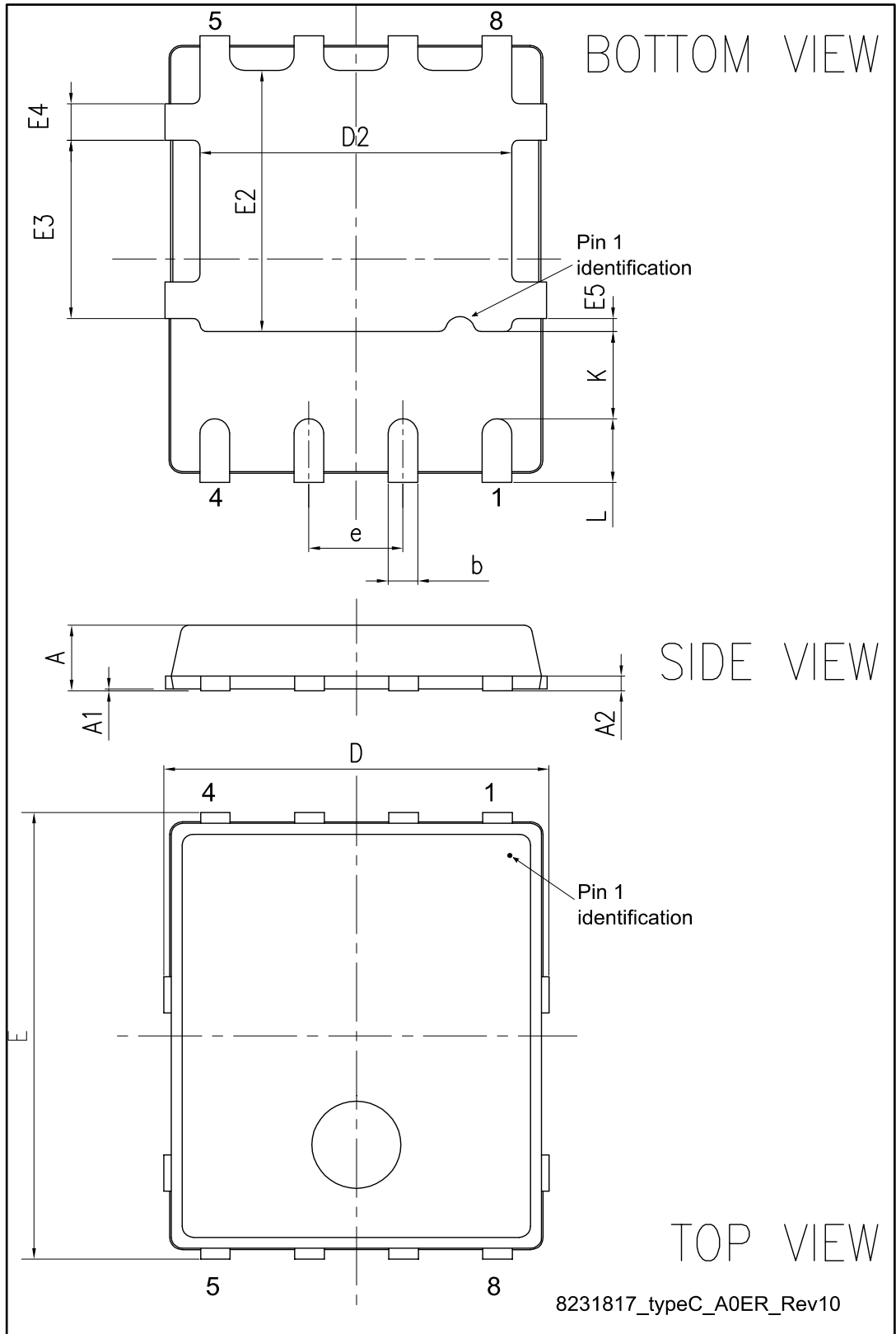
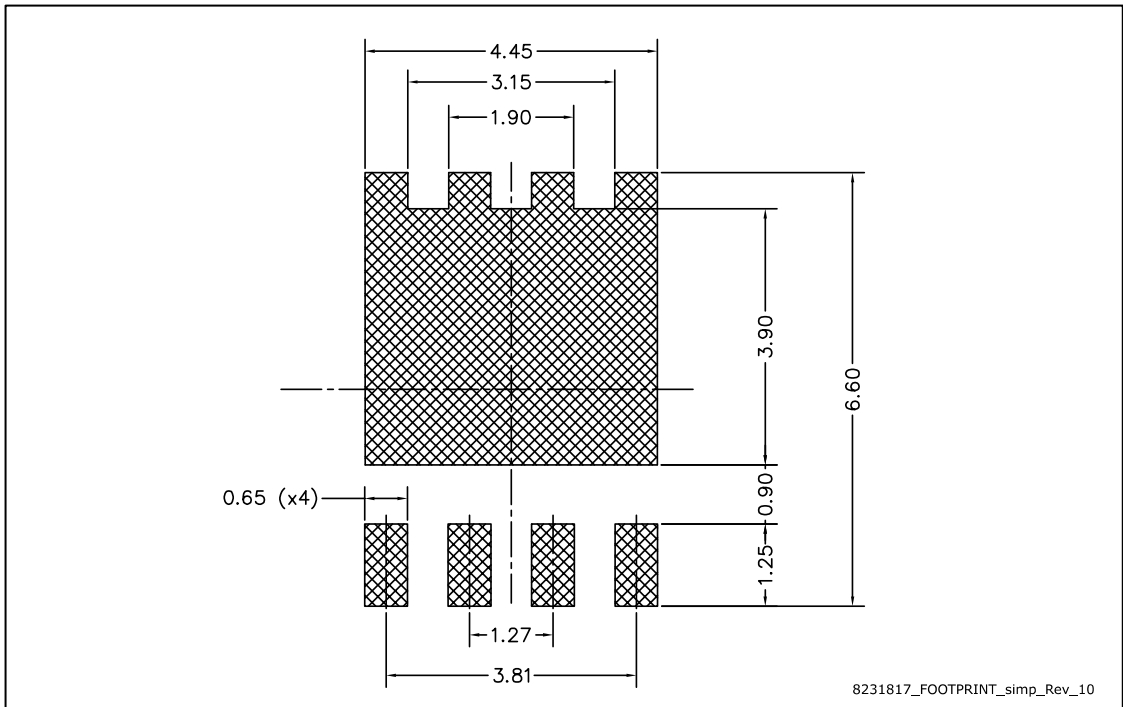


Table 8: PowerFLAT™ 5x6 type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

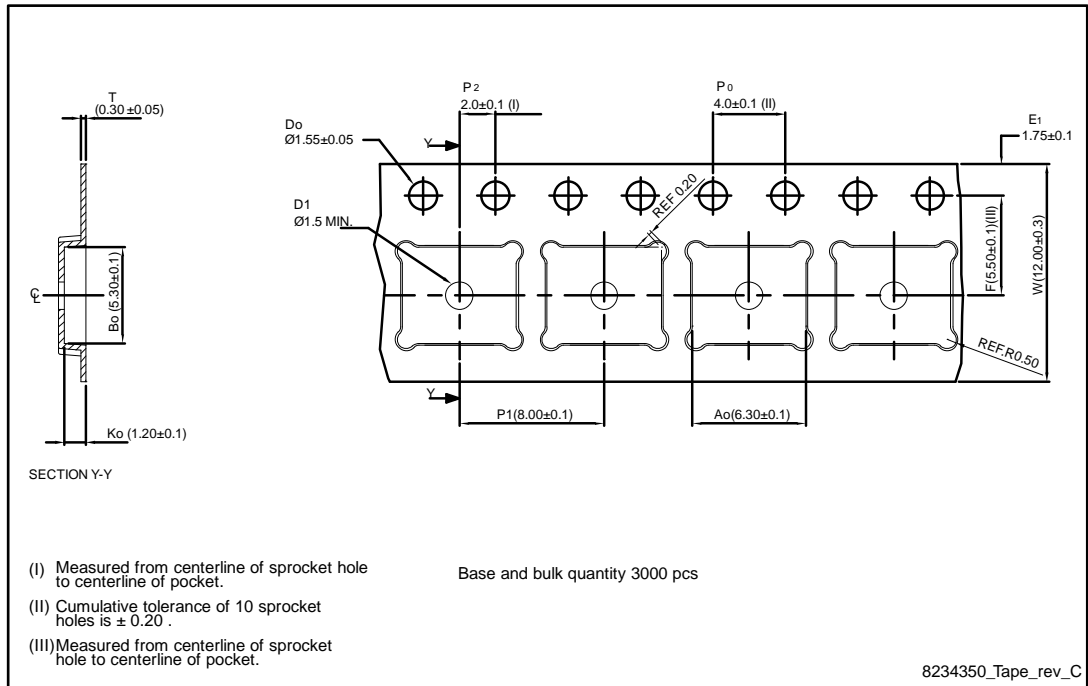


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

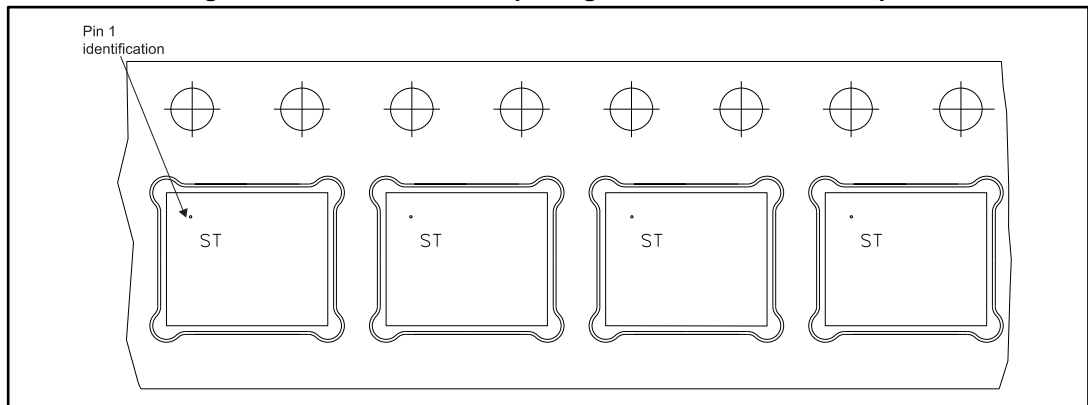
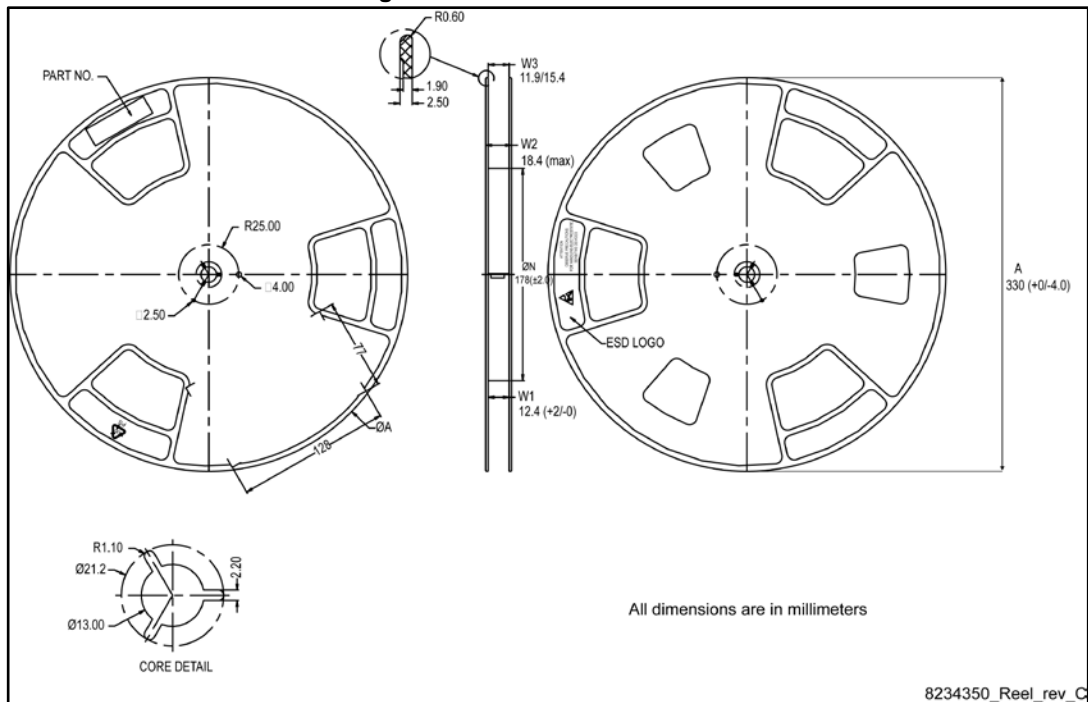


Figure 23: PowerFLAT™ 5x6 reel



## 5 Revision history

**Table 9: Document revision history**

Date	Revision	Changes
02-Aug-2013	1	First release.
18-Mar-2014	2	Updated VDS value in Table 2: Absolute maximum ratings and Table 4: On /off states. Updated Section 4: Package mechanical data. Minor text changes.
09-Apr-2015	3	Text edits and formatting changes throughout document On cover page: -updated title description -updated device 'Features' and 'Description' Updated section 1 Electrical ratings Updated section 2 Electrical characteristics Added section 2.1 Electrical characteristics (curves) Updated and renamed Section 4 Package information (was Package mechanical data) Updated and renamed Section 4.2 Packing information (was Section 5 Packaging mechanical data)
19-May-2015	4	In section 2.1 Electrical characteristics (curves): - updated Figure 8: Capacitance variations

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