## GENERAL DESCRIPTION

OB2203 is a highly integrated Quasi-Resonant (QR) controller optimized for high performance offline flyback converter applications.

At normal load condition, it operates in QR mode with minimum drain voltage switching. To meet the CISPR-22 EMI starting at 150KHz, the maximum switching frequency is internally limited to 130KHz. It operates in PFM mode for high power conversion efficiency at light load condition. When the loading is very small, the IC operates in 'Extended Burst Mode' to minimize the switching loss. As a result, lower standby power consumption and higher conversion efficiency is achieved.

A built-in P-channel MOSFET and its control are integrated to automatically turn on or off PFC stage according to the load conditions. When used with OB6563 (On-Bright's PFC controller), the standby power consumption of less than 400mW can be achieved in typical 150W SMPS.

OB2203 offers comprehensive protection coverage including Cycle-by-Cycle Current Limiting(OCP), VCC Under Voltage Lockout(UVLO), Over Voltage Protection(OVP), VCC Clamp, Gate Clamp, Over Load Protection(OLP), On-chip Thermal Shutdown, Programmable Soft Start, and External Latch Triggering, Max On-time Limit, etc.

OB2203 is offered in SOP-8 and DIP-8 packages.

## FEATURES

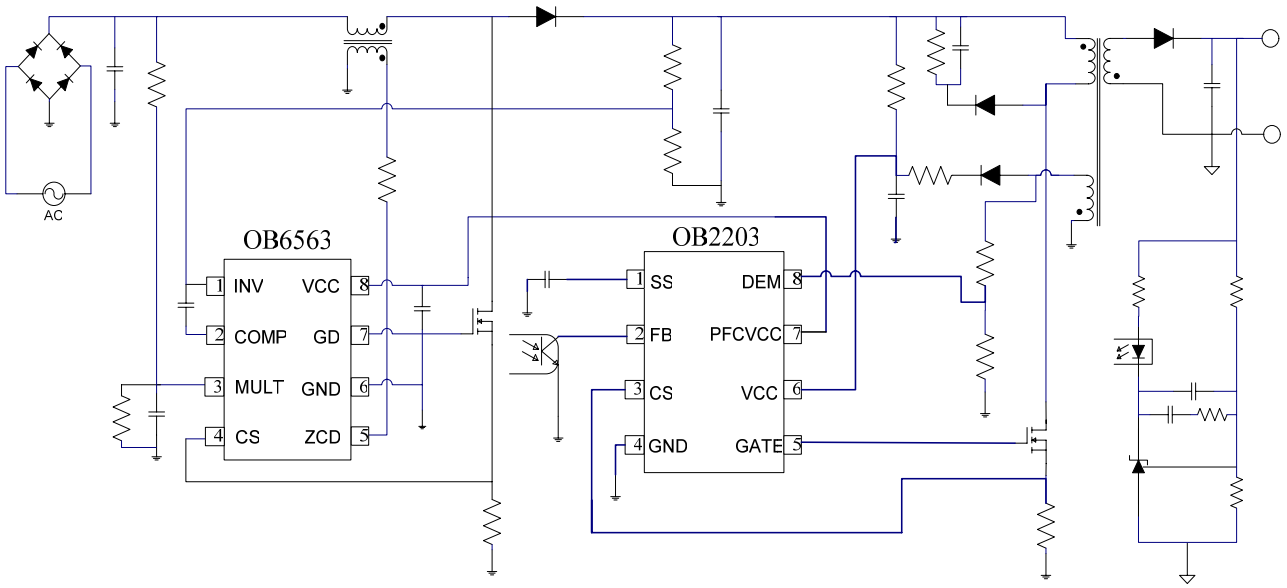
- Multi-Mode Operation
- Quasi-Resonant Operation at Normal Loading
- Pulse Frequency Modulation (PFM) Operation at Light Load
- Burst Mode at No Load
- Direct Control of the Power Supply of PFC Controller for Improved Standby Power at No/Light Load
- 40KHz Minimum Frequency Limit at QR Mode
- 130KHz Maximum Frequency Limit
- Internal Minimum T_off for Ringing Suppression
- 45us Maximum On Time Limit
- Adaptive Slope Compensation
- Internal Leading Edge Blanking
- Programmable Soft-start
- External Latch Triggering
- Internal Temperature Shutdown
- 1A Peak Current Sink/Source Capability
- Programmable Over Voltage Protection (OVP)

## APPLICATIONS

Offline AC/DC flyback converter for

- Power Adaptor and Open-frame SMPS
- LCD Monitor/TV/PC/Set-Top Box Power Supplies
- NB/DVD/Portable DVD Power Supplies

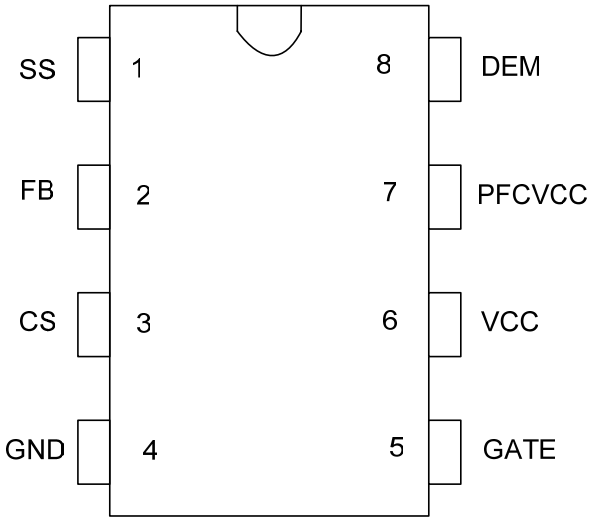
## TYPICAL APPLICATION



## GENERAL INFORMATION

### Pin Configuration

The pin map of OB2203 in DIP8 and SOP8 package is shown as below.




### Ordering Information

| Part Number | Description |
|---|---|
| OB2203AP | 8 Pin DIP, Pb free in Tube |
| OB2203CP | 8 Pin SOP, Pb free in Tube |
| OB2203CPA | 8 Pin SOP, Pb free in T&R |

**Note:** All Devices are offered in Pb-free Package if not otherwise noted.

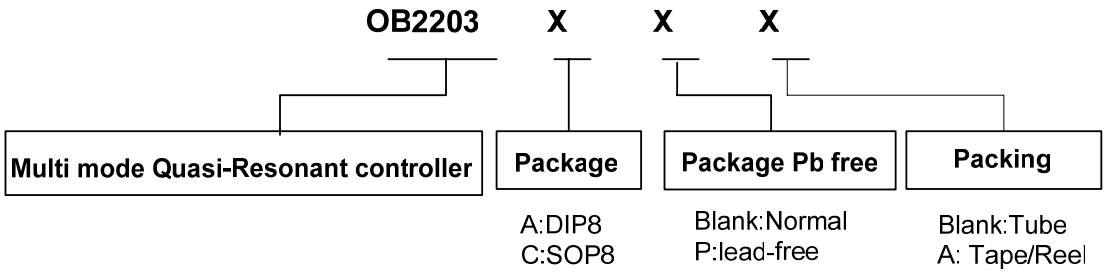
### Package Dissipation Rating

| Package | RθJA (°C/W) |
|---|---|
| DIP8 | 90 |
| SOP8 | 150 |

### Absolute Maximum Ratings

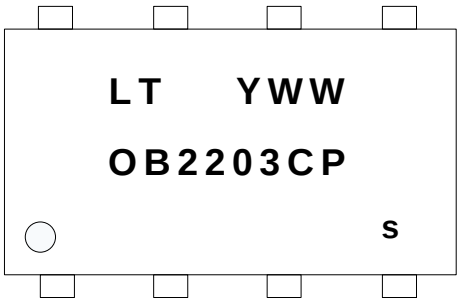
| Parameter | Value |
|---|---|
| VCC Zener Clamp Voltage | 31 V |
| VCC Clamp Continuous Current | 10 mA |
| SS Input Voltage | -0.3 to 7V |
| FB Input Voltage | -0.3 to 7V |
| CS Input Voltage | -0.3 to 7V |
| DEM Input Voltage | -0.3 to 7V |
| Min/Max Operating Junction Temperature $T_J$ | -20 to 150 °C |
| Min/Max Storage Temperature $T_{stg}$ | -55 to 150 °C |
| Lead Temperature (Soldering, 10secs) | 260 °C |

**Note:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



**Marking Information**

**SOP8**




Y: Year Code (0-9)

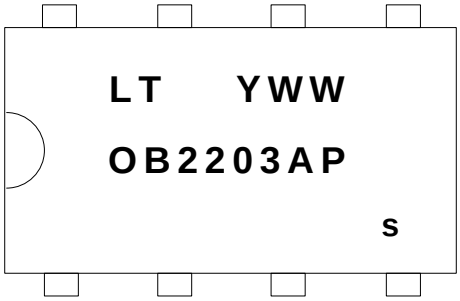
WW: Week Code (1-52)

C: SOP8

P:lead-free

s: internal code

**DIP8**




Y: Year Code (0-9)

WW: Week Code (1-52)

A: DIP8

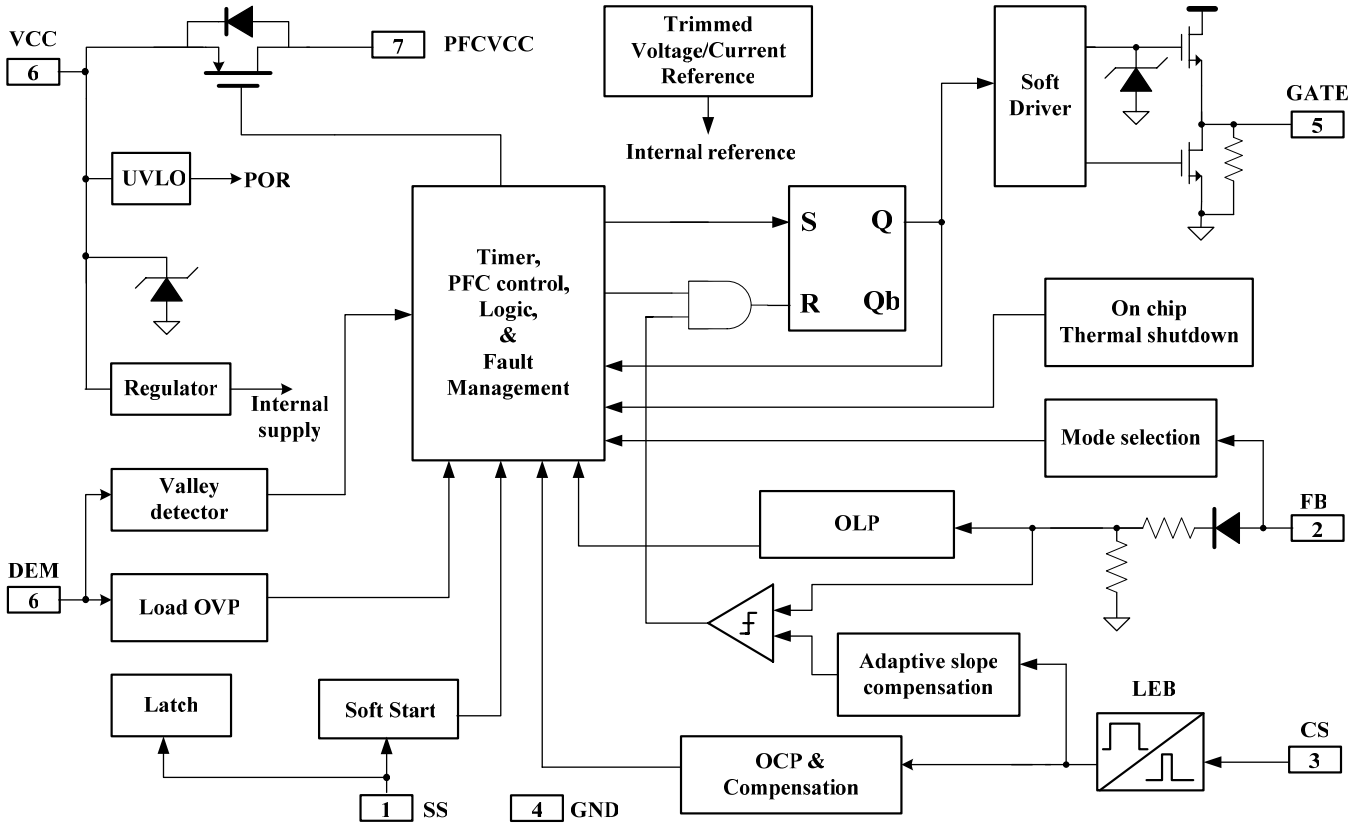
P:lead-free

s: internal code

## TERMINAL ASSIGNMENTS

| Pin Num | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | SS | I/O | Soft-start programming pin. Program the soft-start rate with a capacitor to ground. After soft-start, the pin's voltage is clamped at 2V. External latch input, latch will be triggered when SS pin voltage higher than 3.8V. |
| 2 | FB | I/O | Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 3. The voltage level at this pin also controls the mode of operation in one of the three modes: quasi-resonant (QR), pulse frequency modulation mode (PFM) and burst mode (BM). |
| 3 | CS | I | Current sense input. |
| 4 | GND | O | Ground for internal circuitry. |
| 5 | GATE | O | Totem-pole gate drive output for power MOSFET. |
| 6 | VCC | P | Chip DC power supply pin. |
| 7 | PFCVCC | P | This pin is a direct connection to the VCC pin via a low impedance switch. In standby and during the startup sequence, the switch is open and the PFCVCC is shut down. As soon as the auxiliary winding is stabilized, PFCVCC connects to the VCC pin and provides power supply to PFC controller. It goes down in any fault or at No/Light conditions. |
| 8 | DEM | I/O | Input from auxiliary winding for demagnetization timing. Also this pin is used for load over voltage protection (OVP). |

## BLOCK DIAGRAM




## RECOMMENDED OPERATING CONDITION

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VCC | VCC Supply Voltage | 12 | 23 | V |
| $T_A$ | Operating Ambient Temperature | -20 | 85 | °C |

## ELECTRICAL CHARACTERISTICS

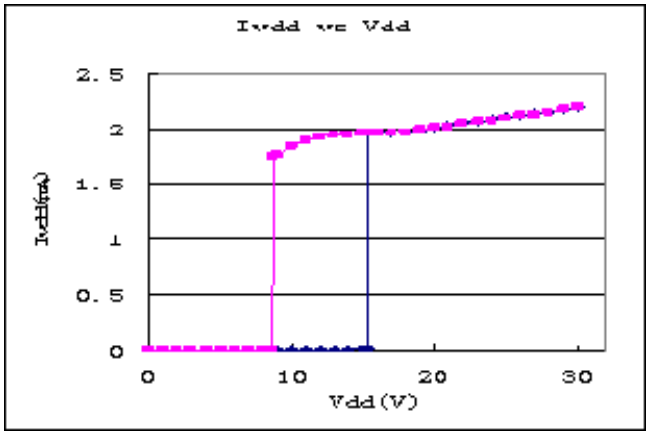
($T_A$ = 25°C, VCC=16V, if not otherwise noted)

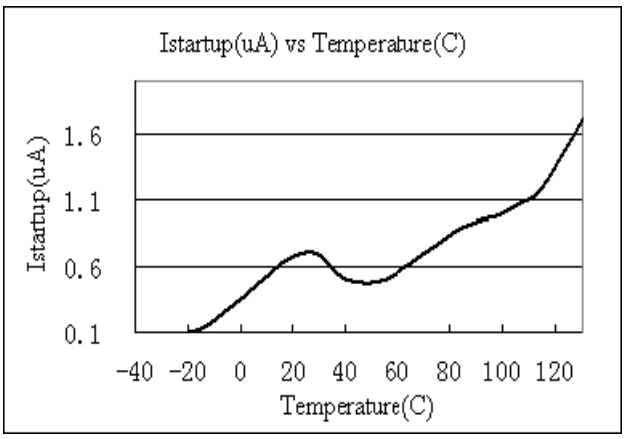
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage (VCC) Section** | | | | | | |
| I_VCC_Startup | VCC Start up Current | VCC =13.5V, Measure current into VCC | - | 5 | 15 | uA |
| I_VCC_quiet | Operation Current without switching | FB=3V, CS is floating, | - | 2.0 | 3.0 | mA |
| I_VCC_operation | Operation current with switching | FB=3V, Fsw=40KHz, 1nF load at GATE | - | 3.0 | 4.0 | mA |
| UVLO(ON) | VCC Under Voltage Lockout Enter | | 7.5 | 8.5 | 9.5 | V |
| UVLO(OFF) | VCC Under Voltage Lockout Exit (Startup) | | 14 | 15 | 16 | V |
| OVP(ON) | VCC Over Voltage Protection Enter | | 29 | 31 | 33 | V |
| VCC_Clamp | VCC Zener Clamp Voltage | I(VCC ) = 5 mA | 30 | 32 | 34 | V |
| **Feedback Input Section(FB Pin)** | | | | | | |
| $A_{VCS}$ | PWM Input Gain | $\Delta V_{FB} / \Delta V_{cs}$ | - | 3.5 | - | V/V |
| $V_{FB}$_Open | FB Open Voltage | | 4.8 | 5.3 | 6.0 | V |
| $I_{FB}$_Short | FB pin short circuit current | Short FB pin to GND, measure current | 1.0 | 1.5 | - | mA |
| $V_{TH}$_0D | Zero Duty Cycle FB Threshold Voltage | | | | 0.95 | V |
| $V_{TH}$_PFM_H | PFM mode up threshold | | | 1.45 | | V |
| $V_{TH}$_PFM_L | PFM mode down threshold | | | 1.0 | | V |
| $V_{TH}$_BM_on | Burst Mode on threshold | | | 1.0 | | V |
| $V_{TH}$_BM_off | Burst Mode off threshold | | | 0.9 | | V |
| $V_{TH}$_PFC_GTS | Threshold for PFC to go to standby | | | 1.35 | | V |
| $V_{TH}$_PFC_on | Threshold for PFC to leave standby mode | | | 1.45 | | V |
| $V_{TH}$_PL | Power Limiting FB Threshold Voltage | | | 4.4 | | V |
| $T_D$_PL | Power limiting Debounce Time | | 60 | 80 | 120 | mSec |
| $Z_{FB}$_IN | Input Impedance | | | 4 | | Kohm |
| **Current Sense Input(CS Pin) Section** | | | | | | |
| T_blanking | CS Input Leading Edge Blanking Time | | | 350 | | nSec |
| $V_{TH}$_OC_0 | Internal current limiting threshold | Zero duty cycle | 0.43 | 0.45 | 0.47 | V |
| $V_{TH}$_OC_60% | Internal current limiting threshold | 60% duty cycle | | 0.80 | | V |
| $T_D$_OC | Over Current | CL=1nf at GATE, | | 100 | 160 | nSec |

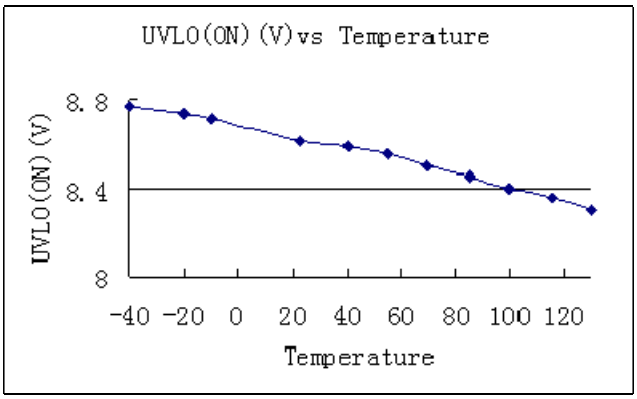
| | | | | | | |
|---|---|---|---|---|---|---|
| | Detection and Control Delay | | | | | |
| **Demagnetization Detection Section** | | | | | | |
| $V_{TH}$_DEM | Demagnetization comparator threshold voltage | | 10 | 75 | 30 | mV |
| $V_{TH}$_DEM_hyst | Hysteresis for DEM comparator | | | 20 | | mV |
| $V_{DEM}$_clamp(neg) | Negative clamp voltage | | | -0.7 | | V |
| $V_{DEM}$_clamp(pos) | Positive clamp voltage | | | 5.8 | | V |
| $T_{supp}$ | Suppression of the transformer ringing at start of secondary stroke | | 1.5 | 2 | 2.5 | usec |
| $T_{OUT}$ | Timeout after last demag transistion | | 4 | 5 | 6 | usec |
| $T_{DEM\_delay}$ | Demag propagation delay | | | 150 | | nsec |
| $V_{TH}$_OVP | OVP trigger point | | | 3.75 | | V |
| T_ovp_plateau | OVP plateau sampling after switching off | | 1.5 | 2 | 2.5 | usec |
| N_true_OVP | Number of subsequent cycles to be true OVP | | | 4 | | Cycle |
| **Soft Start Section** | | | | | | |
| Iss | Soft start charge current | | 8.0 | 10 | 12 | uA |
| $V_{TH}$_ss_over | Soft start over threshold voltage | | | 2.2 | | V |
| $I_{SS}$_clamp_sink | Maximum sink current capability when SS is clamped | | 80 | 120 | 200 | uA |
| $V_{SS}$_clamp | SS pin high clamp voltage | | | 5.8 | | V |
| **Timer Section** | | | | | | |
| $F_{\_burst}$ | Burst mode switching frequency | | | 22 | | KHz |
| F_QR_clamp_h | Frequency high clamp in QR mode | | 117 | 130 | 143 | KHz |
| F_QR_clamp_l | Frequency low clamp in QR mode | | 35 | 40 | 45 | KHz |
| Ton_max | Maximum on time | | 30 | 45 | 55 | usec |
| Toff_max | Maximum off time | | 30 | 45 | 55 | usec |
| G_PFM | PFM mode frequency modulation slope versus control voltage | | | 240 | | KHz/V |
| **Thermal Protection** | | | | | | |
| T_shutdown | Thermal shutdown temperature | | 130 | 140 | 150 | ◦C |
| **Latch Protection** | | | | | | |
| V_latch_trigger | Latch trigger threshod | SS pin pull up current | | 3.8 | | V |

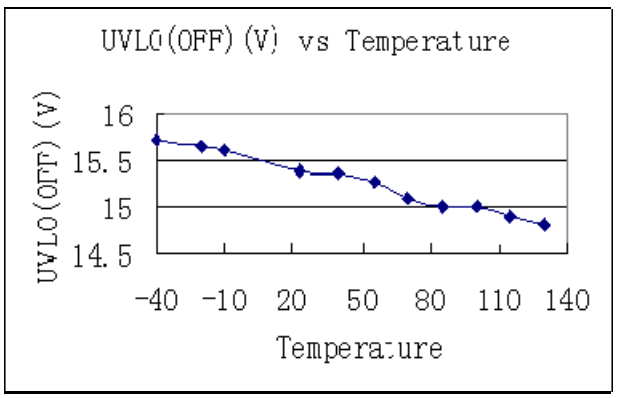
| | | | | | | |
|---|---|---|---|---|---|---|
| | voltage at SS pin | should be larger than 200uA | | | | |
| V_latch_release | VCC latch release voltage | | 5.5 | 6 | 6.5 | V |
| Ivdd(latch) | VCC current when latch off | VCC=V_latch_release+1 V | | 40 | | uA |
| **PFCVCC section** | | | | | | |
| Rdson | On-resistance of PMOS switch | | 10 | 20 | 30 | Ω |
| T_PFC_GTS | PFC go to standby debounce time | | 100 | 125 | 140 | ms |
| T_PFC_ON | PFC ON debounce time | | 4 | 8 | 12 | mS |
| **Gate Drive Output** | | | | | | |
| VOL | Output Low Level | Io = 100 mA (sink) | | | 1 | V |
| VOH | Output High Level | Io = 100 mA (source) | 7.5 | | | V |
| VG_Clamp | Output Clamp Voltage Level | VCC=20V | 15.5 | 16.5 | 17.5 | V |
| T_r | Output Rising Time | CL = 1nf | | 50 | | nSec |
| T_f | Output Falling Time | CL = 1nf | | 20 | | nSec |

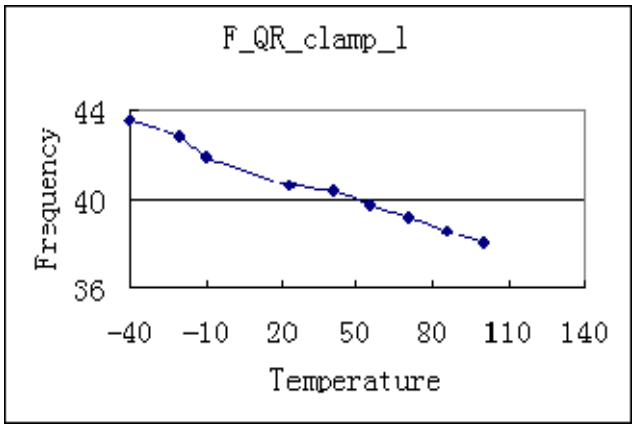
## CHARACTERIZATION PLOTS

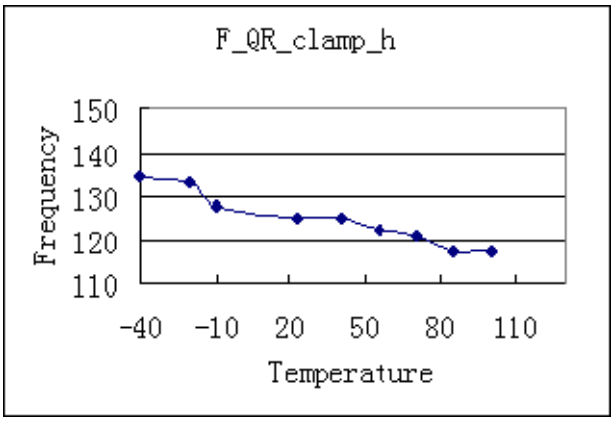


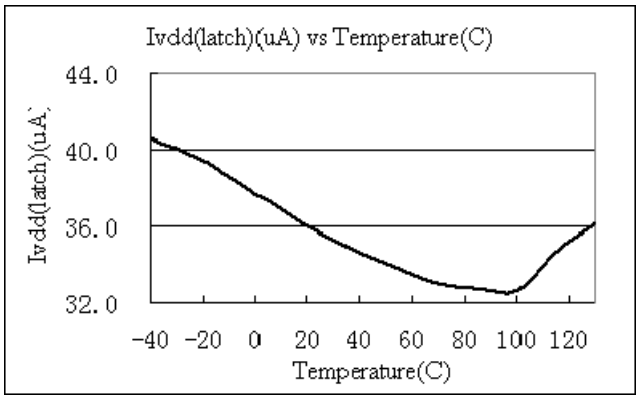



## OPERATION DESCRIPTION

Quasi-Resonant (QR) converter typically features lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency. OB2203 is a highly integrated QR controller optimized for offline flyback converter applications. The built-in advanced energy saving with high level protection features provide cost effective solutions for energy efficient power supplies.

- **Startup Current and Start up Control**

Startup current of OB2203 is designed to be very low so that VCC could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VCC capacitor to provide a fast startup and yet low power dissipation design solution.

- **Operating Current**

The operating current of OB2203 is as low as 2.3mA. Good efficiency is achieved by the low operating current together with extended burst mode control schemes at No/light conditions.

- **Multi-Mode Operation for High Efficiency**

OB2203 is a multi-mode QR controller. The controller changes the mode of operation according to FB voltage, which reflects the line and load conditions.

■ Under normal operating conditions (FB>Vth2, Figure 1), the system operates in QR mode. The frequency variation in QR mode is limited to the range of 40KHz ~ 130KHz due to the fact that frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when 130KHz frequency clamping is reached. In contrast, the system may actually work in CCM when 40KHz frequency clamping is reached. System design should be optimized such that the operation frequency is within the range specified at full loading conditions and in universal AC line input range.

■ At light load condition (Vth1<VFB<Vth2, Figure 1), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. In PFM mode, the "ON" time in a switching cycle is fixed and the system modulates the frequency according to the load conditions. Generally, in flyback converter, the decreasing of loading results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when loading decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency foldback is realized and high power conversion efficiency is achieved.

■ At zero load or very light load conditions (VFB<Vth1), the system operates in On-Bright's proprietary "extended burst mode". In this condition, voltage at FB is below burst mode threshold level, Vth1. The Gate drive output switches only when VCC voltage drops below a preset level or FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. In extended burst mode, the switching frequency is fixed to 22KHz, in this way, possible audio noise is eliminated.

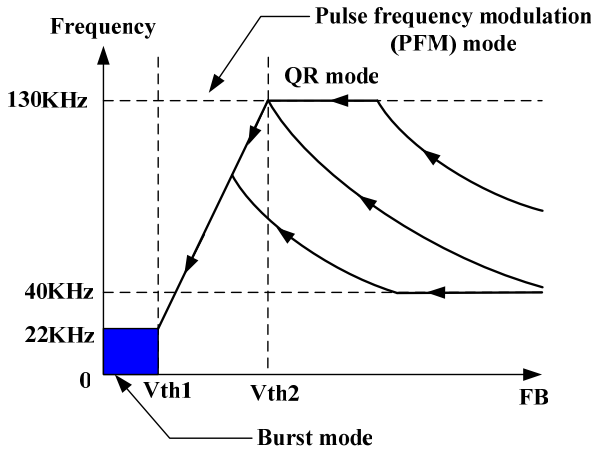



Figure 1

- **Demagnetization Detection**

The core reset is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. This voltage features a flyback polarity. A new cycle starts when the power switch is activated. After the on time (determined by the CS voltage and FB), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_p C_d}$ , where $L_p$ is the

primary self inductance of the transformer and $C_d$ is the capacitance on the drain node.

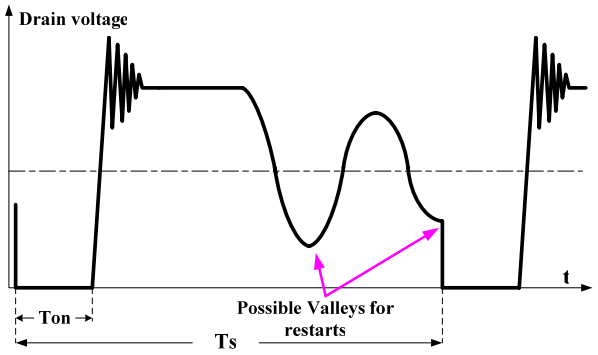



Figure 2

The typical detection level is fixed at 75mV at the DEM pin. Demagnetization is recognized by detection of a possible "valley" when the voltage at DEM is below 75mV in falling edge. DEM detection is suppressed during the first $T_{supp}$ time (typical value of 2us). This suppression is necessary in applications where the transformer has a large leakage inductance and at low output voltages or start-up.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2203 current mode control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer needed. The current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Adaptive Slope Compensation at Large Load**

The slop compensation to ensure system stable operation is active only at large load condition. At large load conditions (such as startup), the switching frequency can be low clamped to 40KHz and the system will actually work in CCM mode. To prevent the possible unstable operation and the sub-harmonic oscillation, an internal synchronized slope compensation is added to the current loop. The internal synchronized slope compensation is disabled at normal or light load, in such condition, the system will work in either QR or DCM mode.

- **Maximum and Minimum On-Time**

The minimum on-time of the system is determined by the LEB time (typical 350ns). The IC limits the on-time to a maximum time of 45us.

- **Ringing Suppression Timer**

A ringing suppression timer is implemented. In normal operation, the ringing suppression timer starts when CS reaches the feedback voltage FB, the gate drive GATE is set to low. During the ringing suppression time, gate drive GATE remains in low state and cannot turn power switch on gain. The ringing suppression is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup. In OB2203, the ringing suppression timer is set to 2us internally.

- **PFC VCC power on/off control**

In medium to large power applications, PFC pre-converter is required and PFC controller is powered by PWM auxiliary power supply. PFCVCC pin is directly connected to VCC pin by an internal low impedance power switching, thus no external components are needed. PFCVCC is shut down in any of the following conditions: any fault condition, No load/light load condition, soft start sequence and VCC voltage less than 12V.

- **Maximum and Minimum Frequency Clamp in QR operation**

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, when the output power decreases, the switching frequency can become rather high without limiting. To meet the CISPR-22 EMI limit starting at 150KHz, the maximum switching frequency in OB2203 is internally limited to 130KHz. In addition to up clamping, the switching frequency is also low clamped to 40KHz in QR mode.

- **On chip Thermal shutdown**

OB2203 provides an on chip thermal shutdown. The IC will stop switching when the junction temperature exceeds the thermal shutdown temperature, typically 140 °C. The IC resumes normal operation when the junction temperature decreased by 20 °C

- **External latch trip point**

By externally forcing a level on pin SS (e.g.., with a signal coming from a temperature sensor) greater than 3.8V, OB2203 can be permanently latched-off. To resume normal operation, VCC voltage should

go below 6V, which implies to unplug the SMPS form the mains.

- **OCP compensation for CCM/DCM**

A proprietary OCP compensation is provided for better OCP performance in the universal input range. Comparing to conventional OCP compensation where the gate delay is compensated, more sophisticated compensation is provided to also compensate the OCP at different line voltage since the switching frequency varies with line voltage. In this way, a more accurate OCP is achieved.

- **Over voltage protection (OVP)**

An over voltage protection (OVP) is implemented by sensing the auxiliary winding voltage at DEM pin during the flyback phase. The auxiliary winding voltage is a well-defined replica of the output voltage. The OVP works by sampling the plateau voltage at DEM pin during the flyback phase. A 2 us internal delay (plateau sampling) guarantees a clean plateau, provided that the leakage inductance ringing has been fully damped.

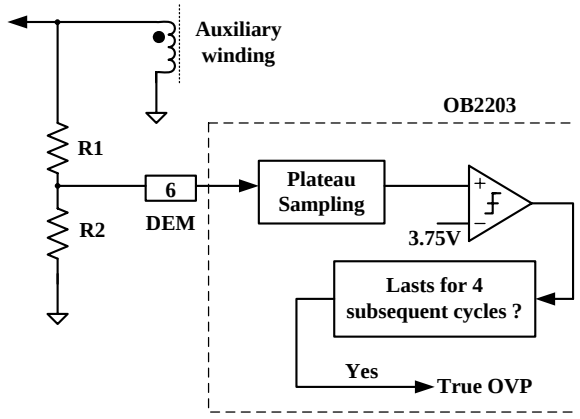



Figure 3

If the sampled plateau voltage exceeds the OVP trip level (3.75V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 4 cycles, the controller assumes a true OVP and it enters a latch off mode and stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level less than 4 successive cycles, the internal counter will be cleared and no fault is asserted.

- **Overload Operation**

When over load (for example, short circuit) occurs, the feedback current is below minimum value and a fault is detected. If this fault is present for more than 80ms, the controller enters an auto-recovery soft burst mode. All pulses are stopped, VCC will drops below UVLO and the controller will try to restart with the power on soft start. The SMPS enters the burst sequence and it resumes operation once the fault disappears.

- **Programmable Soft Start**

OB2203 features a programmable soft start to soften the constraints in the power supply during the startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), an internal trimmed 10 uA current is sourced from SS pin and charges the external programming capacitor, the peak current is then gradually increased from zero. When SS pin reaches 2.2V, soft start process is over.

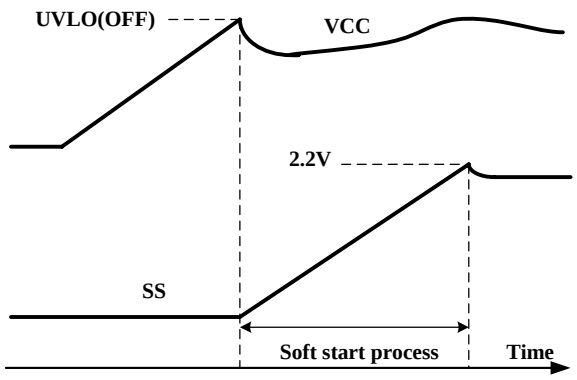



Figure 4

During the soft start process, there is a low frequency (40KHz) clamping to avoid the system switching frequency going too low. Every restart attempt is followed by soft start sequence.

- **Gate Drive**

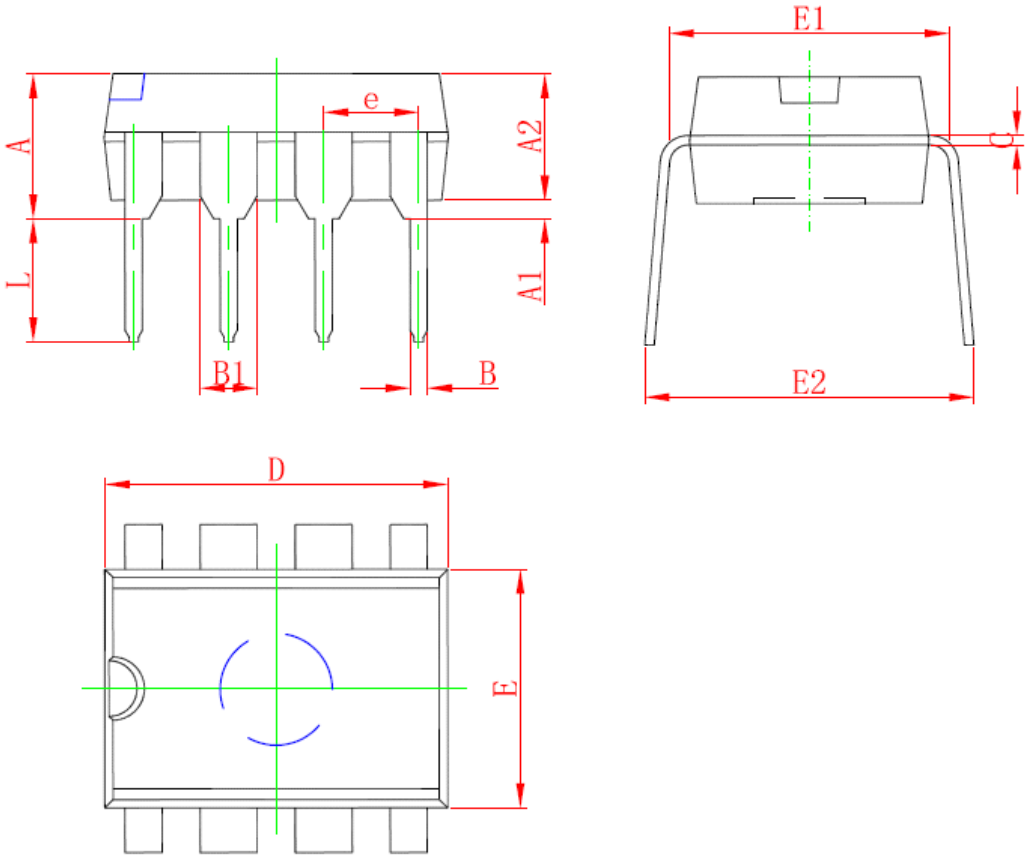
The Gate pin is connected to the gate of an external MOSFET for power switch control. Too weak the gate drive results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 15V clamp is added for MOSFET gate protection at high VCC voltage.

## PACKAGE MECHANICAL DATA

**8-Pin Plastic DIP**

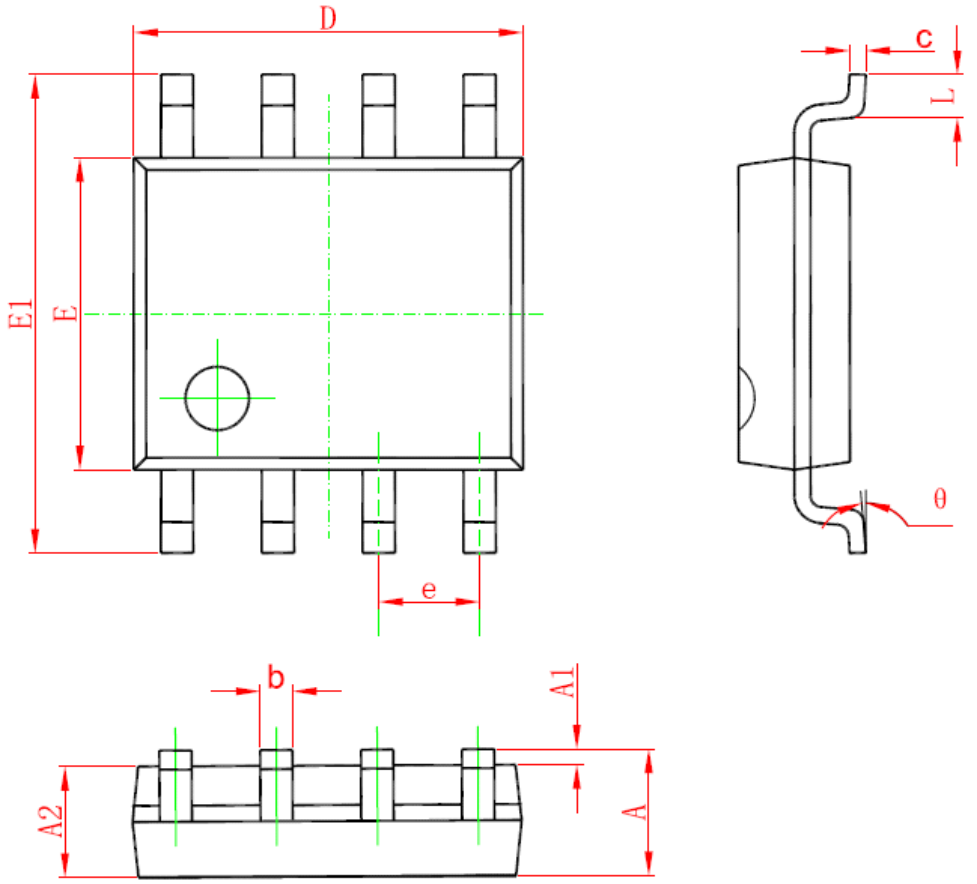
DIP8 PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.710 | 4.310 | 0.146 | 0.170 |
| A1 | 0.500 | | 0.020 | |
| A2 | 3.200 | 3.600 | 0.126 | 0.142 |
| B | 0.350 | 0.650 | 0.014 | 0.026 |
| B1 | 1.524 (BSC) | | 0.060 (BSC) | |
| C | 0.200 | 0.360 | 0.008 | 0.014 |
| D | 9.000 | 9.500 | 0.354 | 0.374 |
| E | 6.200 | 6.600 | 0.244 | 0.260 |
| E1 | 7.320 | 7.920 | 0.288 | 0.312 |
| e | 2.540 (BSC) | | 0.100 (BSC) | |
| L | 3.000 | 3.600 | 0.118 | 0.142 |
| E2 | 8.200 | 9.000 | 0.323 | 0.354 |

**8-Pin Plastic SOP**

SOP8 PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.300 | 1.550 | 0.051 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.150 | 0.185 | 0.203 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |