Datasheet, Version 1.2, 02 Sep 2005

F3

ICE3AS02 / ICE3BS02
ICE3AS02G / ICE3BS02G

Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell

Power Management & Supply

Never stop thinking.

F3

Revision History:	**2005-09-02**	Datasheet
Previous Version:1.1		
Page	Subjects (major changes since last revision)	
16	revise max operating V_{Vcc} to 21V	

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

Edition 2005-09-02

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

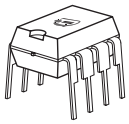
Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

ICE3AS02 / ICE3BS02
ICE3AS02G / ICE3BS02G

Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell



PG-DIP-8

PG-DSO-8

Product Highlights

- **Active Burst Mode to reach the lowest Standby Power Requirements < 100mW**
- **Protection features (Auto Restart Mode) to increase robustness and safety of the system**
- **Adjustable Blanking Window for high load jumps to increase system reliability**
- **PB-free Plating and RoHS compilant**

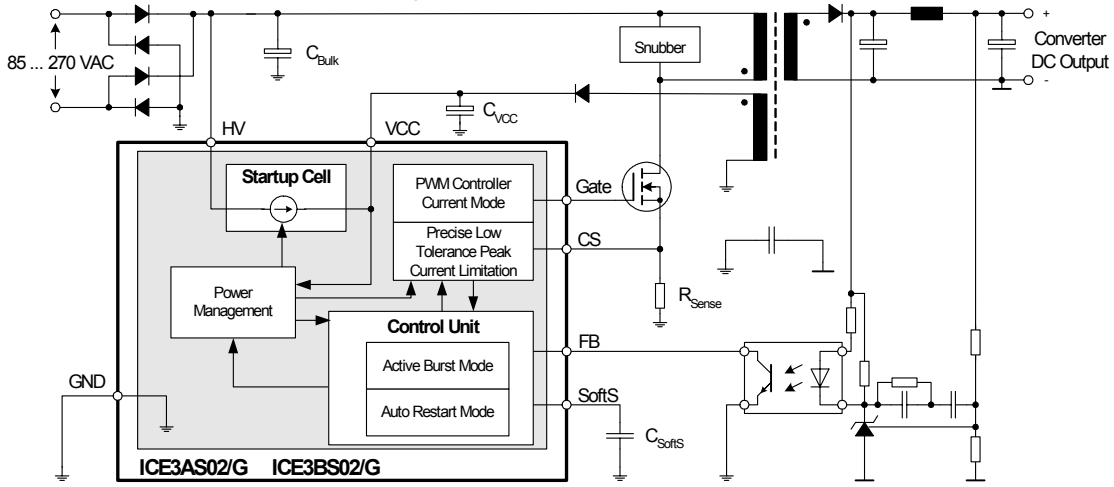
Features

- 500V Startup Cell switched off after Start Up
- Active Burst Mode for lowest Standby Power @ light load controlled by Feedback Signal
- Fast load jump response in Active Burst Mode
- 100/67kHz internally fixed switching frequency
- Auto Restart Mode for Overtemperature Detection
- Auto Restart Mode for VCC Overvoltage Detection
- Auto Restart Mode for Overload and Open Loop
- Auto Restart Mode for VCC Undervoltage
- Blanking Window for short duration high current
- User defined Soft Start
- Minimum of external components required
- Max Duty Cycle 72%
- Overall tolerance of Current Limiting < ±5%
- Internal PWM Leading Edge Blanking
- Soft switching for low EMI

Description

The F3 Controller provides Active Burst Mode to reach the lowest Standby Power Requirements <100mW at no load. As the controller is always active during Active Burst Mode, there is an immediate response on load jumps without any black out in the SMPS. In Active Burst Mode the ripple of the output voltage can be reduced <1%. Furthermore, to increase the robustness and safety of the system, the device enters into Auto Restart Mode in the cases of Overtemperature, VCC Overvoltage, Output Open Loop or Overload and VCC Undervoltage. By means of the internal precise peak current limitation, the dimension of the transformer and the secondary diode can be lowered which leads to more cost efficiency. An adjustable blanking window prevents the IC from entering Auto Restart Mode or Active Burst Mode unintentionally in case of high load jumps.

Typical Application



Type	F_{OSC}	Package
ICE3AS02	100kHz	PG-DIP-8
ICE3BS02	67kHz	PG-DIP-8
ICE3AS02G	100kHz	PG-DSO-8
ICE3BS02G	67kHz	PG-DSO-8

Table of Contents **Page**

1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DIP-8

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	CS	Current Sense
4	HV	High Voltage Input
5	HV	High Voltage Input
6	Gate	Driver Stage Output
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

1.2 Pin Configuration with PG-DSO-8

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	CS	Current Sense
4	Gate	Driver Stage Output
5	HV	High Voltage Input
6	N.C.	Not connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

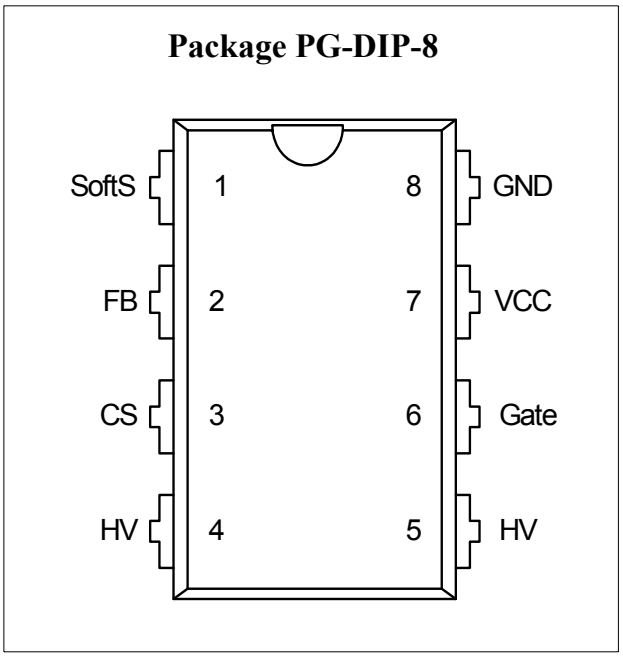


Figure 1 Pin Configuration PG-DIP-8(top view)

Note: Pin 4 and 5 are shorted within the DIP 8 package.

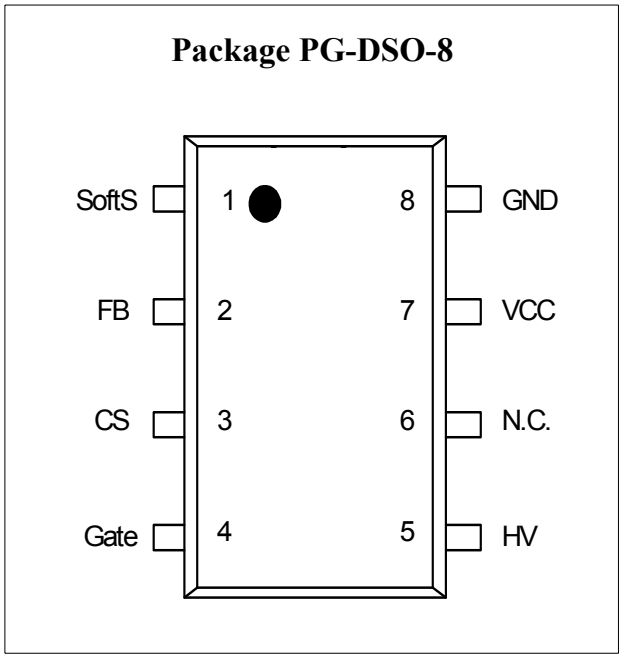


Figure 2 Pin Configuration PG-DSO-8(top view)

1.3 Pin Functionality

SoftS (Soft Start & Auto Restart Control)

The SoftS pin combines the functions of Soft Start during Start Up and error detection for Auto Restart Mode. These functions are implemented and can be adjusted by means of an external capacitor at SoftS to ground. This capacitor also provides an adjustable blanking window for high load jumps, before the IC enters into Auto Restart Mode.

FB (Feedback)

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle. The FB-Signal controls in case of light load the Active Burst Mode of the controller.

CS (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the external PowerMOS. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.

Gate

The Gate pin is the output of the internal driver stage connected to the Gate of an external PowerMOS.

HV (High Voltage)

The HV pin is connected to the rectified DC input voltage. It is the input for the integrated 500V Startup Cell.

VCC (Power supply)

The VCC pin is the positive supply of the IC. The operating range is between 8.5V and 21V.

GND (Ground)

The GND pin is the ground of the controller.

2 Representative Blockdiagram

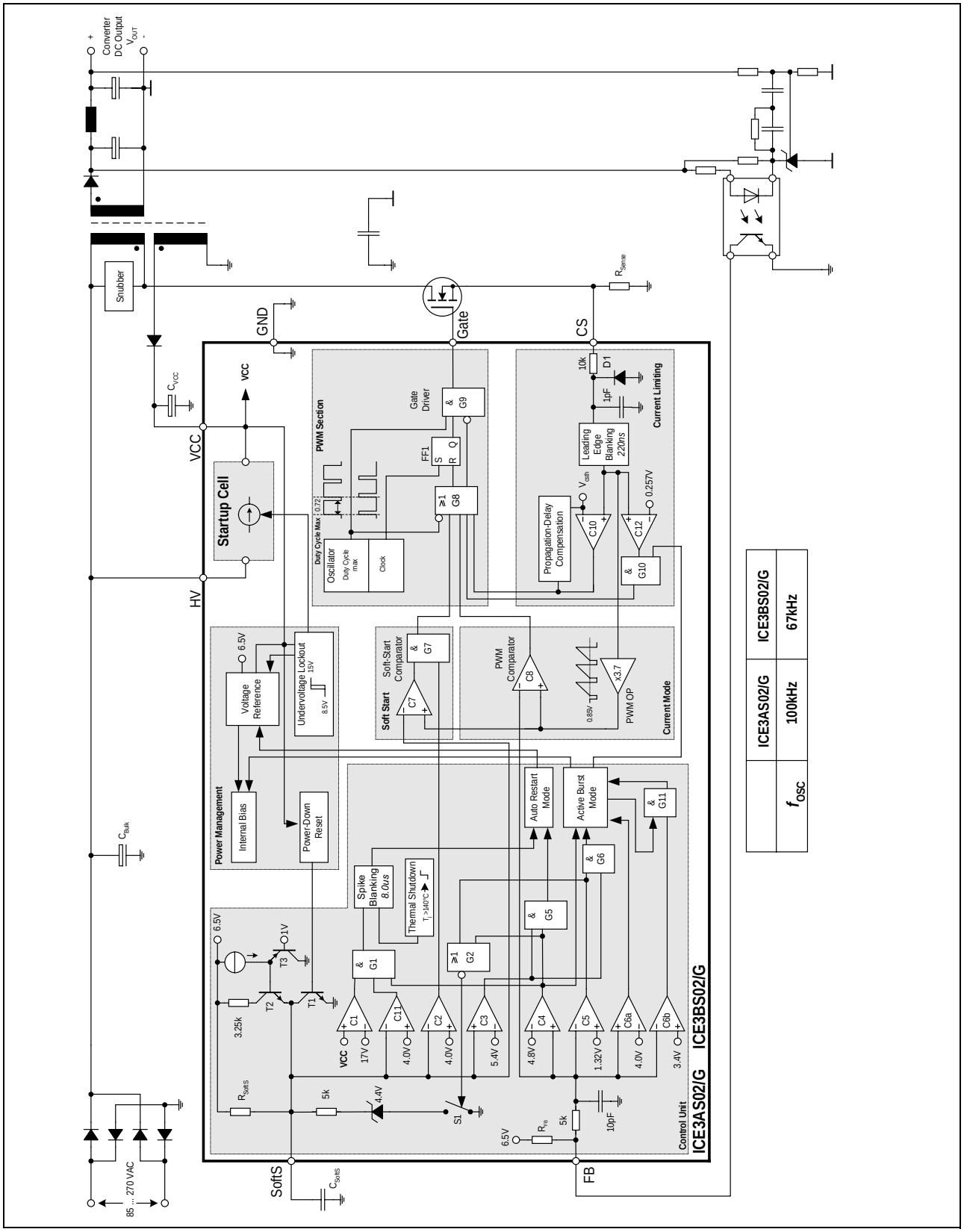


Figure 3 Representative Blockdiagram

3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

3.1 Introduction

The F3 is the further development of the F2 to meet the requirements for the lowest Standby Power at minimum load and no load conditions. A new fully integrated Standby Power concept is implemented into the IC in order to keep the application design easy. Compared to F2 no further external parts are needed to achieve the lowest Standby Power. An intelligent Active Burst Mode is used for this Standby Mode. After entering this mode there is still a full control of the power conversion by the secondary side via the same optocoupler that is used for the normal PWM control. The response on load jumps is optimized. The voltage ripple on V_{out} is minimized. V_{out} is further on well controlled in this mode.

The usually external connected RC-filter in the feedback line after the optocoupler is integrated in the IC to reduce the external part count.

Furthermore a high voltage startup cell is integrated into the IC which is switched off once the Undervoltage Lockout on-threshold of 15V is exceeded. The external startup resistor is no longer necessary. Power losses are therefore reduced. This increases the efficiency under light load conditions drastically.

The Soft-Start capacitor is also used for providing an adjustable blanking window for high load jumps. During this time window the overload detection is disabled. With this concept no further external components are necessary to adjust the blanking window.

An Auto Restart Mode is implemented in the IC to reduce the average power conversion in the event of malfunction or unsafe operating condition in the SMPS system. This feature increases the system's robustness and safety which would otherwise lead to a destruction of the SMPS. Once the malfunction is removed, normal operation is automatically initiated after the next Start Up Phase.

The internal precise peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation. Therefore the maximum power is nearly independent on the input voltage which is required for wide range SMPS. There is no need for an extra over-sizing of the SMPS, e.g. the transformer or PowerMOS.

3.2 Power Management

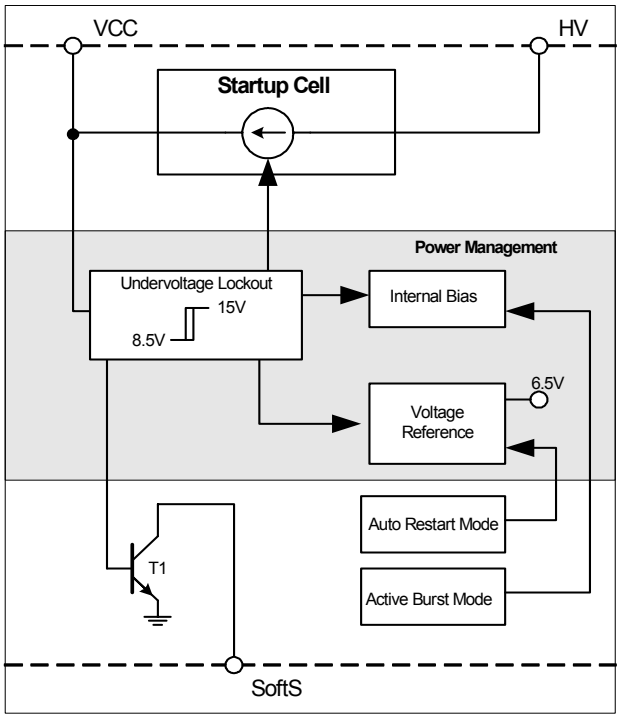


Figure 4 Power Management

The Undervoltage Lockout monitors the external supply voltage V_{VCC}. When the SMPS is plugged to the main line the internal Startup Cell is biased and starts to charge the external capacitor C_{VCC} which is connected to the VCC pin. This VCC charge current which is provided by the Startup Cell from the HV pin is 1.05mA. When V_{VCC} exceeds the on-threshold V_{CCon}=15V the internal voltage reference and bias circuit are switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore no power losses present due to the connection of the Startup Cell to the bus voltage (HV). To avoid uncontrolled ringing at switch-on a hysteresis is implemented. The switch-off of the controller can only take place after Active Mode was entered and V_{VCC} falls below 8.5V.

The maximum current consumption before the controller is activated is about 160µA.

When V_{VCC} falls below the off-threshold V_{CCoff}=8.5V the internal reference is switched off and the Power Down reset let T1 discharging the soft-start capacitor C_{SoftS} at pin SoftS. Thus it is ensured that at every startup cycle the voltage ramp at pin SoftS starts at zero.

The internal Voltage Reference is switched off if Auto Restart Mode is entered. The current consumption is then reduced to 300µA.

Once the malfunction condition is removed, this block will then turn back on. The recovery from Auto Restart Mode does not require disconnecting the SMPS from the AC line.

When Active Burst Mode is entered, the internal Bias is switched off in order to reduce the current consumption to below 1.05mA while keeping the Voltage Reference active as this is necessary in this mode.

3.3 Startup Phase

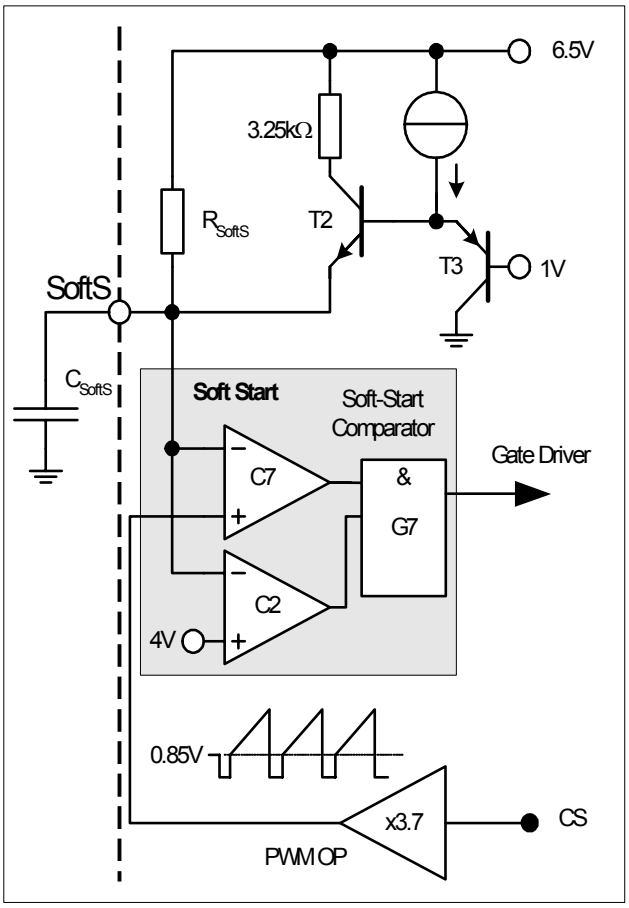


Figure 5 Soft Start

At the beginning of the Startup Phase, the IC provides a Soft Start duration whereby it controls the maximum primary current by means of a duty cycle limitation. A signal V_{SoftS} which is generated by the external capacitor C_{Softs} in combination with the internal pull up resistor R_{SoftS}, determines the duty cycle until V_{SoftS} exceeds 4V.

When the Soft Start begins, C_{SoftS} is immediately charged up to approx. 1V by T2. Therefore the Soft Start Phase takes place between 1V and 4V. Above V_{SoftsS} = 4V there is no longer duty cycle limitation DC_{max} which is controlled by comparator C7 since comparator C2 blocks the gate G7 (see Figure 5). This maximum charge current in the very first stage when V_{SoftS} is below 1V, is limited to 1.32mA.

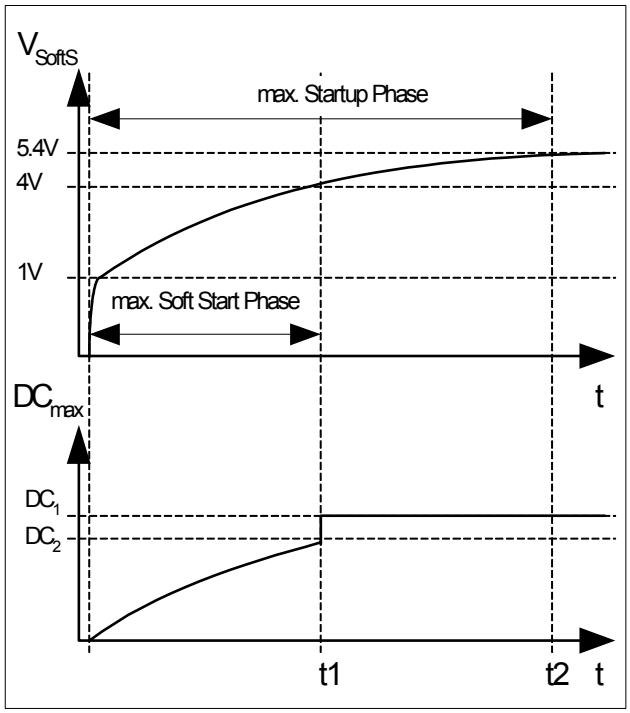


Figure 6 Startup Phase

By means of this extra charge stage, there is no delay in the beginning of the Startup Phase when there is still no switching. Furthermore Soft Start is finished at 4V to have faster the maximum power capability. The duty cycles DC_1 and DC_2 are depending on the mains and the primary inductance of the transformer. The limitation of the primary current by DC_2 is related to V_{SoftS} = 4V. But DC_1 is related to a maximum primary current which is limited by the internal Current Limiting with CS = 1V. Therefore the maximum Startup Phase is divided into a Soft Start Phase until t1 and a phase from t1 until t2 where maximum power is provided if demanded by the FB signal.

3.4 PWM Section

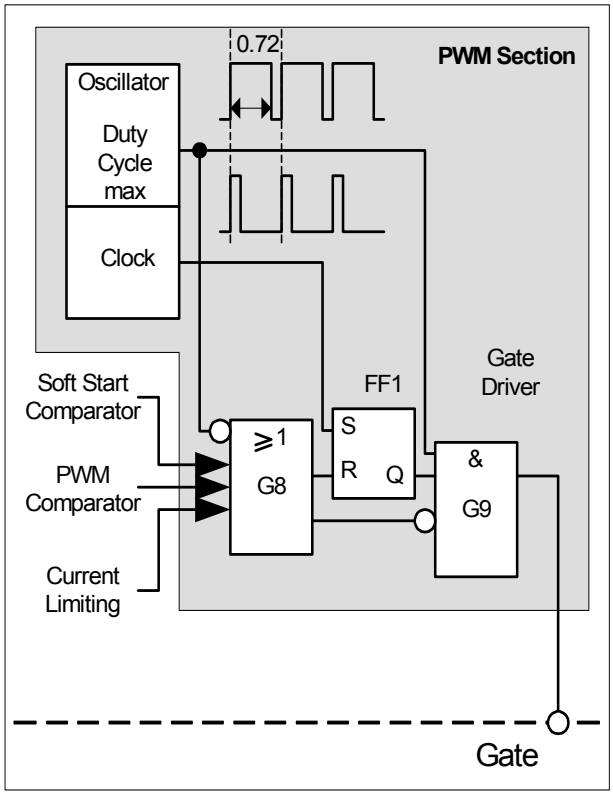


Figure 7 PWM Section

3.4.1 Oscillator

The oscillator generates a fixed frequency. The switching frequency for ICE3AS02/G is f_{OSC} = 100kHz and for ICE3BS02/G f_{OSC} = 67kHz. A resistor, a capacitor and a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of D_{max}=0.72.

3.4.2 PWM-Latch FF1

The oscillator clock output provides a set pulse to the PWM-Latch when initiating the external Power Switch conduction. After setting the PWM-Latch can be reset by the PWM comparator, the Soft Start comparator or the Current-Limit comparator. In case of resetting, the driver is shut down immediately.

3.4.3 Gate Driver

The Gate Driver is a fast totem pole gate drive which is designed to avoid cross conduction currents and which is equipped with a zener diode Z1 (see Figure 8) in order to improve the control of the Gate attached power transistors as well as to protect them against undesirable gate overvoltages.

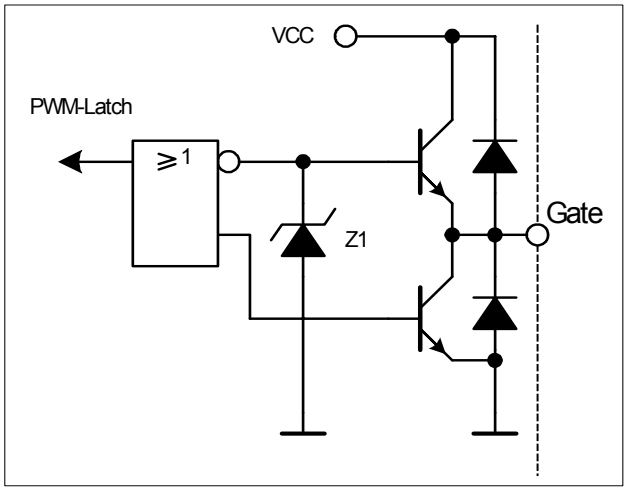


Figure 8 Gate Driver

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when exceeding the external Power Switch threshold. This is achieved by a slope control of the rising edge at the driver's output (see Figure 9).

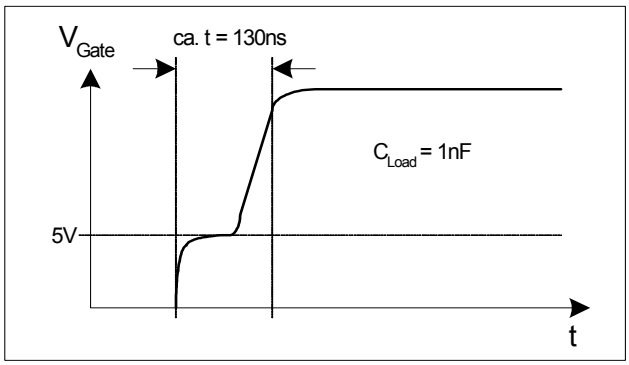


Figure 9 Gate Rising Slope

Thus the leading switch on spike is minimized. When the external Power Switch is switched off, the falling shape of the driver is slowed down when reaching 2V to prevent an overshoot below ground. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

During powerup when VCC is below the undervoltage lockout threshold V_{VCCoff}, the output of the Gate Driver is low to disable power transfer to the secondary side.

3.5 Current Limiting

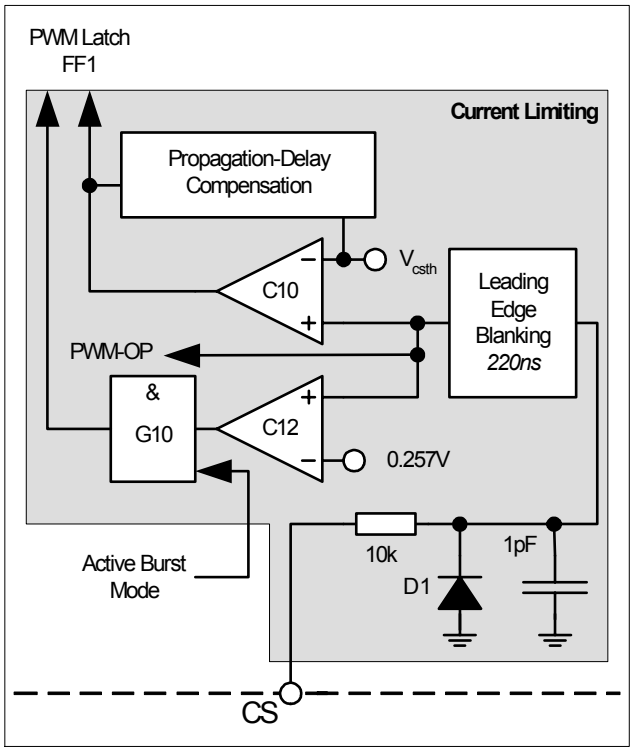


Figure 10 Current Limiting Block

There is a cycle by cycle Current Limiting realized by the Current-Limit comparator C10 to provide an overcurrent detection. The source current of the external Power Switch is sensed via an external sense resistor R_{Sense} . By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense} which is fed into the pin CS. If the voltage V_{Sense} exceeds the internal threshold voltage V_{csth} the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1. A Propagation Delay Compensation is added to support the immediate shut down without delay of the Power Switch in case of Current Limiting. The influence of the AC input voltage on the maximum output power can thereby be avoided.

To prevent the Current Limiting from distortions caused by leading edge spikes a Leading Edge Blanking is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the Gate G10 if Active Burst Mode is entered. Once activated the current limiting is thereby reduced to 0.257V. This voltage level determines the power level when the Active Burst Mode is left if there is a higher power demand.

3.5.1 Leading Edge Blanking

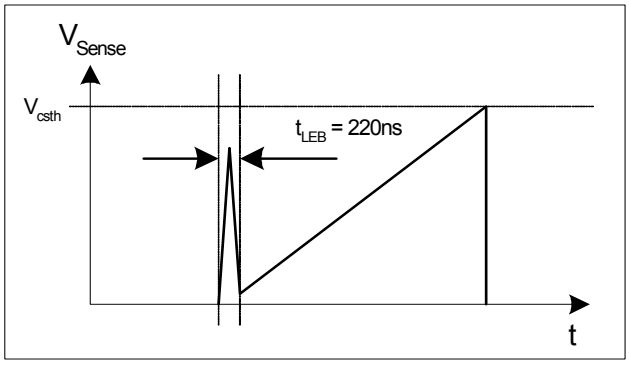


Figure 11 Leading Edge Blanking

Each time when the external Power Switch is switched on, a leading edge spike is generated due to the primary-side capacitances and secondary-side rectifier reverse recovery time. This spike can cause the gate drive to switch off unintentionally. To avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of t_{LEB} = 220ns. During this time, the gate drive will not be switched off.

3.5.2 Propagation Delay Compensation

In case of overcurrent detection, the switch-off of the external Power Switch is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current I_{peak} which depends on the ratio of dI/dt of the peak current (see Figure 12).

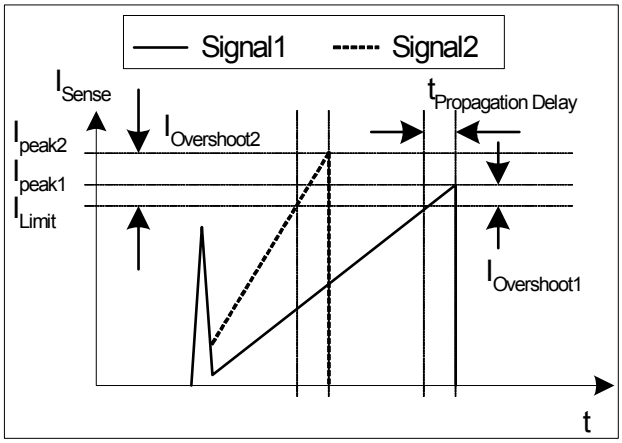


Figure 12 Current Limiting

The overshoot of Signal2 is bigger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to limit the overshoot dependency on dI/dt of the rising primary current. That means the propagation delay time between exceeding the current sense threshold V_{csth} and the switch off of the external Power Switch is compensated over temperature within a wide range.

Current Limiting is now possible in a very accurate way.

E.g. I_{peak} = 0.5A with R_{Sense} = 2. Without Propagation Delay Compensation the current sense threshold is set to a static voltage level V_{csth}=1V. A current ramp of dI/dt = 0.4A/µs, that means dV_{Sense}/dt = 0.8V/µs, and a propagation delay time of i.e. $t_{Propagation\ Delay}$ =180ns leads then to an I_{peak} overshoot of 14.4%. By means of propagation delay compensation the overshoot is only about 2% (see Figure 13).

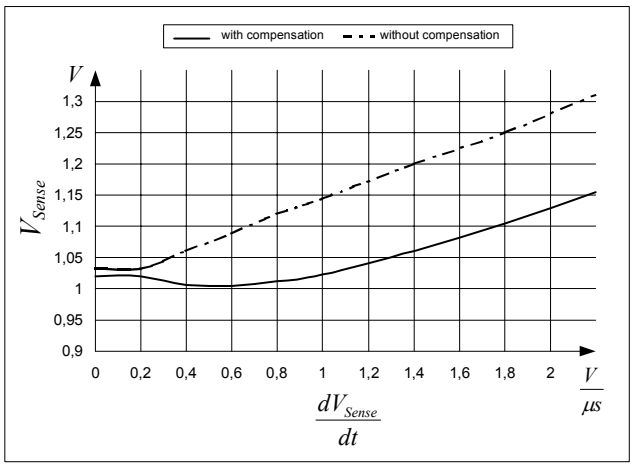


Figure 13 Overcurrent Shutdown

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage V_{csth} (see Figure 14). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

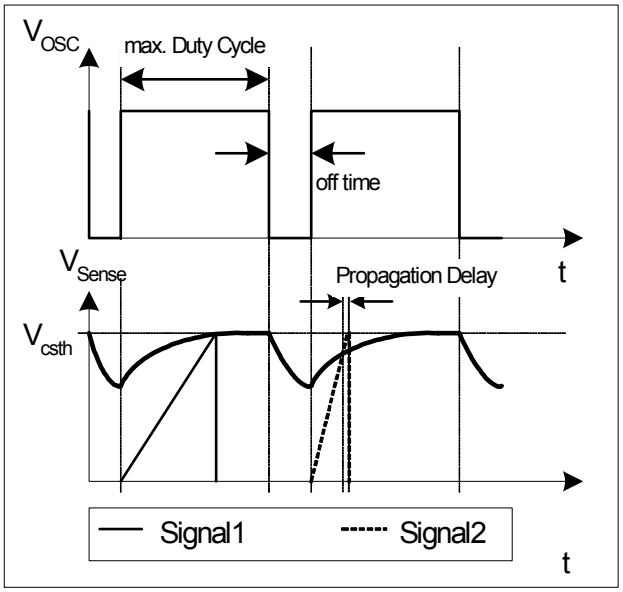


Figure 14 Dynamic Voltage Threshold V_{csth}

3.6 Control Unit

The Control Unit contains the functions for Active Burst Mode and Auto Restart Mode. The Active Burst Mode and the Auto Restart Mode are combined with an Adjustable Blanking Window which is depending on the external Soft Start capacitor. By means of this Adjustable Blanking Window, the IC avoids entering into these two modes accidentally. Furthermore it also provides a certain time whereby the overload detection is delayed. This delay is useful for applications which normally works with a low current and occasionally require a short duration of high current.

3.6.1 Adjustable Blanking Window

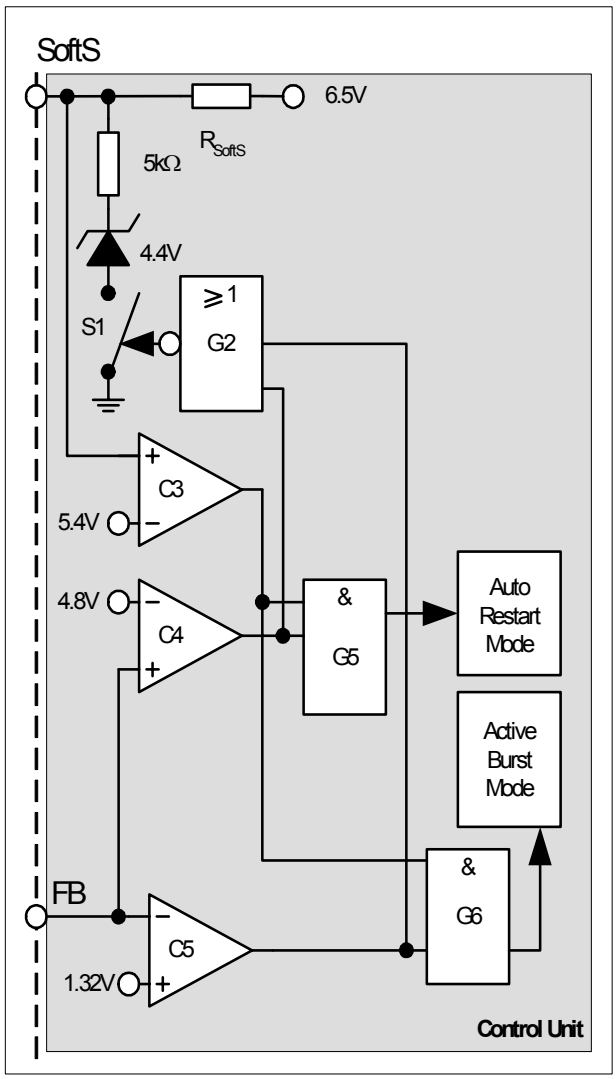


Figure 15 Adjustable Blanking Window

V_{SoftS} is clamped at 4.4V by the closed switch S1 after the SMPS is settled. If overload occurs V_{FB} is exceeding 4.8V. Auto Restart Mode can't be entered as the gate G5 is still blocked by the comparator C3. But after V_{FB} has exceeded 4.8V the switch S1 is opened via the gate G2. The external Soft Start capacitor can now be charged further by the

integrated pull up resistor R_{SoftS}. The comparator C3 releases the gates G5 and G6 once V_{Softs} has exceeded 5.4V. Therefore there is no entering of Auto Restart Mode possible during this charging time of the external capacitor C_{Softs}. The same procedure happens to the external Soft Start capacitor if a low load condition is detected by comparator C5 when V_{FB} is falling below 1.32V. Only after V_{SoftS} has exceeded 5.4V and V_{FB} is still below 1.32V Active Burst Mode is entered.

3.6.2 Active Burst Mode

The controller provides Active Burst Mode for low load conditions at V_{OUT}. Active Burst Mode increases significantly the efficiency at light load conditions while supporting a low ripple on V_{OUT} and fast response on load jumps. During Active Burst Mode which is controlled only by the FB signal the IC is always active and can therefore immediately response on fast changes at the FB signal. The Startup Cell is kept switched off to avoid increased power losses for the self supply.

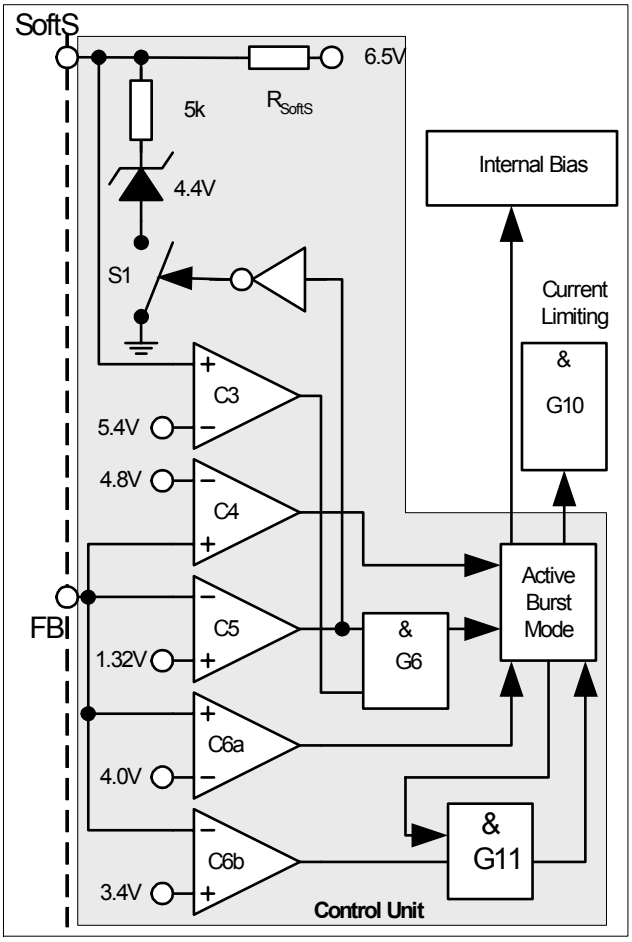


Figure 16 Active Burst Mode

The Active Burst Mode is located in the Control Unit. Figure 16 shows the related components.

3.6.2.1 Entering Active Burst Mode

The FB signal is always observed by the comparator C5 if the voltage level falls below 1.32V. In that case the switch S1 is released which allows the capacitor C_{SoftS} to be charged starting from the clamped voltage level at 4.4V in normal operating mode. If V_{SoftS} exceeds 5.4V the comparator C3 releases the gate G6 to enter the Active Burst Mode. The time window that is generated by combining the FB and SoftS signals with gate G6 avoids a sudden entering of the Active Burst Mode due to large load jumps. This time window can be adjusted by the external capacitor C_{SoftS}.

After entering Active Burst Mode a burst flag is set and the internal bias is switched off in order to reduce the current consumption of the IC down to approx. 1.05mA. In this Off State Phase the IC is no longer self supplied so that therefore C_{VCC} has to provide the VCC current (see Figure 17). Furthermore gate G11 is then released to start the next burst cycle once V_{FB} has 3.4V exceeded.

It has to be ensured by the application that the VCC remains above the Undervoltage Lockout Level of 8.5V to avoid that the Startup Cell is accidentally switched on. Otherwise power losses are significantly increased. The minimum VCC level during Active Burst Mode is depending on the load conditions and the application. The lowest VCC level is reached at no load conditions at V_{OUT}.

3.6.2.2 Working in Active Burst Mode

After entering the Active Burst Mode the FB voltage rises as V_{OUT} starts to decrease due to the inactive PWM section. Comparator C6a observes the FB signal if the voltage level 4V is exceeded. In that case the internal circuit is again activated by the internal Bias to start with switching. As now in Active Burst Mode the gate G10 is released the current limit is only 0.257V to reduce the conduction losses and to avoid audible noise. If the load at V_{OUT} is still below the starting level for the Active Burst Mode the FB signal decreases down to 3.4V. At this level C6b deactivates again the internal circuit by switching off the internal Bias. The gate G11 is released as after entering Active Burst Mode the burst flag is set. If working in Active Burst Mode the FB voltage is changing like a saw tooth between 3.4V and 4V (see Figure 17).

3.6.2.3 Leaving Active Burst Mode

The FB voltage immediately increases if there is a high load jump. This is observed by comparator C4. As the current limit is ca. 26% during Active Burst Mode a certain load jump is needed that FB can exceed 4.8V. At this time C4 resets the Active Burst Mode which also blocks C12 by the

gate G10. Maximum current can now be provided to stabilize V_{OUT}.

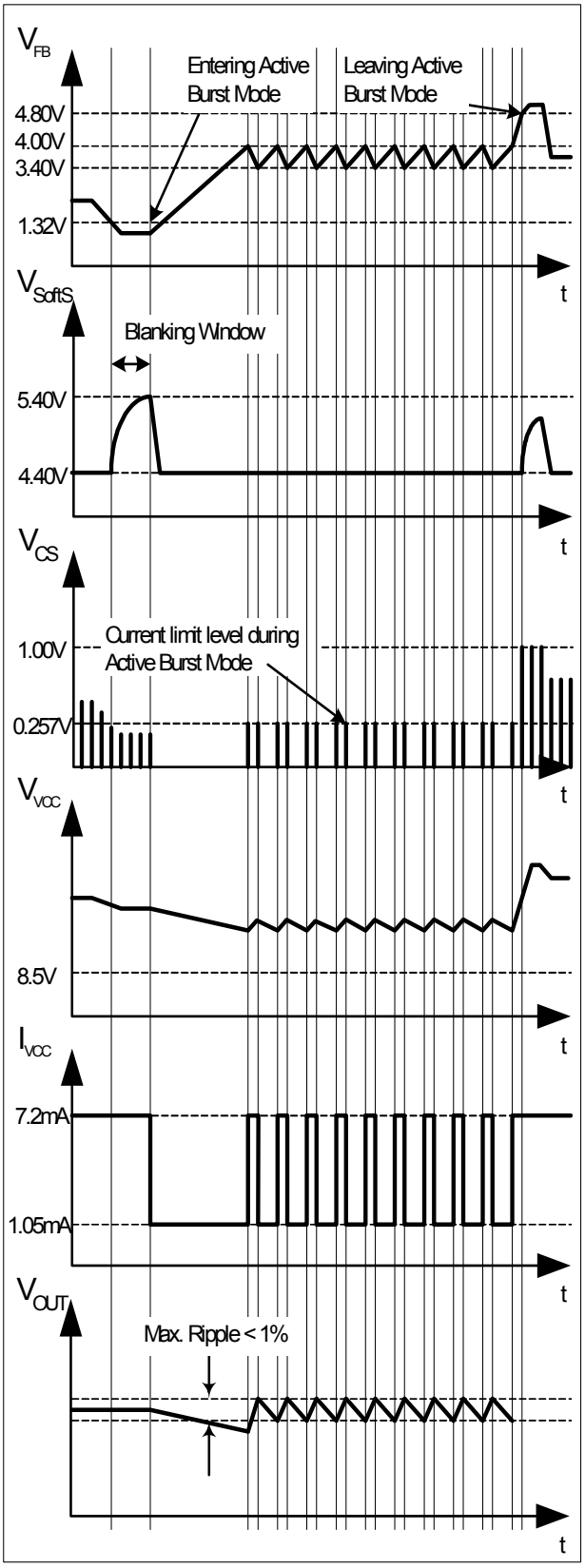


Figure 17 Signals in Active Burst Mode

3.6.3 Protection Mode (Auto Restart Mode)

In order to increase the SMPS system's robustness and safety, the IC provides the Auto Restart Mode as a protection feature. The Auto Restart Mode is entered upon detection of the following faults in the system:

- VCC Overvoltage
- Overtemperature
- Overload
- Open Loop
- VCC Undervoltage
- Short Optocoupler

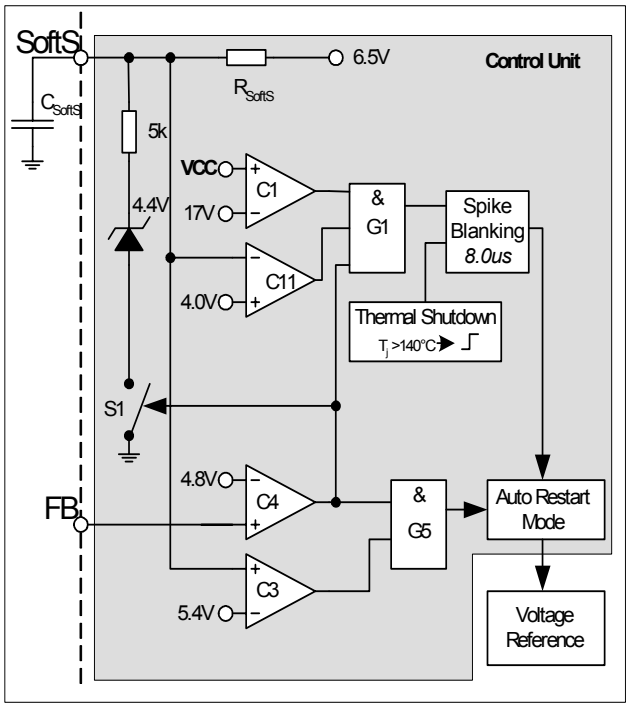


Figure 18 Auto Restart Mode

The VCC voltage is observed by comparator C1 if 17V is exceeded. The output of C1 is combined with both the output of C11 which checks for SoftS<4.0V, and the output of C4 which checks for FB>4.8V. Therefore the overvoltage detection is can only active during Soft Start Phase(SoftS<4.0V) and when FB signal is outside the operating range > 4.8V. This means any small voltage overshoots of V_{VCC} during normal operating cannot trigger the Auto Restart Mode.

In order to ensure system reliability and prevent any false activation, a blanking time is implemented before the IC can enter into the Auto Restart Mode. The output of the VCC overvoltage detection is fed into a spike blanking with a time constant of 8.0µs.

The other fault detection which can result in the Auto Restart Mode and has this 8.0µs blanking time is the Overtemperature detection. This block checks for a junction temperature of higher than 140°C for malfunction operation.

Once the Auto Restart Mode is entered, the internal Voltage Reference is switched off in order to reduce the current consumption of the IC as much as possible. In this mode, the average current consumption is only 300µA as the only working block is the Undervoltage Lockout(UVLO) which controls the Startup Cell by switching on/off at V_{VCCon}/ V_{VCCoff}.

As there is no longer a self supply by the auxiliary winding, VCC starts to drop. The UVLO switches on the integrated Startup Cell when VCC falls below 8.5V. It will continue to charge VCC up to 15V whereby it is switched off again and the IC enters into the Start Up Phase.

As long as all fault conditions have been removed, the IC will automatically power up as usual with switching cycle at the GATE output after Soft Start duration. Thus the name Auto Restart Mode.

Other fault detections which are active in normal operation is the sensing for Overload, Open Loop and VCC undervoltage conditions. In the first 2 cases, FB will rise above 4.8V which will be observed by C4. At this time, S1 is released such that V_{SoftS} can rise from its earlier clamp voltage of 4.4V. If V_{SoftS} exceeds 5.4V which is observed by C3, Auto Restart Mode is entered as both inputs of the gate G5 are high.

This charging of the Soft Start capacitor from 4.4V to 5.4V defines a blanking window which prevents the system from entering into Auto Restart Mode un-intentionally during large load jumps. In this event, FB will rise close to 6.5V for a short duration before the loop regulates with FB less than 4.8V. This is the same blanking time window as for the Active Burst Mode and can therefore be adjusted by the external C_{SoftS}.

In the case of VCC undervoltage, ie. VCC falls below 8.5V, the IC will be turn off with the Startup Cell charging VCC as described earlier in this section. Once VCC is charged above 15V, the IC will start a new startup cycle. The same procedure applies when the system is under Short Optocoupler fault condition, as it will lead to VCC undervoltage.

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HV Voltage	V_{HV}	-	500V	V	
VCC Supply Voltage	V_{VCC}	-0.3	22	V	
FB Voltage	V_{FB}	-0.3	6.5	V	
SoftS Voltage	V_{SoftS}	-0.3	6.5	V	
Gate Voltage	V_{Gate}	-0.3	22	V	Internally clamped at 11.5V
CS Voltage	V_{CS}	-0.3	6.5	V	
Junction Temperature	T_j	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Total Power Dissipation	$P_{totDSO8}$	-	0.45	W	PG-DSO-8, T_{amb} < 50°C
	$P_{totDIP8}$	-	0.90	W	PG-DIP-8, T_{amb} < 50°C
Thermal Resistance Junction-Ambient	$R_{thJADSO8}$	-	185	K/W	PG-DSO-8
	$R_{thJADIP8}$	-	90	K/W	PG-DIP-8
ESD Capability(incl. HV Pin)	V_{ESD}	-	3	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	21	V	
Junction Temperature of Controller	T_{jCon}	-25	130	°C	Max value limited due to thermal shut down of controller

4.3 Characteristics

4.3.1 Supply Section 1

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 25 °C to 130 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 15 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Up Current	$I_{VCCstart}$	-	160	220	µA	V_{VCC} =14V
VCC Charge Current	$I_{VCCcharge1}$	0.55	1.05	1.60	mA	V_{VCC} = 0V
	$I_{VCCcharge2}$	-	0.88	-	mA	V_{VCC} =14V
Leakage Current of Start Up Cell	$I_{StartLeak}$	-	0.2	20	µA	V_{VCC} =16V, V_{HV} = 450V
Supply Current with Inactive Gate	$I_{VCCsup1}$	-	5.5	7.0	mA	
Supply Current in Auto Restart Mode with Inactive Gate	$I_{VCCrestart}$	-	300	-	µA	I_{FB} = 0 I_{Softs} = 0
Supply Current in Active Burst Mode with Inactive Gate	$I_{VCCburst1}$	-	1.05	1.25	mA	V_{VCC} =15V V_{FB} = 3.7V, V_{SoftS} = 4.4V
	$I_{VCCburst2}$	-	0.95	1.15	mA	V_{VCC} = 9.5V V_{FB} = 3.7V, V_{SoftS} = 4.4V
VCC Turn-On Threshold VCC Turn-Off Threshold VCC Turn-On/Off Hysteresis	V_{VCCon} V_{VCCoff} V_{VCChys}	14.2 8.0 -	15.0 8.5 6.5	15.8 9.0 -	V V V	

4.3.2 Supply Section 2

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Supply Current with Active Gate	ICE3AS02 ICE3AS02G	$I_{VCCsup2}$	-	7.0	8.5	mA	V_{SoftS} = 4.4V I_{FB} = 0, C_{Load}=1nF
	ICE3BS02 ICE3BS02G	$I_{VCCsup3}$	-	6.5	8.0	mA	

4.3.3 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	V_{REF}	6.37	6.50	6.63	V	measured at pin FB I_{FB} = 0

4.3.4 PWM Section

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Fixed Oscillator Frequency	ICE3AS02 ICE3AS02G	f_{OSC1}	92	100	108	kHz	
		f_{OSC2}	94	100	106	kHz	T_j = 25°C
	ICE3BS02 ICE3BS02G	f_{OSC3}	61	67	73	kHz	
		f_{OSC4}	63	67	71	kHz	T_j = 25°C
Max. Duty Cycle		D_{max}	0.67	0.72	0.77		
Min. Duty Cycle		D_{min}	0	-	-		V_{FB} < 0.3V
PWM-OP Gain		A_V	3.5	3.7	3.9		
Voltage Ramp Max Level		$V_{Max-Ramp}$	-	0.85	-	V	
V_{FB} Operating Range Min Level		V_{FBmin}	0.3	0.7	-	V	
V_{FB} Operating Range Max level		V_{FBmax}	-	-	4.75	V	CS=1V, limited by Comparator C4[1)]
FB Pull-Up Resistor		R_{FB}	16	20	27	kΩ	
SoftS Pull-Up Resistor		R_{SoftS}	39	50	62	kΩ	

1) The parameter is not subjected to production test - verified by design/characterization

4.3.5 Control Unit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Deactivation Level for SoftS Comparator C7 by C2	$V_{SoftSC2}$	3.85	4.00	4.15	V	V_{FB} > 5V
Clamped V_{SoftS} Voltage during Normal Operating Mode	$V_{SoftSclmp}$	4.23	4.40	4.57	V	V_{FB} = 4V
Activation Limit of Comparator C3	$V_{SoftSC3}$	5.20	5.40	5.60	V	V_{FB} > 5V
SoftS Startup Current	$I_{SoftSstart}$	-	1.3	-	mA	V_{SoftS} = 0V
Over Load & Open Loop Detection Limit for Comparator C4	V_{FBC4}	4.62	4.80	4.98	V	V_{SoftS} > 5.6V
Active Burst Mode Level for Comparator C5	V_{FBC5}	1.23	1.30	1.37	V	V_{SoftS} > 5.6V
Active Burst Mode Level for Comparator C6a	V_{FBC6a}	3.85	4.00	4.15	V	After Active Burst Mode is entered

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Active Burst Mode Level for Comparator C6b	V_{FBC6b}	3.25	3.40	3.55	V	After Active Burst Mode is entered
Overvoltage Detection Limit	V_{VCCOVP}	16.1	17.1	18.1	V	V_{FB} > 5V V_{SoftS} < 4.0V
Thermal Shutdown[1)]	T_{jSD}	130	140	150	°C	
Spike Blanking	t_{Spike}	-	8.0	-	µs	

1) The parameter is not subjected to production test - verified by design/characterization

Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except V_{VCCOVP} *and* V_{VCCPD}

4.3.6 Current Limiting

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay Time of external MOS)	V_{csth}	0.97	1.02	1.07	V	dV_{sense} / dt = 0.6V/µs (see Figure 14)
Peak Current Limitation during Active Burst Mode	V_{CS2}	0.232	0.257	0.282	V	
Leading Edge Blanking	t_{LEB}	-	220	-	ns	V_{SoftS} = 4.4V
CS Input Bias Current	I_{CSbias}	-1.0	-0.2	0	µA	V_{CS} =0V

4.3.7 Driver Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE Low Voltage	$V_{GATElow}$	-	-	1.2	V	V_{VCC} = 5 V I_{Gate} = 5 mA
		-	-	1.5	V	V_{VCC} = 5 V I_{Gate} = 20 mA
		-	0.8	-	V	I_{Gate} = 0 A
		-	1.6	2.0	V	I_{Gate} = 20 mA
		-0.2	0.2	-	V	I_{Gate} = -20 mA
GATE High Voltage	$V_{GATEhigh}$	-	11.5	-	V	V_{VCC} = 20V C_L = 4.7nF
		-	10.5	-	V	V_{VCC} = 11V C_L = 4.7nF
		-	7.5	-	V	V_{VCC} = V_{VCCoff} + 0.2V C_L = 4.7nF
GATE Rise Time (incl. Gate Rising Slope)	t_{rise}	-	150	-	ns	V_{Gate} = 2V ...9V[1)] C_L = 4.7nF
GATE Fall Time	t_{fall}	-	55	-	ns	V_{Gate} = 9V ...2V[1)] C_L = 4.7nF
GATE Current, Peak, Rising Edge	I_{GATE}	-0.5	-	-	A	C_L = 4.7nF[2)]
GATE Current, Peak, Falling Edge	I_{GATE}	-	-	0.7	A	C_L = 4.7nF[2)]

1) Transient reference value

2) The parameter is not subjected to production test - verified by design/characterization

5 Outline Dimension

PG-DIP-8
(Pb-free Plating
Plastic Dual In-Line Outline)

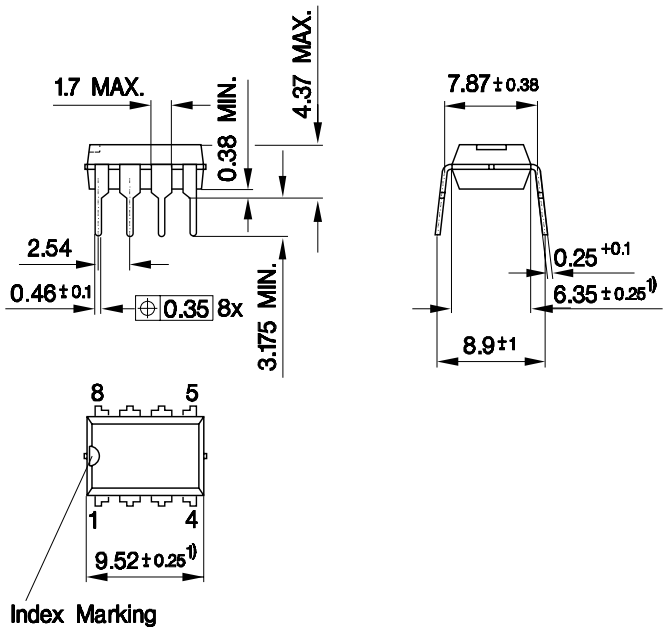


Figure 19 PG-DIP-8 (Pb-free Plating Plastic Dual In-Line Outline)

PG-DSO-8
(Pb-free Plating
Plastic Dual Small Outline)

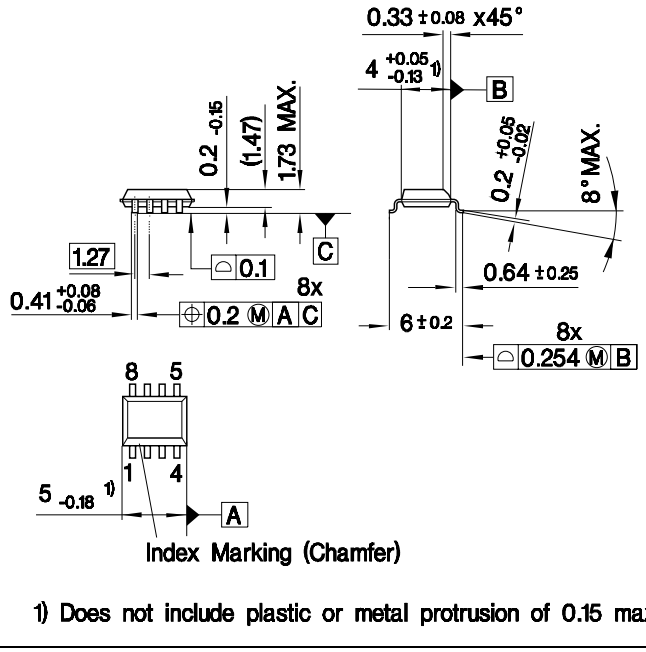


Figure 20 GP-DSO-8 (Pb-free Plating Plastic Dual Small Outline)

Dimensions in mm

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an allencompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

http://www.infineon.com

Published by Infineon Technologies AG