Precision, Selectable Gain, Fully Differential Funnel Amplifier

Data Sheet **AD8475**

FEATURES

- Precision attenuation: G = 0.4, G = 0.8
- Fully differential or single-ended input/output
- Differential output designed to drive precision ADCs
  - Drives switched capacitor and Σ-Δ ADCs
  - Rail-to-rail output
- VOCM pin adjusts output common-mode voltage
- Robust overvoltage protection up to ±15 V (V_S = +5 V)
- Single supply: 3 V to 10 V
- Dual supplies: ±1.5 V to ±5 V
- High performance
  - Suited for driving 18-bit converters up to 4 MSPS
  - 10 nV/√Hz output noise
  - 3 ppm/°C gain drift
  - 500 µV maximum output offset
  - 50 V/µs slew rate
- Low power: 3.2 mA supply current

APPLICATIONS

- ADC drivers
- Differential instrumentation amplifier building blocks
- Single-ended-to-differential converters

GENERAL DESCRIPTION

The AD8475 is a fully differential, attenuating amplifier with integrated precision gain resistors. It provides precision attenuation (by 0.4 or 0.8), common-mode level shifting, and single-ended-to-differential conversion along with input overvoltage protection. Power dissipation on a single 5 V supply is only 16 mW.

The AD8475 is a simple to use, fully integrated precision gain block, designed to process signal levels of up to ±10 V on a single supply. It provides a complete interface to make industrial level signals directly compatible with the differential input ranges of low voltage high performance 16-bit or 18-bit single-supply successive approximation (SAR) analog-to-digital converters (ADCs).

The AD8475 comes with two standard pin-selectable gain options: 0.4 and 0.8. The gain of the part is set by driving the input pin corresponding to the appropriate gain.

The AD8475 also provides overvoltage protection from large industrial input voltages up to ±15 V while operating on a single 5 V supply. The VOCM pin adjusts the output voltage common mode for precision level shifting, to match the ADC's input range and maximize dynamic range.

FUNCTIONAL BLOCK DIAGRAMS

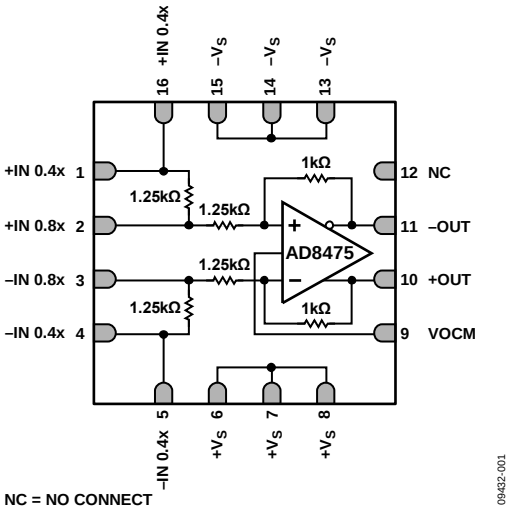

Figure 1. 16-Lead LFCSP

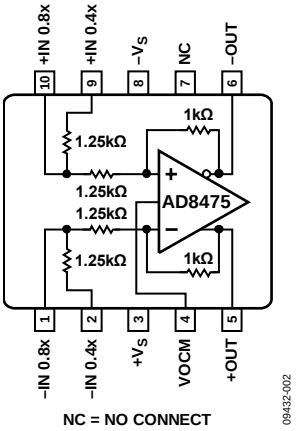

Figure 2. 10-Lead MSOP

The AD8475 works extremely well with SAR, Σ-Δ, and pipeline converters. The high current output stage of the part allows it to drive the switched capacitor front-end circuits of many ADCs with minimal error.

Unlike many differential drivers in the market, the AD8475 is a high precision amplifier. With 500 µV maximum output offset, 10 nV/√Hz output noise, and −112 dB THD + N, the AD8475 pairs well with high accuracy converters. Considering its low power consumption and high precision, the slew-enhanced AD8475 has excellent speed, settling to 18-bit precision for 4 MSPS acquisition.

The AD8475 is available in a space-saving 16-lead 3 mm × 3 mm LFCSP package and a 10-lead MSOP package. It is fully specified over the −40°C to +85°C temperature range.

Rev. C Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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10/10—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, G = 0.4, VOCM connected to 2.5 V, R_L = 1 kΩ differentially, T_A = 25°C, referred to output (RTO), unless otherwise noted.

Table 1.

		B Grade			A Grade			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Small Signal Bandwidth			150			150		MHz
−3 dB Large Signal Bandwidth			15			15		MHz
Slew Rate	2 V step		50			50		V/µs
Settling Time to 0.01%	2 V step on output		45			45		ns
Settling Time to 0.001%	2 V step on output		50			50		ns
NOISE/DISTORTION[1]								
THD + N	f = 100 kHz, V_{OUT} = 4 V p-p, 22 kHz band-pass filter		−112			−112		dB
HD2	f = 1 MHz, V_{OUT} = 2 V p-p		−110			−110		dB
HD3	f = 1 MHz, V_{OUT} = 2 V p-p		−96			−96		dB
IMD3	f_1 = 0.95 MHz, f_2 = 1.05 MHz, V_{OUT} = 2 V p-p		−90			−90		dBc
IMD3	f_1 = 95 kHz, f_2 = 105 kHz, V_{OUT} = 2 V p-p		−84			−84		dBc
Output Voltage Noise	f = 0.1 Hz to 10 Hz		2.5			2.5		µV p-p
Spectral Noise Density	f = 1 kHz		10			10		nV/√Hz
GAIN			0.4			0.4		V/V
Gain Error	R_L = ∞			0.02			0.05	%
Gain Drift	−40°C ≤ T_A ≤ +85°C		1	3		1	3	ppm/°C
Gain Nonlinearity	V_{OUT} = 4 V p-p		2.5			2.5		ppm
OFFSET AND CMRR								
Offset[2]	RTO		50	200		50	500	µV
vs. Temperature	−40°C ≤ T_A ≤ +85°C		2.5			2.5		µV/°C
vs. Power Supply	V_S = ±2.5 V to ±5 V	90			90			dB
Common-Mode Rejection Ratio	V_{INCm} = ±5 V	86			76			dB
INPUT CHARACTERISTICS								
Input Voltage Range[3]	Differential input	−6.25		+6.25	−6.25		+6.25	V
	Single-ended input	−12.5		+12.5	−12.5		+12.5	V
Impedance[4]	V_{INCm} = V_S/2							
Single-Ended Input			2.92			2.92		kΩ
Differential Input			5			5		kΩ
Common Mode Input			1.75			1.75		kΩ
OUTPUT CHARACTERISTICS								
Output Swing		$-V_S$ + 0.05		$+V_S$ − 0.05	$-V_S$ + 0.05		$+V_S$ − 0.05	
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$	−90			−80			dB
Output Impedance			0.1			0.1		Ω
Capacitive Load	Per output		30			30		pF
Short-Circuit Current Limit			110			110		mA
VOCM CHARACTERISTICS								
VOCM Input Voltage Range		$-V_S$ + 1		$+V_S$	$-V_S$ + 1		$+V_S$	V
VOCM Input Impedance			100			100		kΩ
VOCM Gain Error				0.02			0.02	%

		B Grade			A Grade			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
POWER SUPPLY								
Specified Voltage			5			5		V
Operating Voltage Range		3		10	3		10	V
Supply Current			3	3.2		3	3.2	mA
Over Temperature	$-40°C \le T_A \le +85°C$			4			4	mA
TEMPERATURE RANGE								
Specified Performance Range		−40		+85	−40		+85	°C
Operating Range		−40		+125	−40		+125	°C

[1] Includes amplifier voltage and current noise, as well as noise of internal resistors.
[2] Includes input bias and offset current errors.
[3] The input voltage range is a function of the voltage supplies and ESD diodes. See the Input Voltage Range section for more information.
[4] Internal resistors are trimmed to be ratio matched but have ±20% absolute accuracy.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	11 V
Maximum Voltage at Any Input Pin	$+V_S$ + 10.5 V
Minimum Voltage at Any Input Pin	$-V_S$ − 16 V
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +85°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature	150°C
ESD (FICDM)	1500 V
ESD (HBM)	2000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	84.90	°C/W
10-Lead MSOP	214.0	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

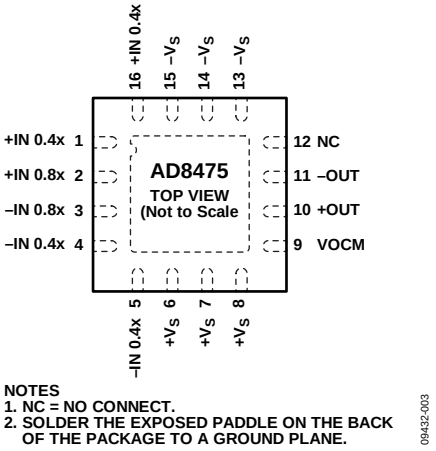


Figure 3. 16-Lead LFCSP Pin Configuration

Table 4. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	+IN 0.4x	Positive Input for 0.4 Attenuation.
2	+IN 0.8x	Positive Input for 0.8 Attenuation
3	−IN 0.8x	Negative Input for 0.8 Attenuation.
4	−IN 0.4x	Negative Input for 0.4 Attenuation.
5	−IN 0.4x	Negative Input for 0.4 Attenuation.
6	$+V_S$	Positive Supply.
7	$+V_S$	Positive Supply.
8	$+V_S$	Positive Supply.
9	VOCM	Output Common-Mode Adjust.
10	+OUT	Positive Output.
11	−OUT	Negative Output.
12	NC	No Connect.
13	$-V_S$	Negative Supply.
14	$-V_S$	Negative Supply.
15	$-V_S$	Negative Supply.
16	+IN 0.4x	Positive Input for 0.4 Attenuation.
	EPAD	Solder the exposed paddle on the back of the package to a ground plane.

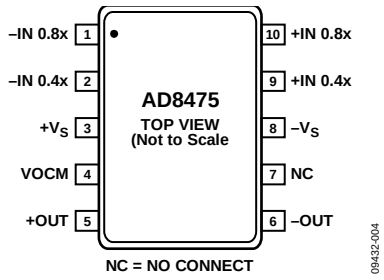


Figure 4. 10-Lead MSOP Pin Configuration

Table 5. 10-Lead MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN 0.8x	Negative Input for 0.8 Attenuation
2	−IN 0.4x	Negative Input for 0.4 Attenuation
3	$+V_S$	Positive Supply
4	VOCM	Output Common-Mode Adjust
5	+OUT	Noninverting Output
6	−OUT	Inverting Output
7	NC	No Connect
8	$-V_S$	Negative Supply
9	+IN 0.4x	Positive Input for 0.4 Attenuation
10	+IN 0.8x	Positive Input for 0.8 Attenuation

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, gain = 0.4, R_{LOAD} = 1 kΩ, RTO, unless otherwise specified.

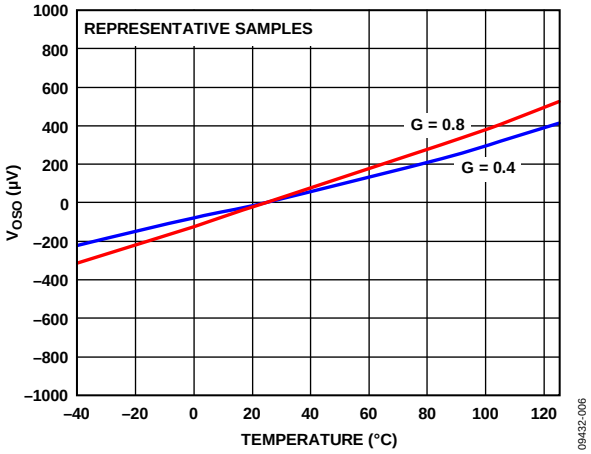


Figure 5. System Offset vs. Temperature

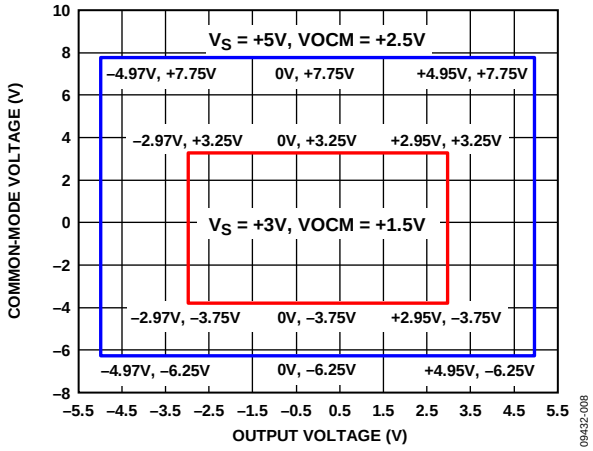


Figure 8. Input Common-Mode Voltage vs. Output Voltage, V_S = +5 V and +3 V

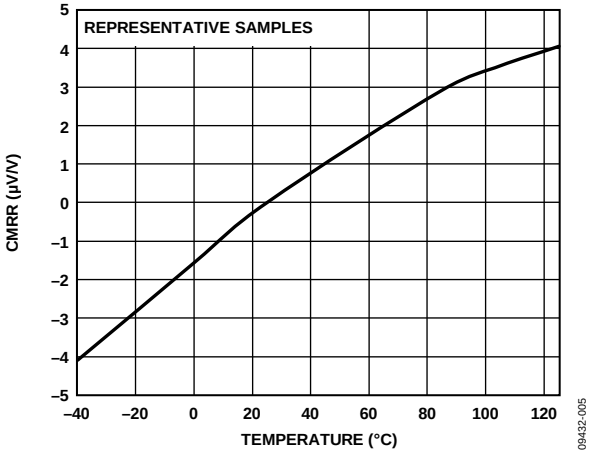


Figure 6. CMRR vs. Temperature (G = 0.8)

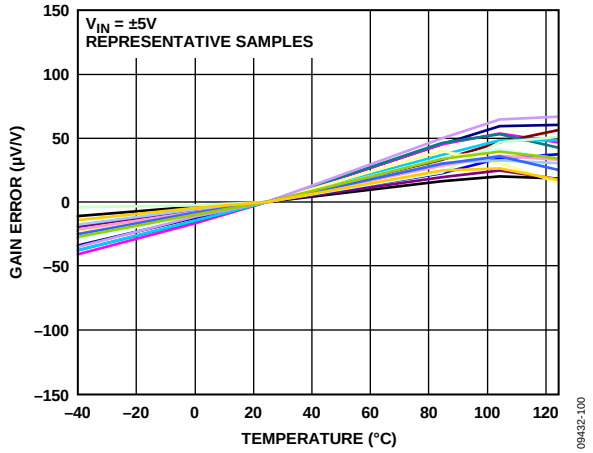


Figure 9. Gain Error vs. Temperature, V_S = ±5 V

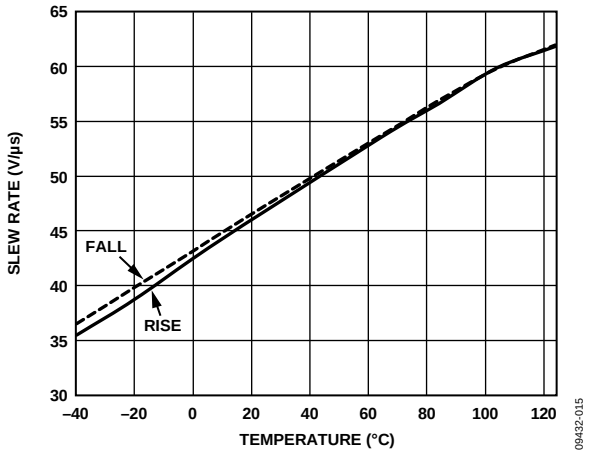


Figure 7. Slew Rate vs. Temperature

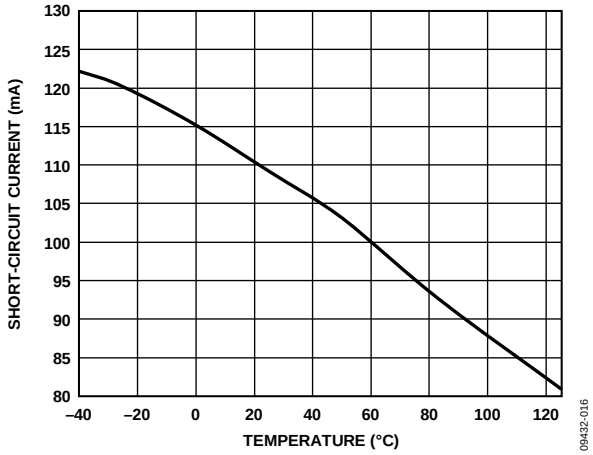


Figure 10. Short-Circuit Current vs. Temperature

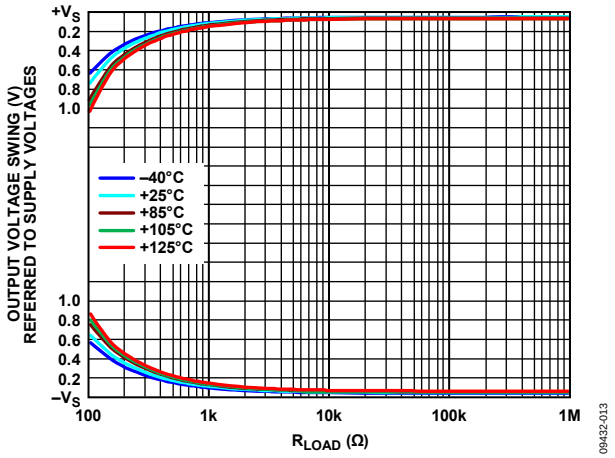


Figure 11. Output Voltage Swing vs. R_{LOAD} vs. Temperature, V_S = ±5 V and +5 V

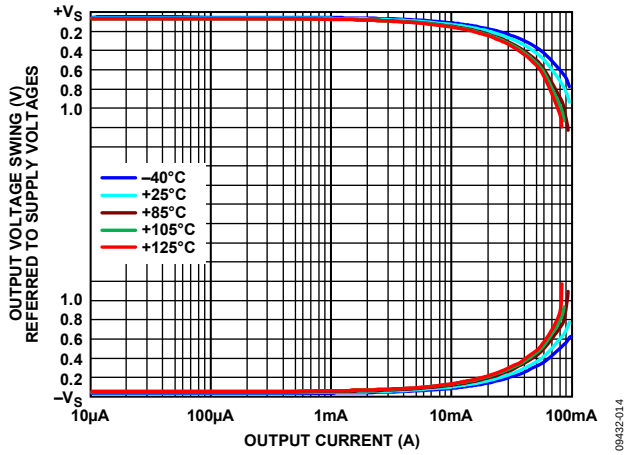


Figure 14. Output Voltage Swing vs. Output Current vs. Temperature, V_S = ±5 V and +5 V

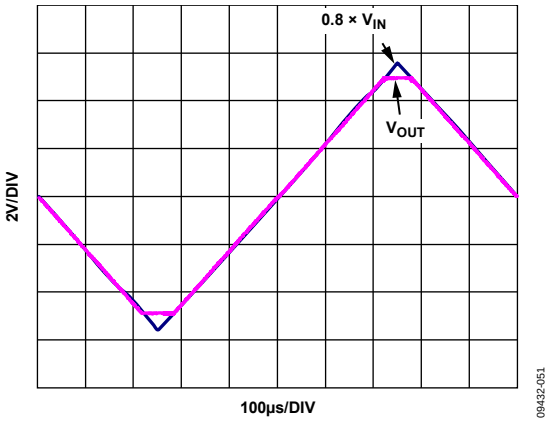


Figure 12. Overdrive Recovery

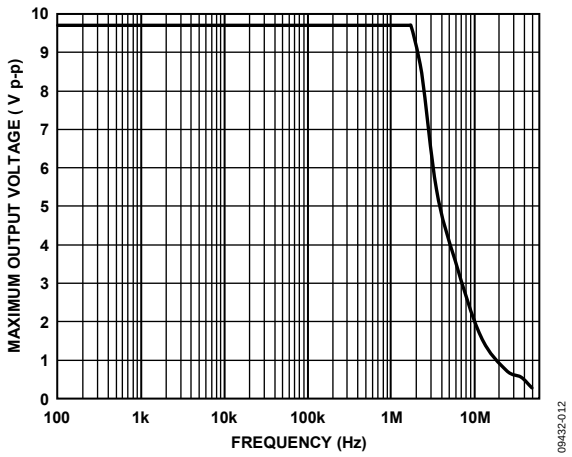


Figure 15. Maximum Output Voltage vs. Frequency

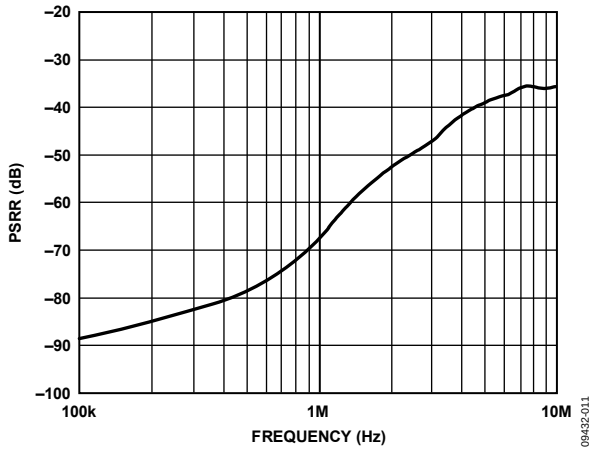


Figure 13. Power Supply Rejection Ratio (PSRR) vs. Frequency

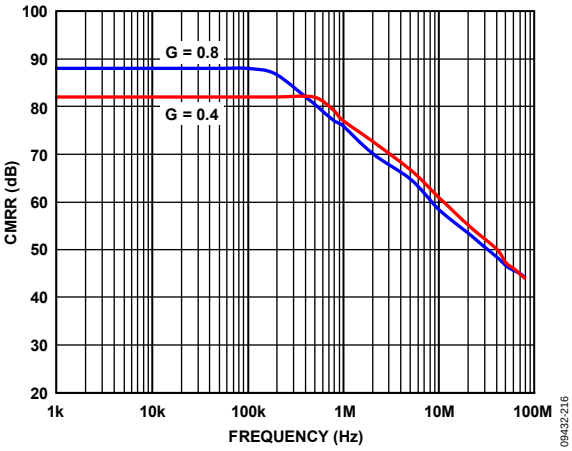


Figure 16. CMRR vs. Frequency

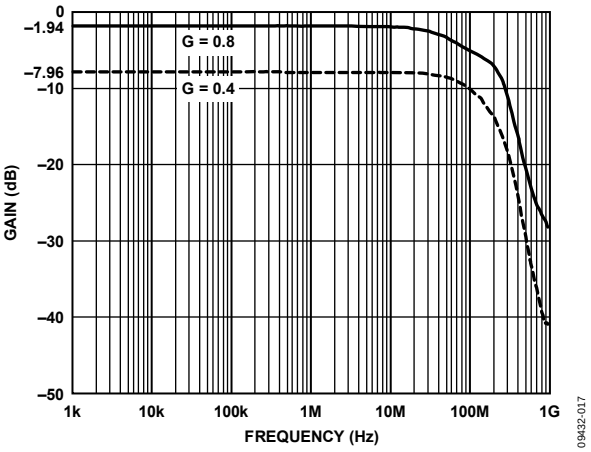


Figure 17. Small Signal Frequency Response for All Gains V_S = ±5 V

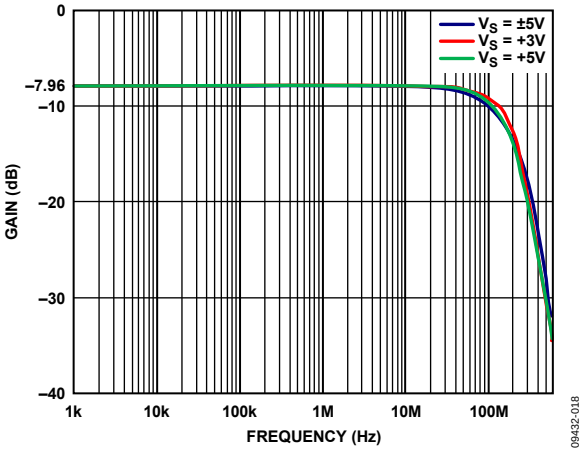


Figure 18. Small Signal Frequency Response for Various Supplies

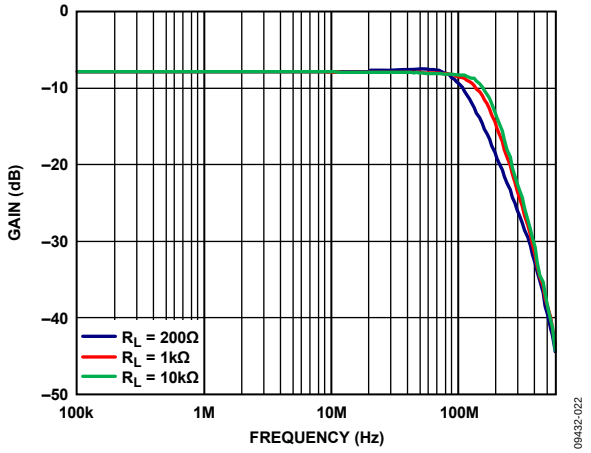


Figure 19. Small Signal Frequency Response for Various Loads

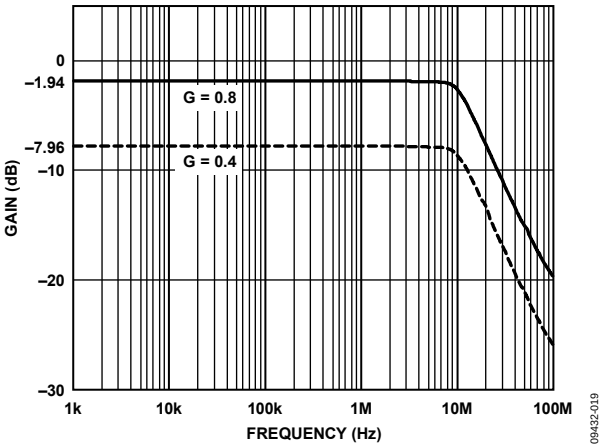


Figure 20. Large Signal Frequency Response for All Gains, V_S = ±5 V

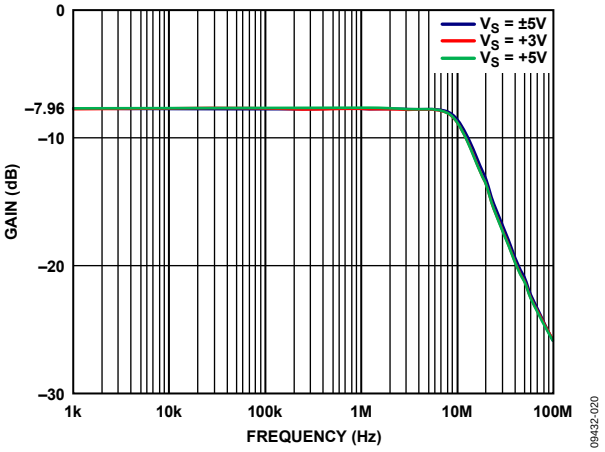


Figure 21. Large Signal Frequency Response for Various Supplies

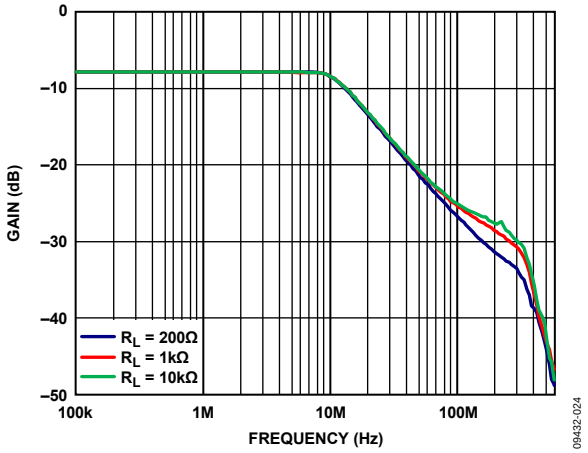


Figure 22. Large Signal Frequency Response for Various Loads

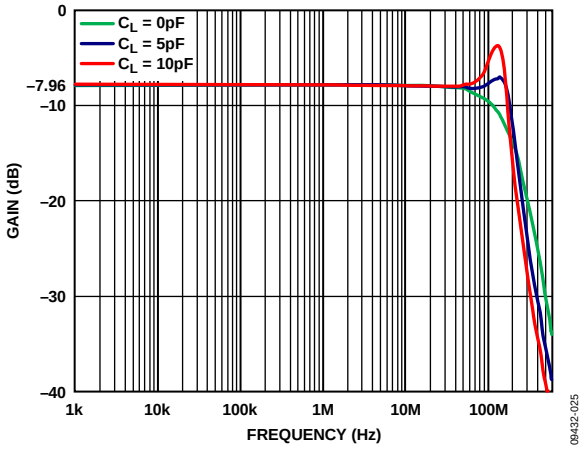


Figure 23. Small Signal Frequency Response for Various Capacitive Loads

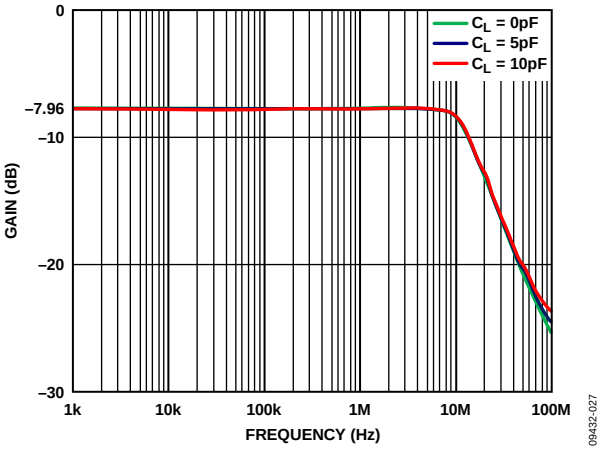


Figure 26. Large Signal Frequency Response for Various Capacitive Loads

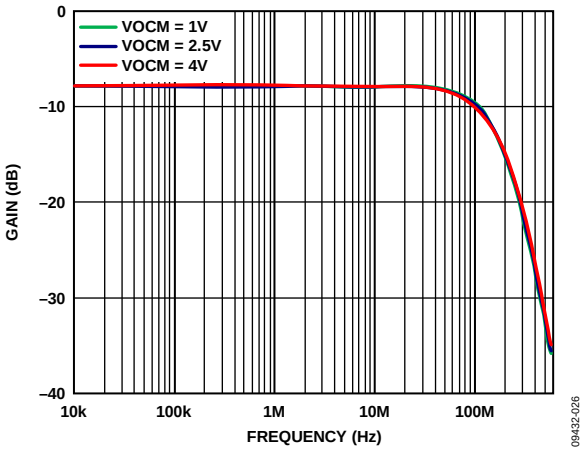


Figure 24. Small Signal Frequency Response for Various VOCM Levels

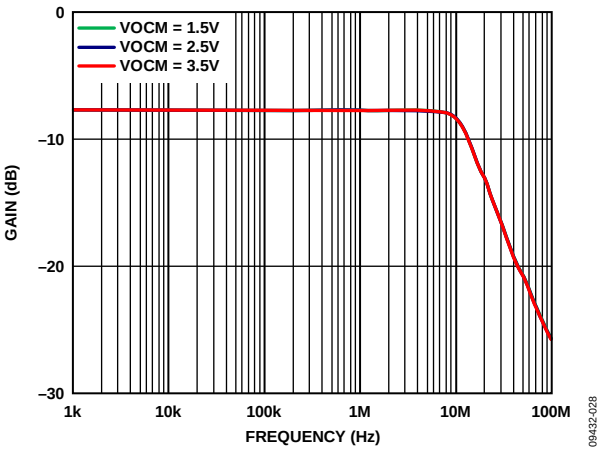


Figure 27. Large Signal Frequency Response for Various VOCM Levels

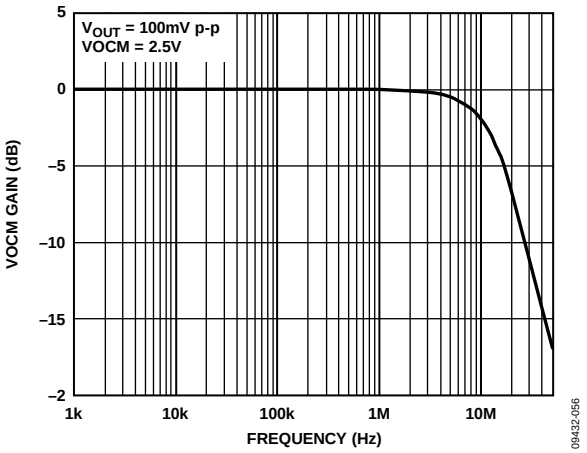


Figure 25. VOCM Small Signal Frequency Response

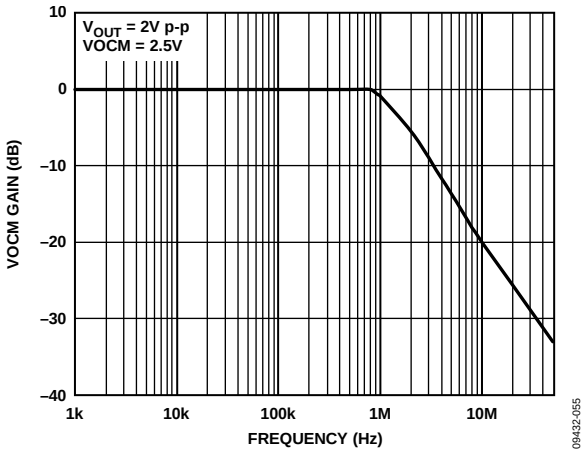


Figure 28. VOCM Large Signal Frequency Response

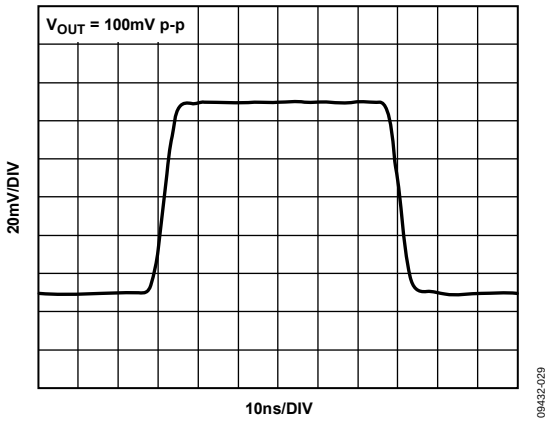


Figure 29. Small Signal Pulse Response, V_S = ±2.5 V

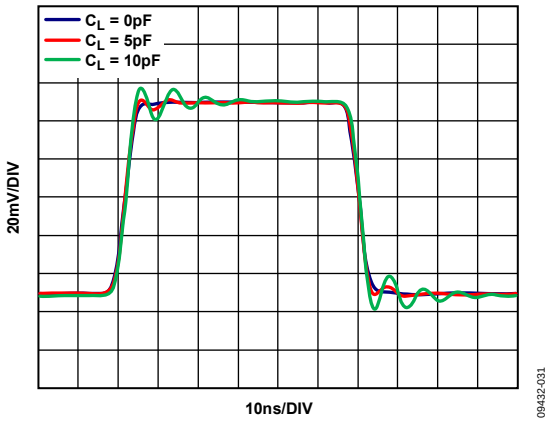


Figure 30. Small Signal Step Response for Various Capacitive Loads, V_S = ±2.5 V

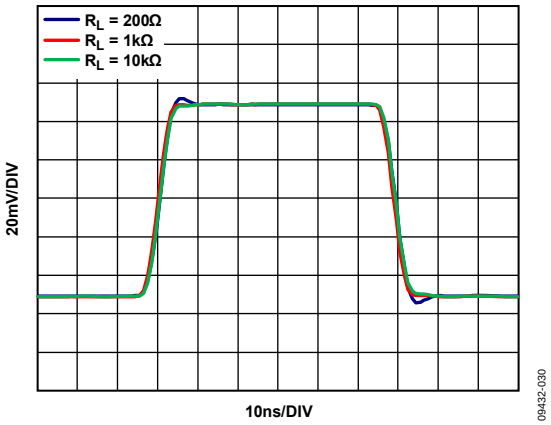


Figure 31. Small Signal Step Response for Various Resistive Loads

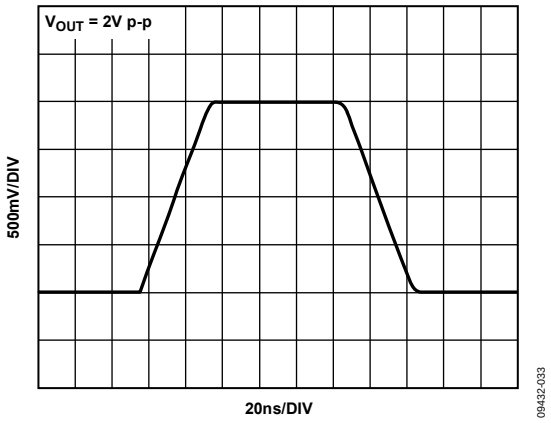


Figure 32. Large Signal Pulse Response, V_S = ±2.5 V

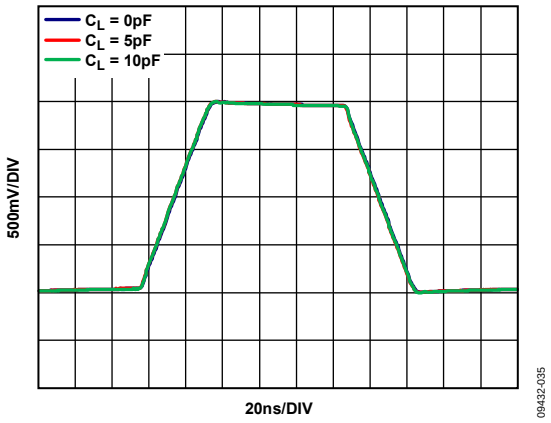


Figure 33. Large Signal Step Response for Various Capacitive Loads

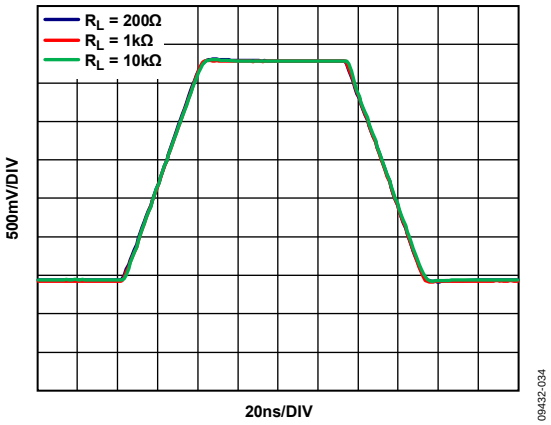


Figure 34. Large Signal Step Response for Various Resistive Loads

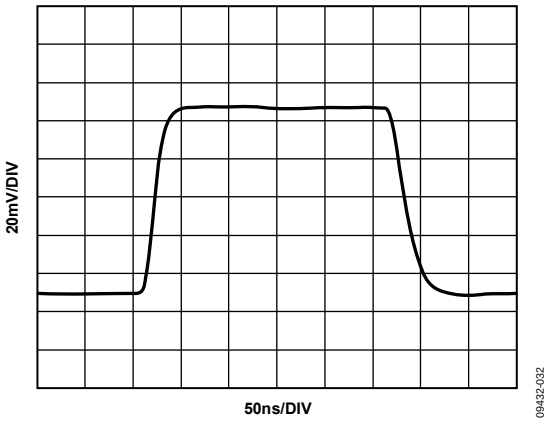


Figure 35. VOCM Small Signal Step Response, V_S = ±2.5 V

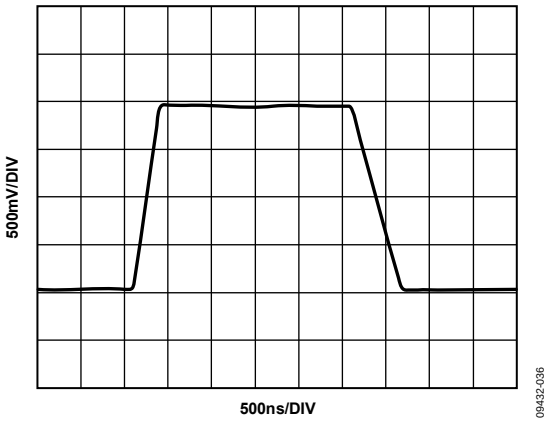


Figure 38. VOCM Large Signal Step Response

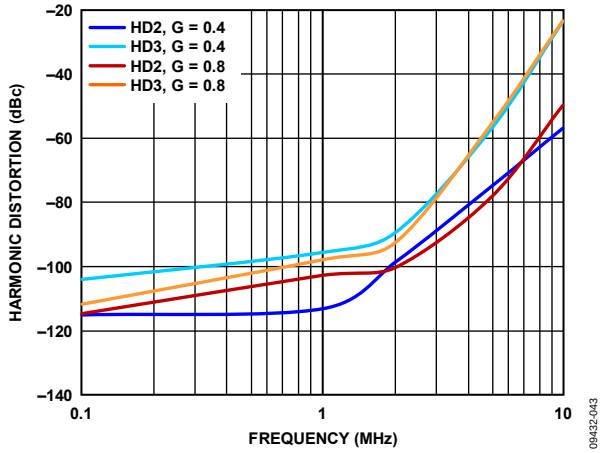


Figure 36. Harmonic Distortion vs. Frequency at Various Gains

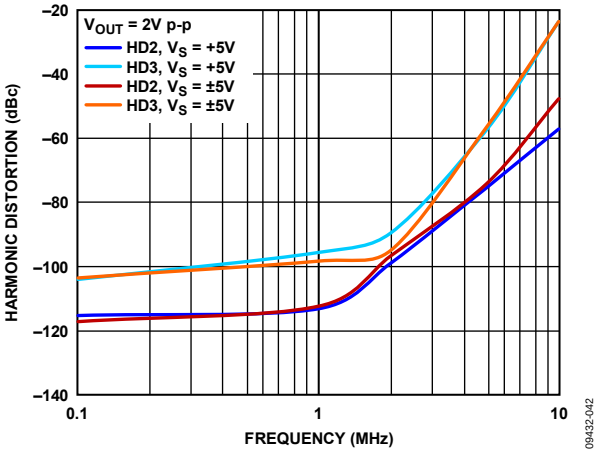


Figure 39. Harmonic Distortion vs. Frequency at Various Supplies

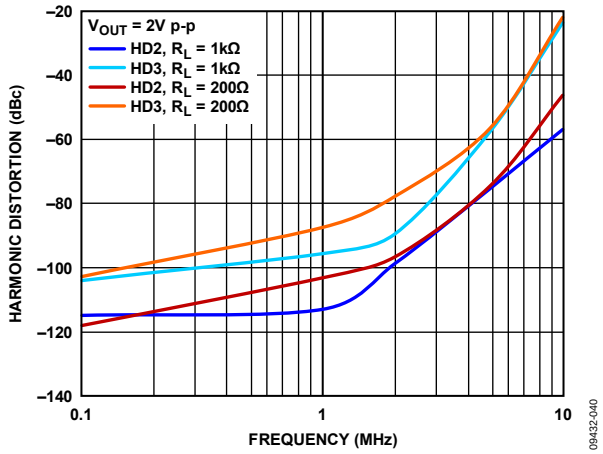


Figure 37. Harmonic Distortion vs. Frequency at Various Loads

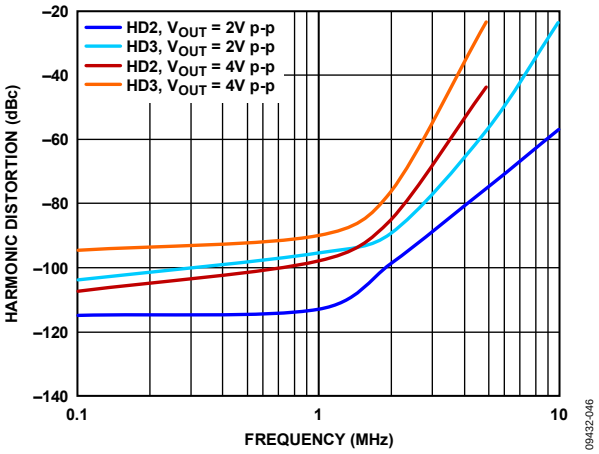


Figure 40. Harmonic Distortion vs. Frequency at Various $V_{OUT,dm}$

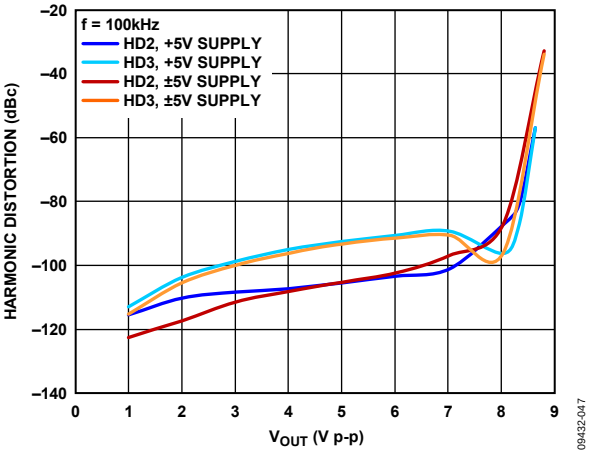


Figure 41. Harmonic Distortion vs. V_{OUT} at Various Supplies

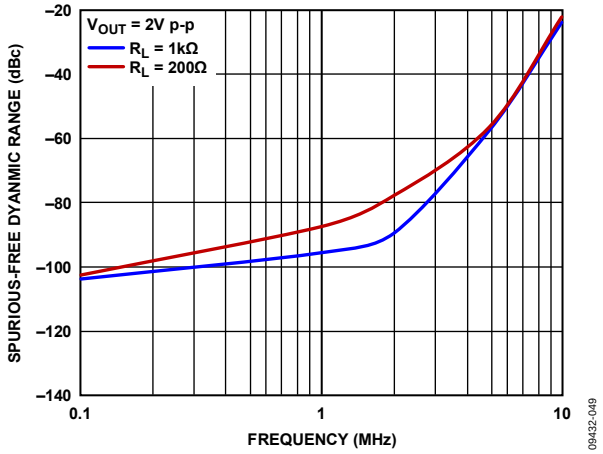


Figure 44. Spurious-Free Dynamic Range vs. Frequency at Various Loads

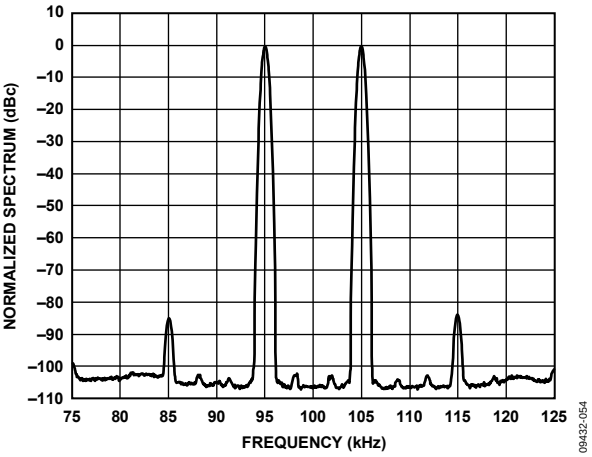


Figure 42. 100 kHz Intermodulation Distortion

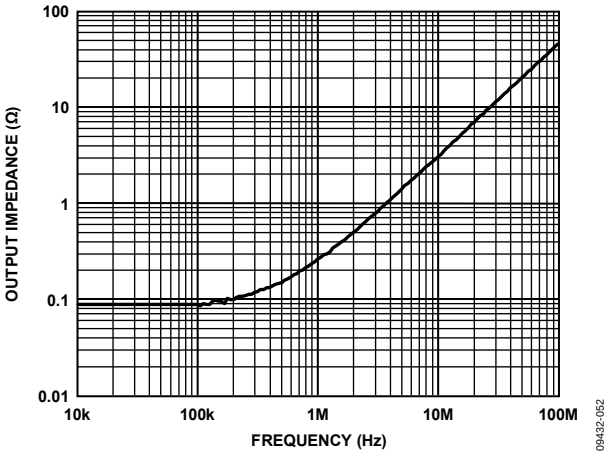


Figure 45. Output Impedance vs. Frequency

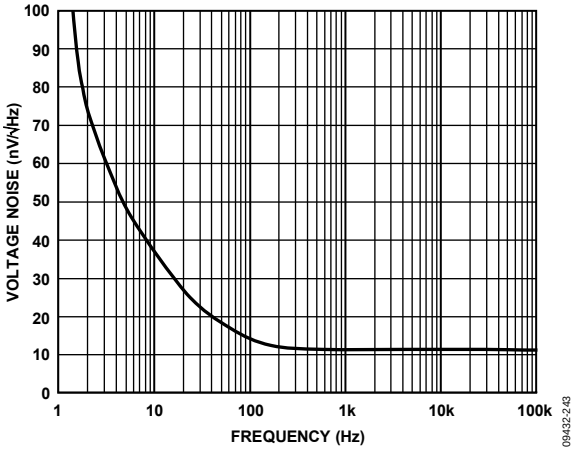


Figure 43. Voltage Noise Density vs. Frequency

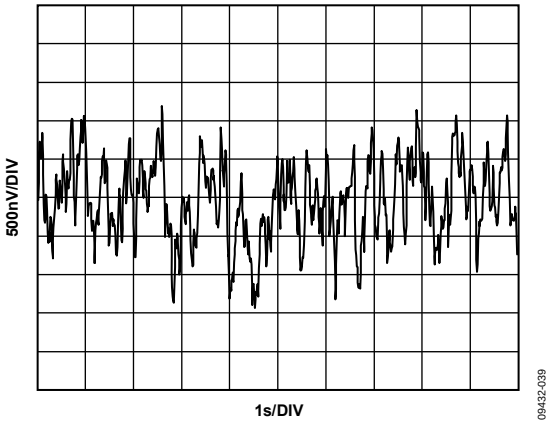


Figure 46. 0.1 Hz to 10 Hz Voltage Noise

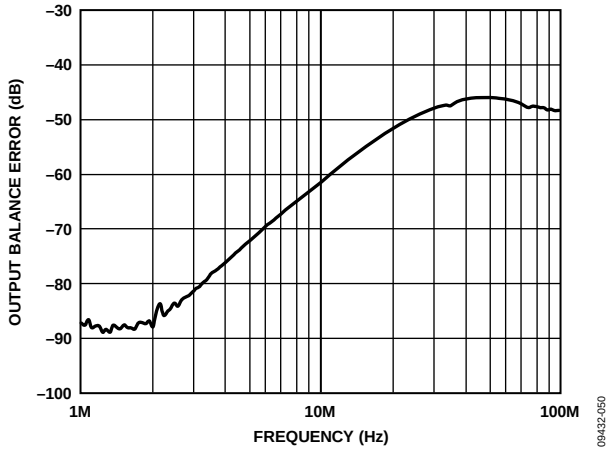


Figure 47. Output Balance Error vs. Frequency

TERMINOLOGY

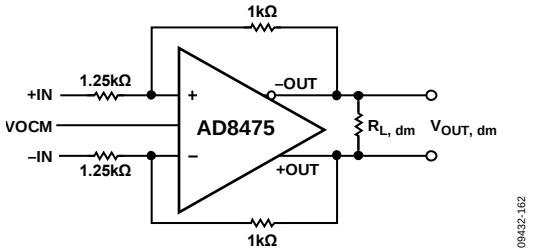


Figure 48. Signal and Circuit Definitions

Differential Voltage

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common ground reference. Similarly, the differential input voltage is defined as

$$V_{IN,\,dm} = (V_{+IN} - (V_{-IN}))$$

Common-Mode Voltage

Common-mode voltage refers to the average of two node voltages with respect to the local ground reference. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

The input common-mode voltage is defined as

$$V_{IN,\,cm} = (V_{+IN} + V_{-IN})/2$$

Balance

Output balance is a measure of how close the output differential signals are to being equal in amplitude and opposite in phase. Output balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider midpoint with the magnitude of the differential signal. By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{\Delta V_{OUT,\,cm}}{\Delta V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

OVERVIEW

The AD8475 is a fully differential amplifier, with integrated laser-trimmed resistors, that provides precision attenuating gains of 0.4 and 0.8. The internal differential amplifier of the AD8475 differs from conventional operational amplifiers in that it has two outputs whose voltages are equal in magnitude, but move in opposite directions (180° out of phase). An additional input, VOCM, sets the output common-mode voltage. Like an operational amplifier, it relies on high open-loop gain and negative feedback to force the output nodes to the desired voltages. The AD8475 is designed to greatly simplify single-ended-to-differential conversion, common-mode level shifting and precision attenuation of large signals so that they are compatible with low voltage, differential input ADCs.

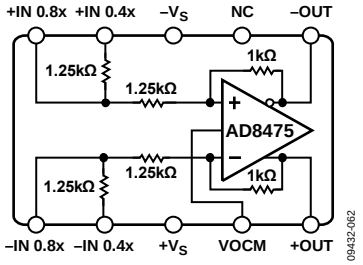


Figure 49. Block Diagram

CIRCUIT INFORMATION

The AD8475 amplifier uses a voltage feedback topology; therefore, the amplifier exhibits a nominally constant gain bandwidth product. Like a voltage feedback operational amplifier, the AD8475 also has high input impedance at its internal input terminals (the summing nodes of the internal amplifier) and low output impedance.

The AD8475 employs two feedback loops, one each to control the differential and common-mode output voltages. The differential feedback loop, which is fixed with precision laser trimmed on-chip resistors, controls the differential output voltage.

Output Common-Mode Voltage (VOCM)

The internal common-mode feedback controls the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value independent of the input voltage. The output common-mode voltage is forced by the internal common-mode feedback loop to be equal to the voltage applied to the VOCM input. The VOCM pin can be left unconnected, and the output common-mode voltage self-biases to midsupply by the internal feedback control.

Due to the internal common-mode feedback loop and the fully differential topology of the amplifier, the AD8475 outputs are precisely balanced over a wide frequency range. This means that the amplifier's differential outputs are very close to the ideal of being identical in amplitude and exactly 180° out of phase.

DC PRECISION

The dc precision of the AD8475 is highly dependent on the accuracy of its internal resistors. Using superposition to analyze the circuit shown in Figure 50, the following equation shows the relationship between the input and output voltages of the amplifier:

$$V_{IN,cm}\left(R_P - R_N\right) + V_{IN,dm}\frac{1}{2}\left(2R_PR_N + R_P + R_N\right)$$
$$= V_{OUT,cm}\left(R_P - R_N\right) + V_{OUT,dm}\frac{1}{2}\left(2 + R_P + R_N\right)$$

where,

$$R_P = \frac{RFP}{RGP},\ R_N = \frac{RFN}{RGN}$$

$$V_{IN,dm} = V_P - V_N$$

$$V_{IN,cm} = \frac{1}{2}(V_P + V_N)$$

The differential closed loop gain of the amplifier is

$$\frac{V_{OUT,dm}}{V_{IN,dm}} = \frac{2R_PR_N + R_P + R_N}{2 + R_P + R_N}$$

and the common rejection of the amplifier is

$$\frac{V_{OUT,dm}}{V_{IN,cm}} = \frac{2\left(R_P - R_N\right)}{2 + R_P + R_N}$$

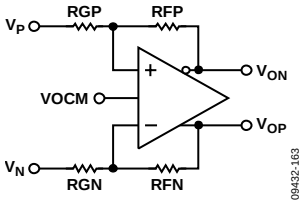


Figure 50. Functional Circuit Diagram of the AD8475 at a Given Gain

The preceding equations show that the gain accuracy and the common-mode rejection (CMRR) of the AD8475 are determined primarily by the matching of the feedback networks (resistor ratios). If the two networks are perfectly matched, that is, if R_P and R_N equal RF/RG, then the resistor network does not generate any CMRR errors and the differential closed loop gain of the amplifier reduces to

$$\frac{v_{OUT,dm}}{v_{IN,dm}} = \frac{RF}{RG}$$

The AD8475's integrated resistors are precision wafer-laser-trimmed to guarantee a minimum CMRR of 86dB (50µV/V), and gain error of less that 0.05%. To achieve equivalent precision and performance using a discrete solution, resistors must be matched to 0.01% or better.

INPUT VOLTAGE RANGE

The AD8475 can measure input voltages that are larger than the supply rails. The internal gain and feedback resistors form a divider, which reduces the input voltage seen by the internal input nodes of the amplifier. The largest voltage that can be measured is constrained by the capability of the amplifier's internal summing nodes. This voltage is defined by the input voltage and the ratio between the feedback and the gain resistors. Figure 51 shows the voltage at the internal summing nodes of the amplifier, defined by the input voltage and internal resistor network. Written in terms of the input and output common-mode voltages, this equation simplifies to

$$V_{PLUS} = V_{MINUS} = \frac{RG}{RF + RG}\left(V_{OUT,cm}\right) + \frac{RF}{RF + RG}\left(V_{IN,cm}\right)$$

For the AD8475, RF is 1 kΩ, and RG is either 2.5 kΩ for G = 0.4 or 1.25 kΩ when G = 0.8 is used.

The internal amplifier of the AD8475 has rail-to-rail inputs. To obtain accurate measurements with minimal distortion, the voltage at the internal inputs of the amplifier must stay below $+V_S - 1$ V and above $-V_S$.

For example, with $V_S = 5$ V in a G = 0.4 configuration, the AD8475 can measure a single-ended input as high as ±12.5 V and maintain its excellent distortion performance.

The AD8475 provides overvoltage protection for excessive input voltages beyond the supply rails. Integrated ESD protection diodes at the inputs prevent damage to the AD8475 up to $+V_S + 10.5$ V and $-V_S - 16$ V.

DRIVING THE AD8475

Care should be taken to drive the AD8475 with a low impedance source: for example, another amplifier. Source resistance can unbalance the resistor ratios and, therefore, significantly degrade the gain accuracy and common-mode rejection of the AD8475. For the best performance, source impedance to the AD8475 input terminals should be kept below 0.1 Ω. Refer to the DC Precision section for details on the critical role of resistor ratios in the precision of the AD8475.

POWER SUPPLIES

The AD8475 operates over a wide range of supply voltages. It can be powered on a single supply as low as 3 V and as high as 10 V. The AD8475 can also operate on dual supplies from ±1.5 V up to ±5 V

A stable dc voltage should be used to power the AD8475. Note that noise on the supply pins can adversely affect performance. For more information, see the PSRR performance curve in Figure 13.

Place a bypass capacitor of 0.1 µF between each supply pin and ground, as close as possible to each supply pin. Use a tantalum capacitor of 10 µF between each supply and ground. It can be farther away from the supply pins and, typically, it can be shared by other precision integrated circuits.

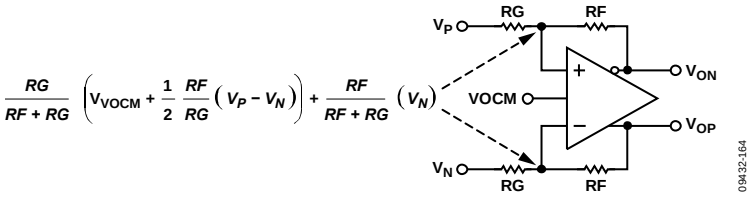


Figure 51. Voltages at the Internal Op Amp Inputs of the AD8475

APPLICATIONS INFORMATION

TYPICAL CONFIGURATION

The AD8475 is designed to facilitate single-ended-to-differential conversion, common-mode level shifting, and precision attenuation of large signals so that they are compatible with low voltage ADCs.

Figure 53 shows a typical connection diagram of the AD8475 in a gain of 0.4. To use the AD8475 in a gain of 0.8, drive the ±IN 0.8x inputs with a low impedance source.

SINGLE-ENDED TO DIFFERENTIAL CONVERSION

Many industrial systems use single-ended voltages in the signal path; however, the signals are frequently processed by high performance differential input ADCs for higher precision. The AD8475 performs the critical function of precisely converting single-ended signals to the differential inputs of precision ADCs, and it does so with no need for external components.

To convert a single-ended signal to a differential signal, connect one input to the signal source and the other input to ground (see Figure 55). Note that either input can be driven by the source with the only effect being that the outputs have reversed polarity. The AD8475 also accepts truly differential input signals in precision systems with differential signal paths.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The VOCM pin of the AD8475 is internally biased with a precision voltage divider comprising two 200 kΩ resistors between the supplies. This divider level shifts the output to midsupply. Relying on the internal bias results in an output common-mode voltage that is within 0.01% of the expected value.

In cases where control of the output common-mode level is desired, an external source with output resistance less than 100 Ω can be used to drive the VOCM pin. If an external voltage divider consisting of equal resistor values is used to set VOCM to midsupply, higher values can be used because the external resistors are placed in parallel with the internal resistors. The output common-mode gain error listed in the Specifications section assumes that the VOCM input is driven by a low impedance voltage source.

Because of the internal divider, the VOCM pin sources and sinks current, depending on the externally applied voltage and its associated source resistance.

It is also possible to connect the VOCM input to the voltage reference of an ADC via a resistor divider as shown in Figure 55. Connecting the VOCM input in this manner reduces power supply noise and optimizes the output common mode voltage of the AD8475 to utilize the entire differential input voltage range of the ADC. If AD8475 is used with a single supply that is the same voltage as the voltage reference, two 10 kΩ resistors connected to the VOCM pin is sufficient to override the internal resistors. Otherwise, a voltage follower should be used to drive VOCM.

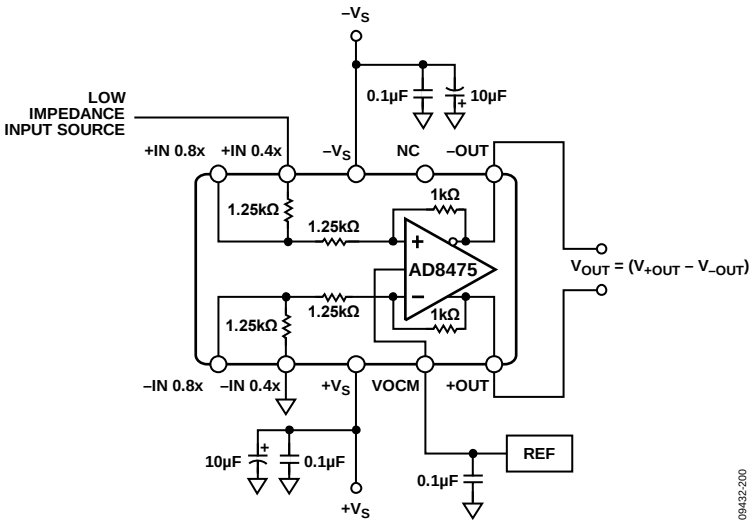


Figure 52. Typical Configuration—10-Lead MSOP

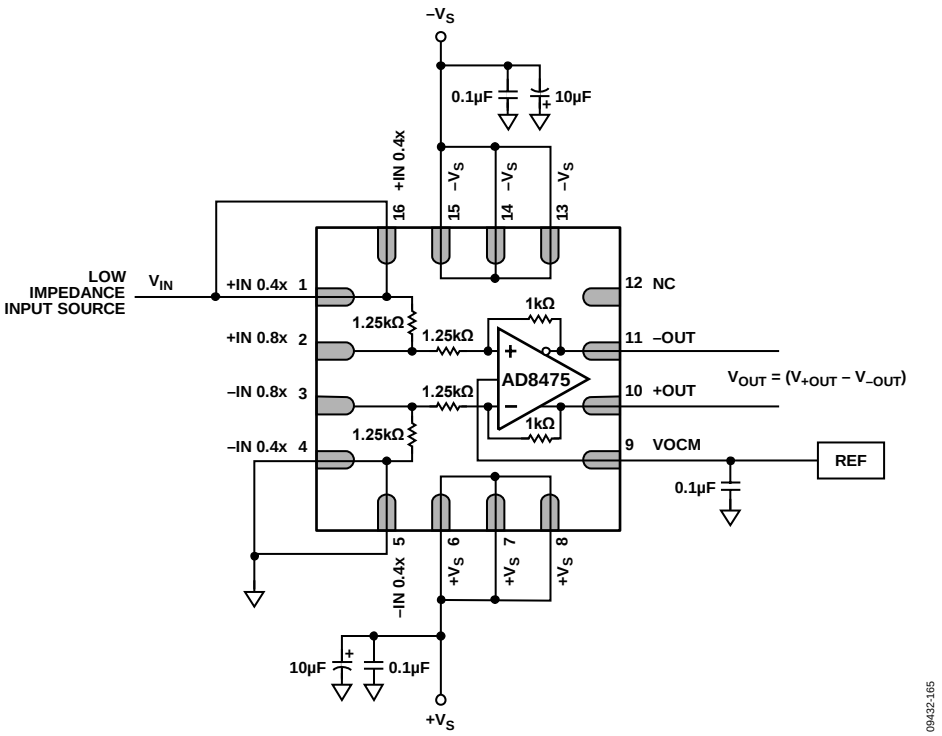


Figure 53. Typical Configuration—16-Lead LFCSP

HIGH PERFORMANCE ADC DRIVING

The AD8475 is ideally suited for broadband dc-coupled and industrial applications. The circuit in Figure 55 shows an industrial front-end connection for an AD8475 driving an AD7982, a 18-bit, 1 MSPS ADC, with dc coupling on the AD8475 input and output. (The AD7982 achieves its optimum performance when driven differentially.) The AD8475 performs the attenuation of a 20 V p-p input signal, level shifts it, and converts it to a differential signal without the need for any external components. The AD8475 eliminates the need for dual supplies at the front end to accept large bipolar signals. It also eliminates the need for a precision resistor network for attenuation, and a transformer to drive the ADC and perform the single-ended-to-differential conversion.

The ac and dc performance of the AD8475 are compatible with the 18-bit, 1 MSPS AD7982 PulSAR® ADC and other 16-bit and 18-bit members of the family, which have sampling rates up to 4 MSPS. Some suitable high performance differential ADCs are listed in Table 6.

Table 6. High Performance SAR ADCs

Part	Resolution	Sample Rate	Description
AD7984	18 Bits	1.33 MSPS	True differential input, 14 mW, 2.5 V ADC
AD7982	18 Bits	1 MSPS	True differential Input, 7.0 mW, 2.5 V ADC
AD7690	18 Bits	400 kSPS	True differential input, 4.5 mW, 5 V ADC
AD7641	18 Bits	2 MSPS	True differential input, 75 mW, 2.5 V ADC

In this example, the AD8475 is powered with a single 5 V supply and used in a gain of 0.4, with a single-ended input converted to a differential output. The input is a 20 V p-p symmetric, ground-referenced bipolar signal. With an output common-mode voltage of 2.5 V, each AD8475 output swings between 0.5 V and 4.5 V, opposite in phase, providing an 8 V p-p differential signal to the ADC input.

The differential RC network between the AD8475 output and the ADC provides a single-pole filter that reduces undesirable aliasing effects and high frequency noise. The common-mode bandwidth of the filter is 29.5 MHz (20 Ω, 270 pF), and the differential bandwidth is 3.1 MHz (40 Ω, 1.3 nF).

The VOCM input is bypassed for noise reduction, and set externally with 1% resistors to maximize output dynamic range on a single 5 V supply.

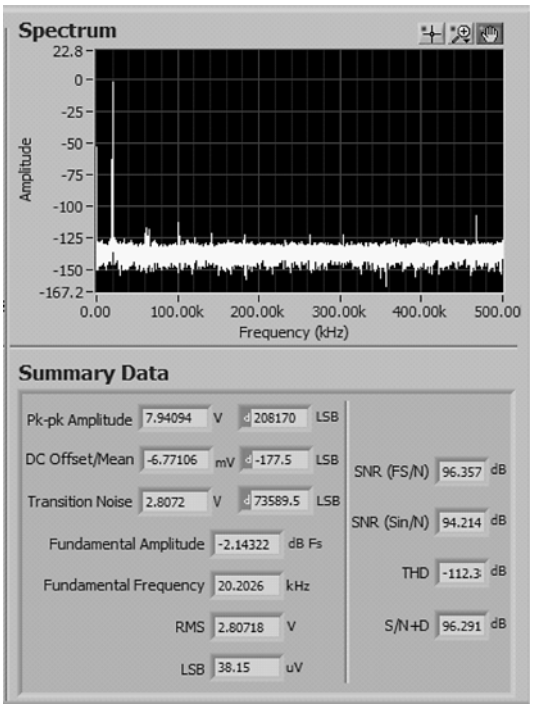


Figure 54. FFT Results of the AD8475 Driving the AD7982

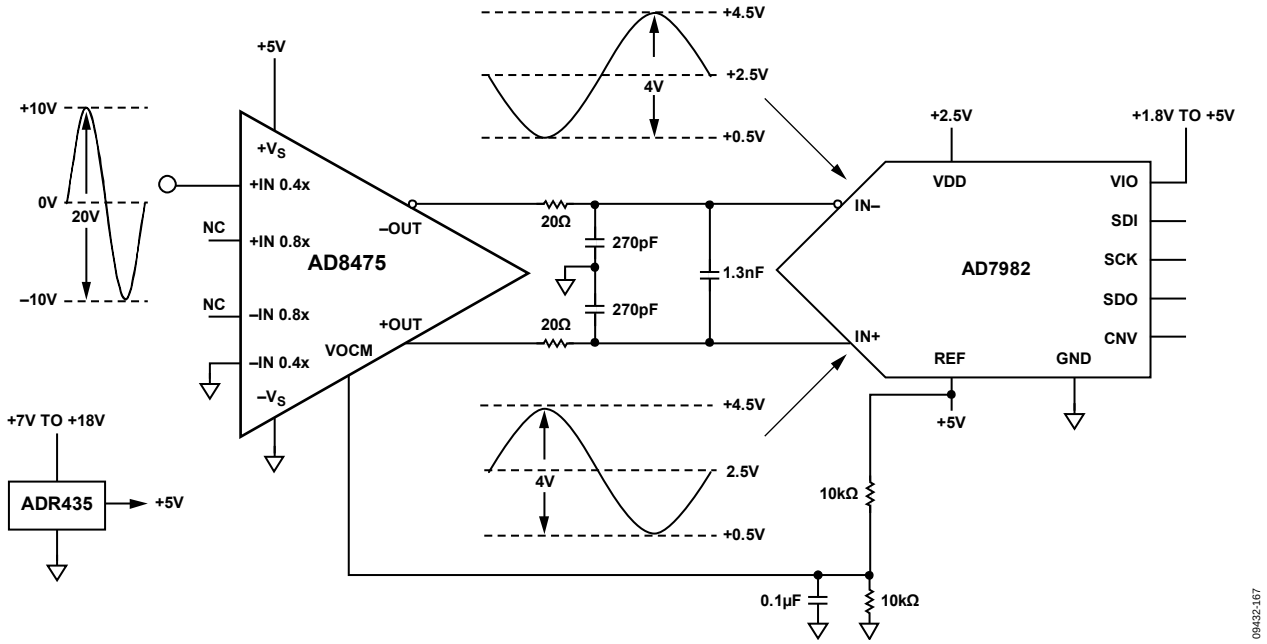


Figure 55. Attenuation and Level Shifting of Industrial Voltages to Drive Single-Supply Precision ADC

AD8475 EVALUATION BOARD

An evaluation board for the AD8475 is available to facilitate standalone testing of the AD8475 performance and functionality for customer evaluation and system design. The board provides the user flexibility to configure the AD8475 in the desired gain (0.4 or 0.8) and to install the suitable input and load impedances.

The AD8475-EVALZ board is designed so that a user can easily evaluate system performance when the AD8475 is mated with any Analog Devices, Inc., SAR ADC. The board can be installed with SMB connectors that mate directly to the Pulsar® Analog-to-Digital Converter Evaluation Kit.

See the AD8475 product page for more information on the AD8475-EVALZ.

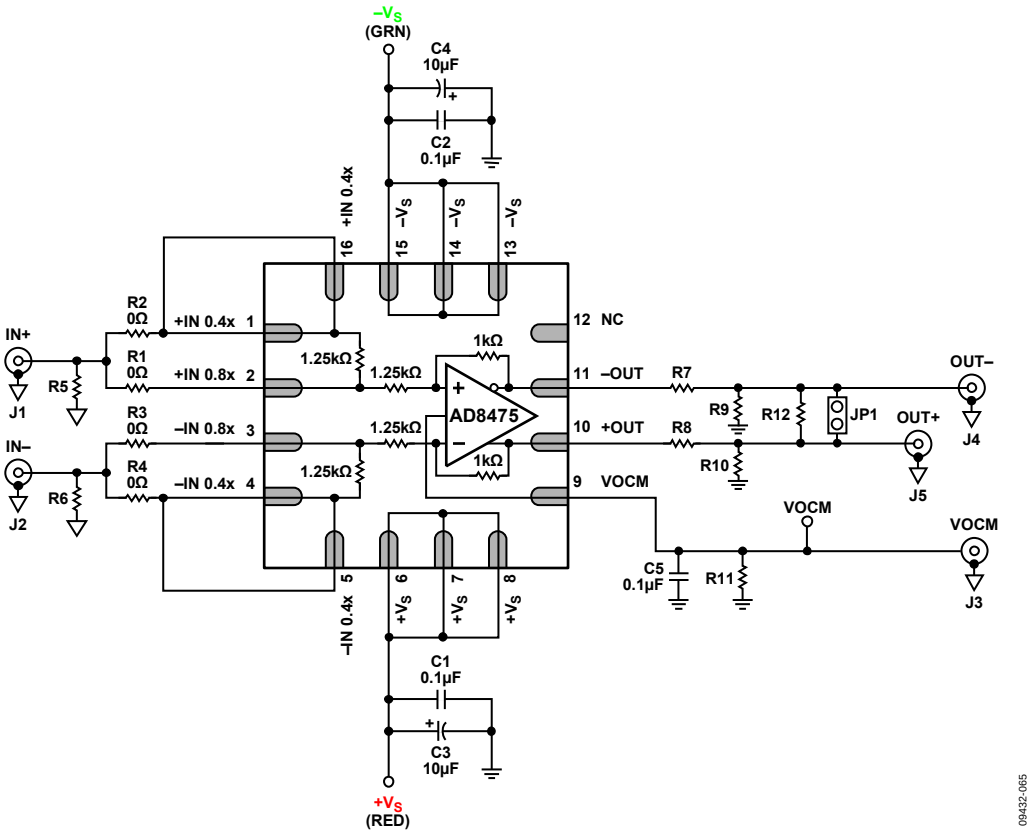
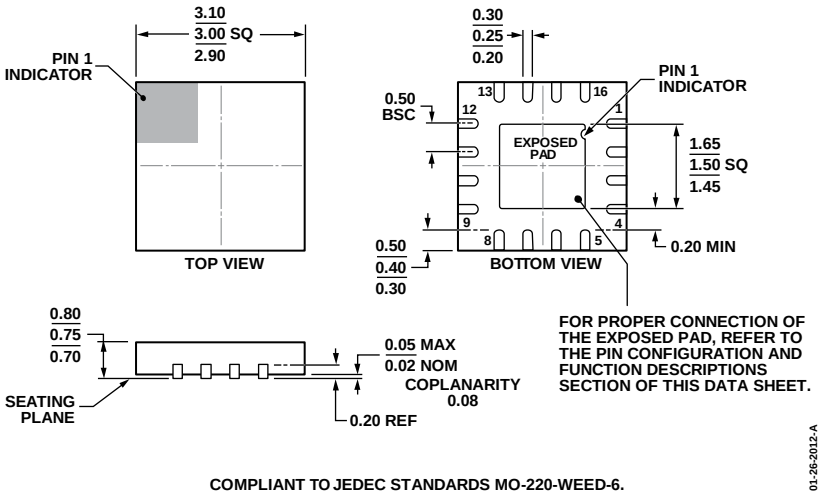


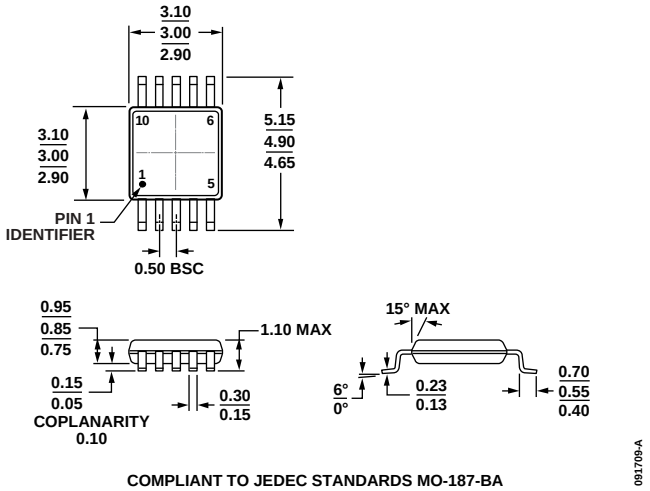
Figure 56. AD8475-EVALZ Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 57. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-27)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 58. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8475ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-27	Y3H
AD8475ACPZ-RL	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-27	Y3H
AD8475ACPZ-WP	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-27	Y3H
AD8475BRMZ	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [MSOP]	RM-10	Y41
AD8475BRMZ-R7	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [MSOP]	RM-10	Y41
AD8475BRMZ-RL	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [MSOP]	RM-10	Y41
AD8475ARMZ	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [MSOP]	RM-10	Y31
AD8475ARMZ-R7	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [MSOP]	RM-10	Y31
AD8475ARMZ-RL	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [MSOP]	RM-10	Y31
AD8475-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

D09432-0-1/14(C)

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