High Voltage, Precision Operational Amplifier

Data Sheet

ADA4700-1

FEATURES

- Low input offset voltage: 0.2 mV typical
- High output current drive: 30 mA
- Wide range of operating voltage: ±5 V to ±50 V
- High slew rate: 20 V/µs typical
- High gain bandwidth product: 3.5 MHz typical
- Thermal regulation at junction temperature >145°C
- Ambient temperature range: −40°C to +85°C
- Low input bias current ≤ 15 nA typical

APPLICATIONS

- Automated and bench top test equipment
- High voltage regulators and power amplifiers
- Data acquisition and signal conditioning
- Piezo drivers and predrivers
- General-purpose current sensing

PIN CONFIGURATION

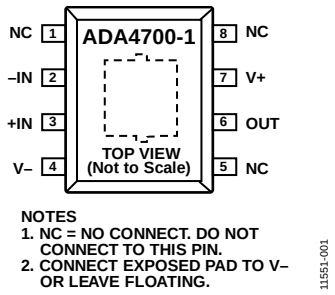

Figure 1.

GENERAL DESCRIPTION

The ADA4700-1 is a high voltage, precision, single-channel operational amplifier with a wide operating voltage range (±5 V to ±50 V) and relatively high output current drive. Its advanced design combines low power (170 mW for a ±50 V supply), high bandwidth (3.5 MHz), and a high slew rate with unity-gain stability and phase inversion free performance. The ability to swing near rail to rail at the output enables designers to maximize signal-to-noise ratios (SNRs).

The ADA4700-1 is designed for applications requiring both ac and dc precision performance, making the ADA4700-1 useful in a wide variety of applications, including high voltage test equipment and instrumentation, high voltage regulators and power amplifiers, power supply control and protection, and as an amplifier or buffer for transducers with wide output ranges. It is particularly well suited for high intensity LED testing applications where it provides highly accurate voltage and current feedback as well as a predriver to provide accurate voltage and/or current sourcing stimulus to the LED string under test.

The ADA4700-1 is specified over the industrial temperature range of −40°C to +85°C and includes thermal regulation at a junction temperature greater than 145°C and an integrated current limit. The ADA4700-1 is available in a thermally enhanced, 8-lead SOIC package with an exposed pad.

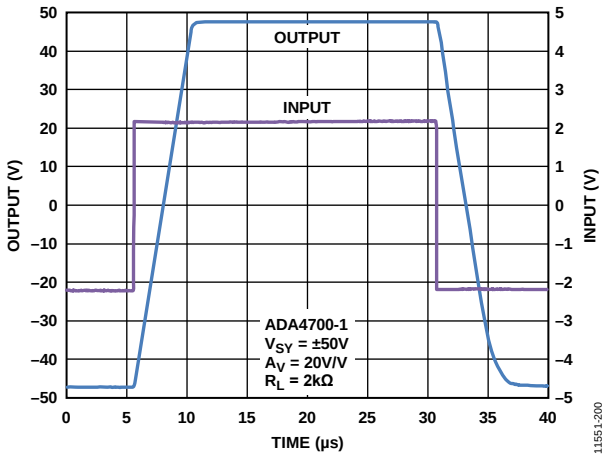

Figure 2. Slew Rate

Rev. 0

Document Feedback

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Technical Support
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REVISION HISTORY

8/13—Revision 0: Initial Version

SPECIFICATIONS

V_{SY} = ±50 V ELECTRICAL CHARACTERISTICS

V_{SY} = ±50 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	2	mV
		−40°C ≤ T_A ≤ +85°C			2.5	mV
Offset Voltage Drift[1]	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		2	13	µV/°C
Input Bias Current	I_B			15	30	nA
		−40°C ≤ T_A ≤ +85°C			50	nA
Input Offset Current	I_{OS}			2	25	nA
		−40°C ≤ T_A ≤ +85°C			30	nA
Input Voltage Range	IVR	−40°C ≤ T_A ≤ +85°C	(V−) + 3		(V+) − 3	V
Common-Mode Rejection Ratio	CMRR	(V−) + 3 V ≤ V_{CM} ≤ (V+) − 3 V	103	108		dB
		−40°C ≤ T_A ≤ +85°C	103			dB
Large Signal Voltage Gain	A_{VO}	−47 V ≤ V_{OUT} ≤ +47 V, R_L = 2 kΩ	103	106		dB
		−40°C ≤ T_A ≤ +85°C	100			dB
Input Impedance						
Common-Mode	$R_{IN}\|\|C_{INCM}$			2.3||5.3		MΩ||pF
Differential	$R_{IN}\|\|C_{INDM}$			2.3||0.5		MΩ||pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	48.0	48.5		V
		−40°C ≤ T_A ≤ +85°C	47.8			V
		R_L = 2 kΩ to GND	47.5	48.0		V
		−40°C ≤ T_A ≤ +85°C	47.3			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−48.5	−48.0	V
		−40°C ≤ T_A ≤ +85°C			−47.8	V
		R_L = 2 kΩ to GND		−48.0	−47.5	V
		−40°C ≤ T_A ≤ +85°C			−47.3	V
Capacitive Load Drive[2]	C_L	A_V = +1		1		nF
Output Current Drive[3]	I_{OUT}			30		mA
Short-Circuit Limit	I_{SC}	Sourcing/Sinking		+72/−65		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 Hz, A_V = +1		0.001		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±55 V	110	130		dB
		−40°C ≤ T_A ≤ +85°C	110			dB
Supply Current per Amplifier	I_{SY}			1.7	2.2	mA
		−40°C ≤ T_A ≤ +85°C			2.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{IN} = ±45 V p-p, A_V = +1, R_L = 2 kΩ, C_L = 300 pF		20		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, A_V = +100		3.5		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, A_V = +1		2.6		MHz
−3 dB Bandwidth	−3 dB	V_{IN} = 5 mV p-p, A_V = −1		4.8		MHz
Phase Margin	ΦM	V_{IN} = 5 mV p-p, R_L = 1 MΩ, C_L = 35 pF, A_V = −1		70		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 30 V p-p, R_L = 10 kΩ, C_L = 5 pF, A_V = −1		4		µs
Settling Time to 0.01%	t_S	V_{IN} = 30 V p-p, R_L = 10 kΩ, C_L = 5 pF, A_V = −1		8		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	A_V = +1, V_{IN} = 10 V p-p at 1 kHz, R_L = 10 kΩ, bandwidth = 80 kHz		0.0002		%
Peak-to-Peak Noise	$e_{n\ p-p}$	f = 0.1 Hz to 10 Hz		800		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		14.7		nV/√Hz
		f = 10 Hz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		400		fA/√Hz

[1] See Figure 7 through Figure 9.
[2] Overshoot vs. temperature and capacitive load performance is shown in Figure 27 through Figure 30. Refer to the Driving Capacitive Loads section for recommendations on driving capacitive loads greater than 1 nF.
[3] Refer to the Safe Operating Area section.

V_{SY} = ±24 V ELECTRICAL CHARACTERISTICS

V_{SY} = ±24 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	2	mV
		−40°C ≤ T_A ≤ +85°C			2.5	mV
Offset Voltage Drift[1]	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		2.5	15	µV/°C
Input Bias Current	I_B			5	30	nA
		−40°C ≤ T_A ≤ +85°C			50	nA
Input Offset Current	I_{OS}			2	25	nA
		−40°C ≤ T_A ≤ +85°C			30	nA
Input Voltage Range	IVR	−40°C ≤ T_A ≤ +85°C	(V−) + 3		(V+) − 3	V
Common-Mode Rejection Ratio	CMRR	(V−) + 3 V ≤ V_{CM} ≤ (V+) − 3 V	100	103		dB
		−40°C ≤ T_A ≤ +85°C	100			dB
Large Signal Voltage Gain	A_{VO}	−21 V ≤ V_{OUT} ≤ +21 V, R_L = 2 kΩ	103	105		dB
		−40°C ≤ T_A ≤ +85°C	100			dB
Input Impedance						
Common-Mode	$R_{IN}\|\|C_{INCM}$			2.3||5.3		MΩ||pF
Differential	$R_{IN}\|\|C_{INDM}$			2.3||0.5		MΩ||pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	22.2	22.5		V
		−40°C ≤ T_A ≤ +85°C	22.0			V
		R_L = 2 kΩ to GND	22.0	22.4		V
		−40°C ≤ T_A ≤ +85°C	21.8			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND		−22.5	−22.2	V
		−40°C ≤ T_A ≤ +85°C			−22.0	V
		R_L = 2 kΩ to GND		−22.4	−22.0	V
		−40°C ≤ T_A ≤ +85°C			−21.8	V
Capacitive Load Drive[2]	C_L	A_V = +1		1		nF
Output Current Drive	I_{OUT}			30		mA
Short-Circuit Limit[3]	I_{SC}	Sourcing/Sinking		+72/−65		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 Hz, A_V = +1		0.001		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±55 V	110	130		dB
		−40°C ≤ T_A ≤ +85°C	110			dB
Supply Current per Amplifier	I_{SY}			1.65	2.1	mA
		−40°C ≤ T_A ≤ +85°C			2.3	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{IN} = ±20 V p-p, A_V = +1, R_L = 2 kΩ, C_L = 300 pF		20		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, A_V = +100		3.5		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, A_V = +1		2.6		MHz
−3 dB Bandwidth	−3 dB	V_{IN} = 5 mV p-p, A_V = −1		4.8		MHz
Phase Margin	ΦM	V_{IN} = 5 mV p-p, R_L = 1 MΩ, C_L = 35 pF, A_V = −1		70		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 20 V p-p, R_L = 10 kΩ, C_L = 5 pF, A_V = −1		4		µs
Settling Time to 0.01%	t_S	V_{IN} = 20 V p-p, R_L = 10 kΩ, C_L = 5 pF, A_V = −1		9		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	A_V = +1, V_{IN} = 10 V p-p at 1 kHz, R_L = 10 kΩ, bandwidth = 80 kHz		0.0002		%
Peak-to-Peak Noise	$e_{n\ p-p}$	f = 0.1 Hz to 10 Hz		800		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		14.7		nV/√Hz
		f = 10 Hz		27		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		400		fA/√Hz

[1] See Figure 7 through Figure 9.
[2] Overshoot vs. temperature and capacitive load performance is shown in Figure 27 through Figure 30. Refer to the Driving Capacitive Loads section for recommendations on driving capacitive loads greater than 1 nF.
[3] Refer to the Safe Operating Area section.

V_{SY} = ±5 V ELECTRICAL CHARATERISTICS

V_{SY} = ±5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	2	mV
		−40°C ≤ T_A ≤ +85°C			2.5	mV
Offset Voltage Drift[1]	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +85°C		3		µV/°C
Input Bias Current	I_B			5	30	nA
		−40°C ≤ T_A ≤ +85°C			50	nA
Input Offset Current	I_{OS}			2	25	nA
		−40°C ≤ T_A ≤ +85°C			30	nA
Input Voltage Range	IVR	−40°C ≤ T_A ≤ +85°C	−2		+2	V
Common-Mode Rejection Ratio	CMRR	−2 V ≤ V_{CM} ≤ +2 V	86	89		dB
		−40°C ≤ T_A ≤ +85°C	86			dB
Large Signal Voltage Gain	A_{VO}	−2 V ≤ V_{OUT} ≤ +2 V, R_L = 2 kΩ	97	99		dB
		−40°C ≤ T_A ≤ +85°C	95			dB
Input Impedance						
Common-Mode	$R_{IN}\|\|C_{INCM}$			2.3||5.3		MΩ||pF
Differential	$R_{IN}\|\|C_{INDM}$			2.3||0.5		MΩ||pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	3.4	3.6		V
		−40°C ≤ T_A ≤ +85°C	3.2			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		−3.6	−3.4	V
		−40°C ≤ T_A ≤ +85°C			−3.2	V
Capacitive Load Drive[2]	C_L	A_V = +1		1		nF
Output Current Drive	I_{OUT}			30		mA
Short Circuit Limit[3]	I_{SC}	Sourcing/Sinking		+72/−65		mA
Closed-Loop Impedance	Z_{OUT}	f = 100 Hz, A_V = +1		0.003		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±55 V	110	130		dB
		−40°C ≤ T_A ≤ +85°C	110			dB
Supply Current per Amplifier	I_{SY}			1.5	2	mA
		−40°C ≤ T_A ≤ +85°C			2.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{IN} = ±2 V p-p, A_V = +1, R_L = 2 kΩ, C_L = 300 pF		18		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, A_V = +100		3.5		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, A_V = +1		2.6		MHz
−3 dB Bandwidth	−3 dB	V_{IN} = 5 mV p-p, A_V = −1		4.8		MHz
Phase Margin	ΦM	V_{IN} = 5 mV p-p, R_L = 1 MΩ, C_L = 35 pF, A_V = −1		70		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 6 V p-p, R_L = 10 kΩ, C_L = 5 pF, A_V = −1		1.5		µs
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	A_V = +1, V_{IN} = 2 V p-p at 1 kHz, R_L = 10 kΩ, bandwidth = 80 kHz		0.0005		%
Peak-to-Peak Noise	$e_{n\ p-p}$	f = 0.1 Hz to 10 Hz		800		nV p-p
Voltage Noise Density	e_n	f = 1 kHz		14.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		400		fA/√Hz

[1] See Figure 7 through Figure 9.
[2] Overshoot vs. temperature and capacitive load performance is shown in Figure 27 through Figure 30. Refer to the Driving Capacitive Loads section for recommendations on driving capacitive loads greater than 1 nF.
[3] Refer to the Safe Operating Area section.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	110 V
Input Voltage	$V- \le V_{IN} \le V+$
Input Current	±10 mA
Differential Input Voltage	$V- \le V_{IN} \le V+$
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range[1]	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD	
Charged Device Model (CDM)	1250 V
Human Body Model (HBM)	4500 V
Machine Model (MM)	200 V

[1] Refer to the Thermal Management section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The values in Table 5 were obtained per JEDEC standard JESD51.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N_EP	45	30	°C/W

Board layout impacts thermal characteristics such as θ_{JA}. When proper thermal management techniques are used, a better θ_{JA} can be achieved. Refer to the Thermal Management section for additional information.

Although the exposed pad can be left floating, it must be connected to an external V− plane for proper thermal management.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

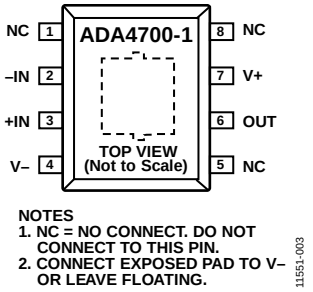

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 8	NC	No Connect. Do not connect to these pins.
2	–IN	Inverting Input.
3	+IN	Noninverting Input.
4	V–	Negative Supply Voltage.
6	OUT	Output.
7	V+	Positive Supply Voltage.
9	EPAD	Exposed Pad. Connect the exposed pad to V– or leave floating. The exposed pad is electrically connected to the device.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

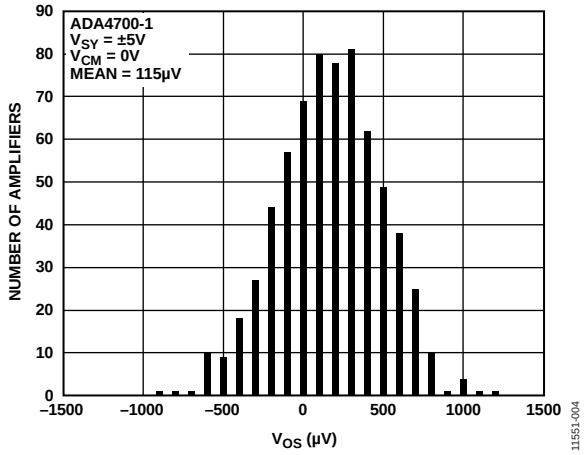

Figure 4. Input Offset Voltage Distribution, V_{SY} = ±5 V

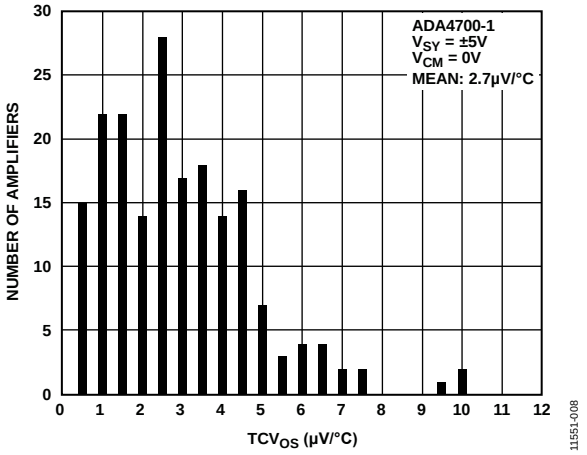

Figure 7. Input Offset Voltage Drift Distribution, V_{SY} = ±5 V

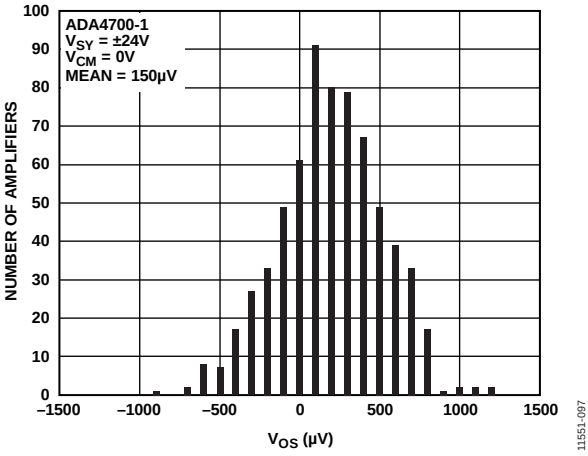

Figure 5. Input Offset Voltage Distribution, V_{SY} = ±24 V

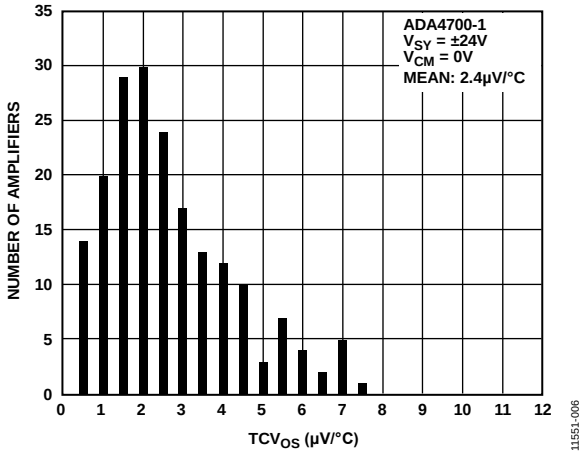

Figure 8. Input Offset Voltage Drift Distribution, V_{SY} = ±24 V

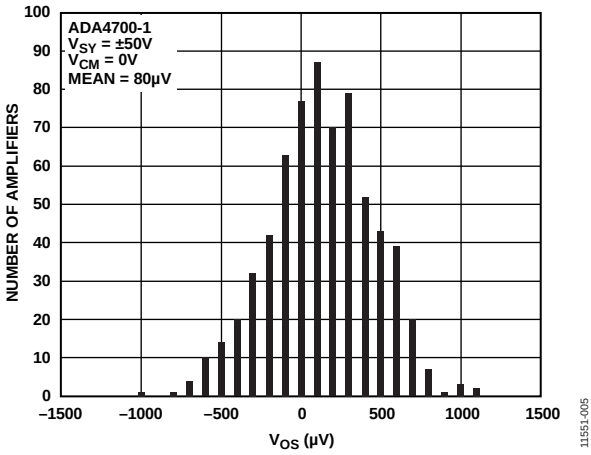

Figure 6. Input Offset Voltage Distribution, V_{SY} = ±50 V

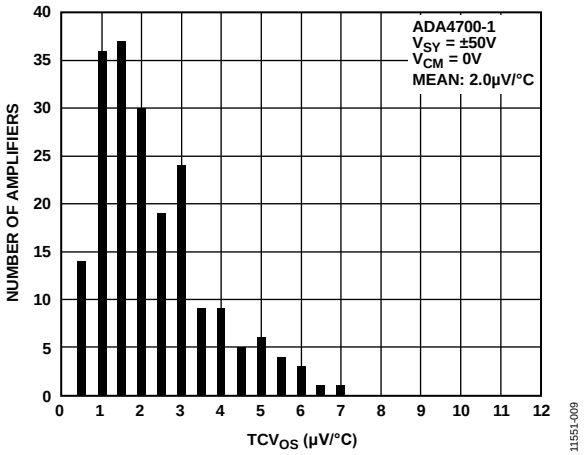

Figure 9. Input Offset Voltage Drift Distribution, V_{SY} = ±50 V

T_A = 25°C, unless otherwise noted.

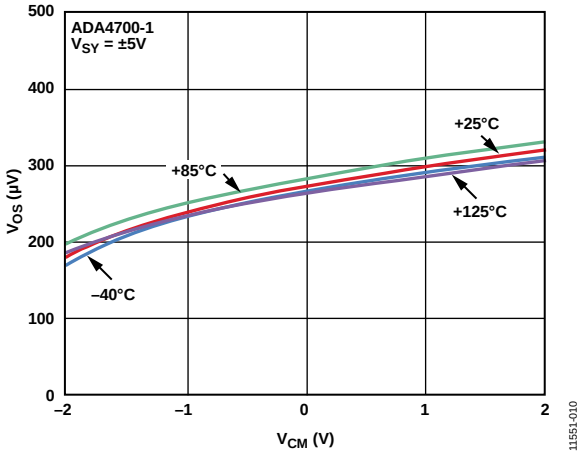

Figure 10. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±5 V

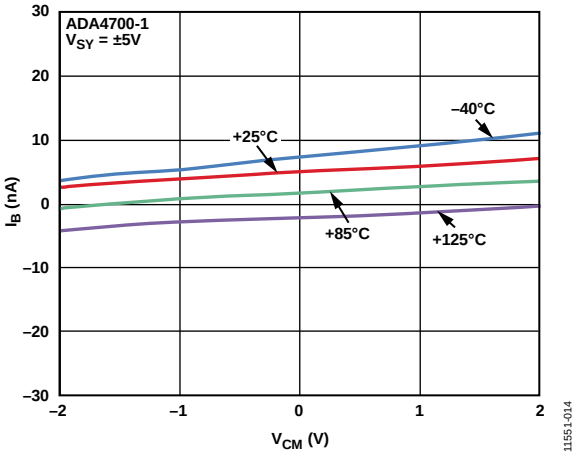

Figure 13. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}) and Temperature, V_{SY} = ±5 V

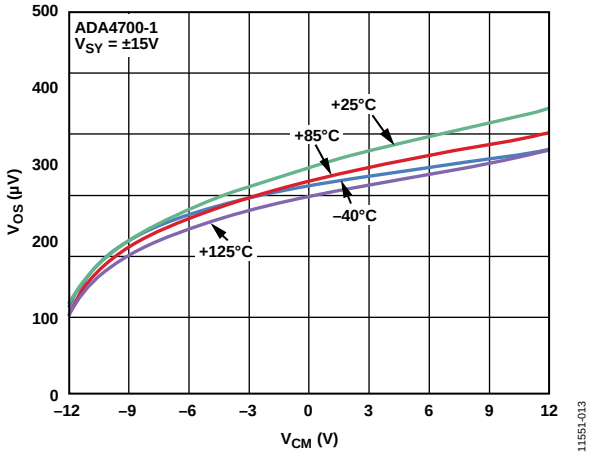

Figure 11. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±15 V

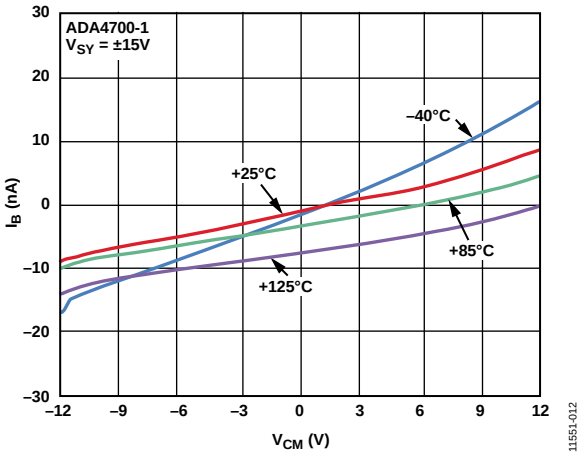

Figure 14. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}) and Temperature, V_{SY} = ±15 V

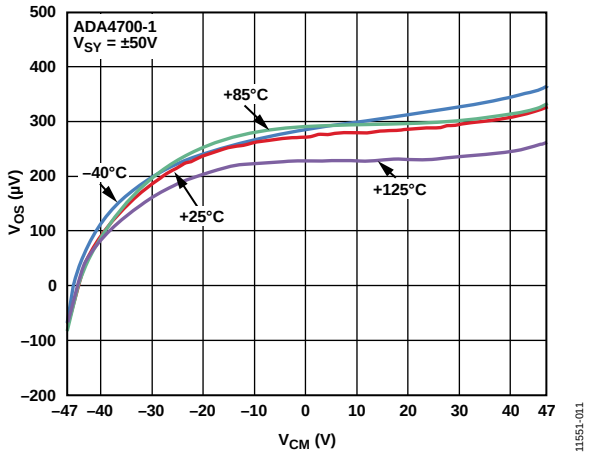

Figure 12. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±50 V

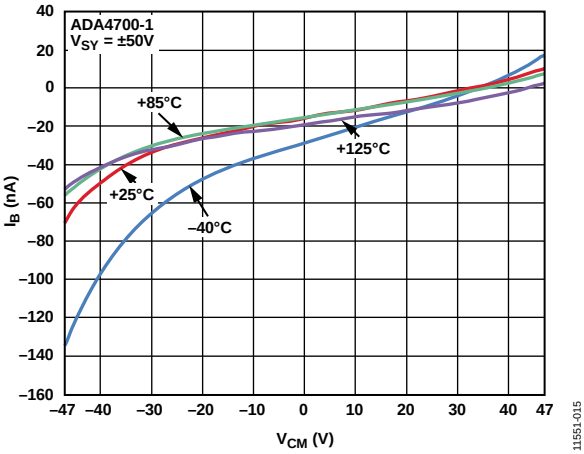

Figure 15. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}) and Temperature, V_{SY} = ±50 V

T_A = 25°C, unless otherwise noted.

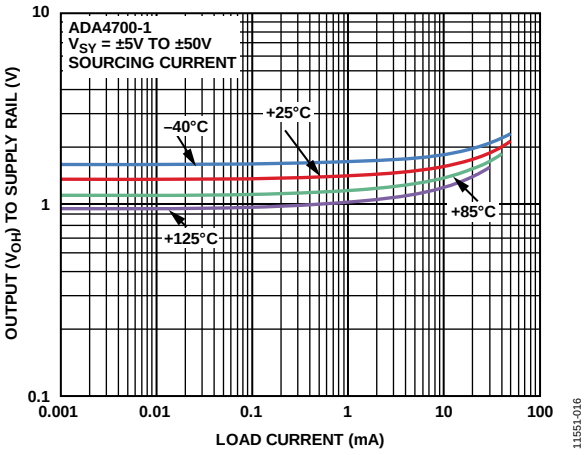

Figure 16. Output Voltage (V_{OH}) to Supply Rail vs. Load Current, V_{SY} = ±5 V to ±50 V

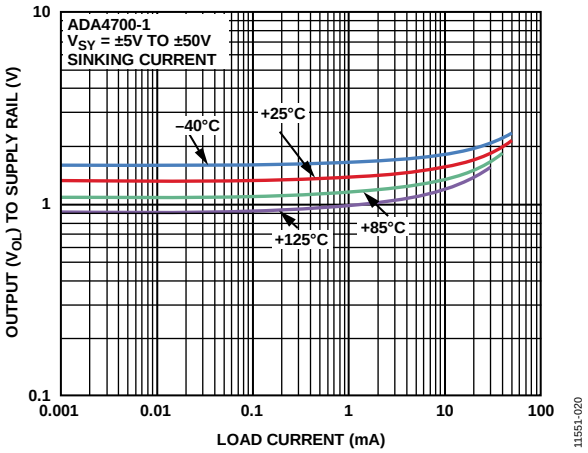

Figure 19. Output Voltage (V_{OL}) to Supply Rail vs. Load Current, V_{SY} = ±5 V to ±50 V

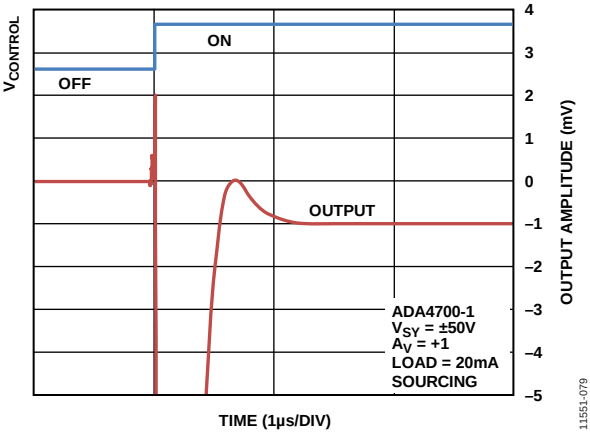

Figure 17. Output Current Transient Settling Time (Sourcing), V_{SY} = ±50 V, Refer to Figure 56 for the Test Circuit

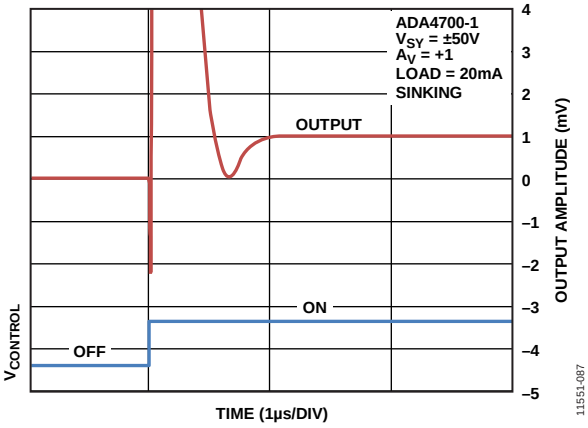

Figure 20. Output Current Transient Settling Time (Sinking), V_{SY} = ±50 V, Refer to Figure 57 for the Test Circuit

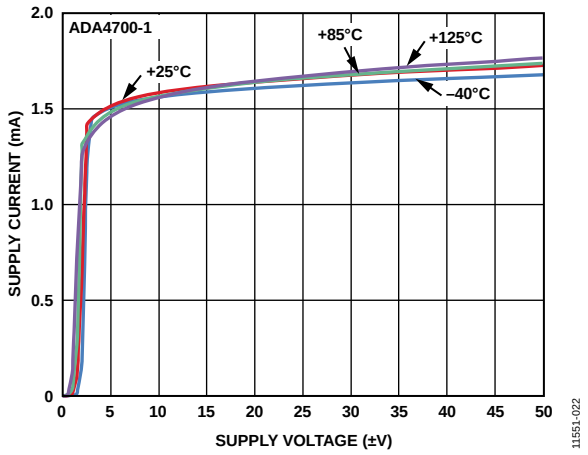

Figure 18. Supply Current vs. Supply Voltage

T_A = 25°C, unless otherwise noted.

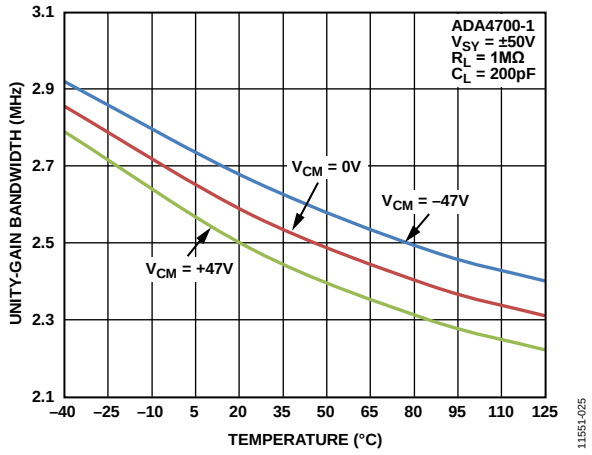

Figure 21. Unity-Gain Bandwidth vs. Temperature, V_{SY} = ±50 V

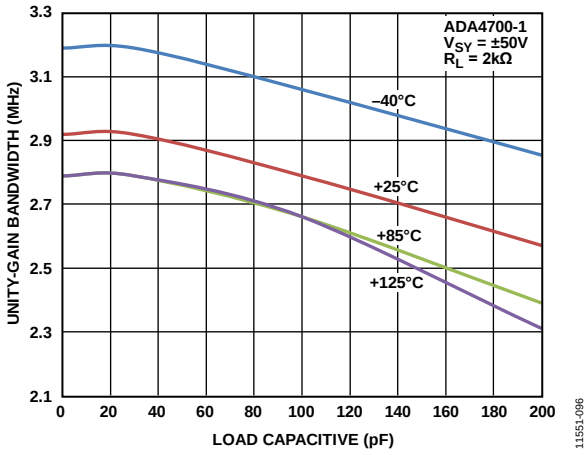

Figure 24. Unity-Gain Bandwidth vs. Load Capacitance and Temperature, V_{SY} = ±50 V

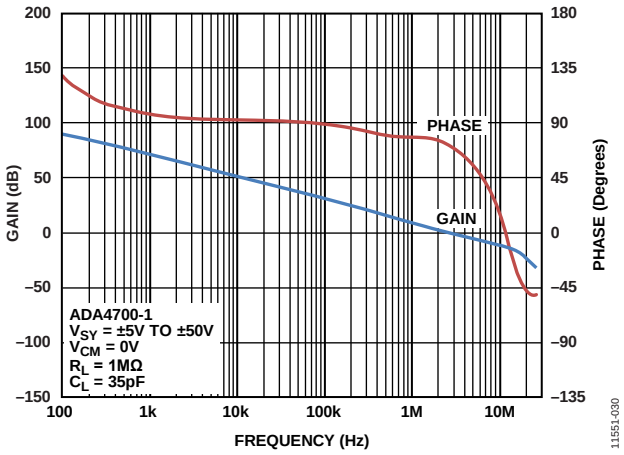

Figure 22. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±5 V to ±50 V

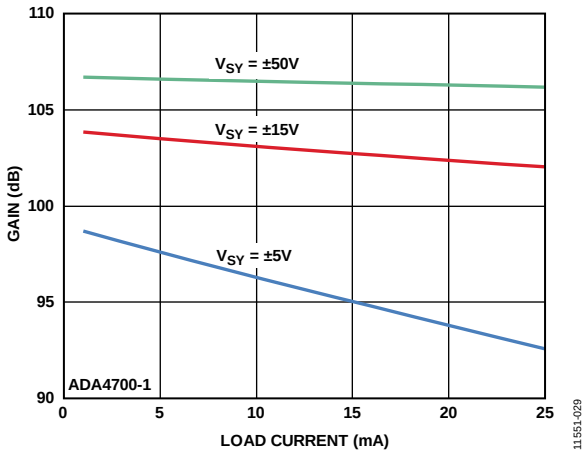

Figure 25. Open-Loop Gain vs. Load Current for Various Supply Voltages

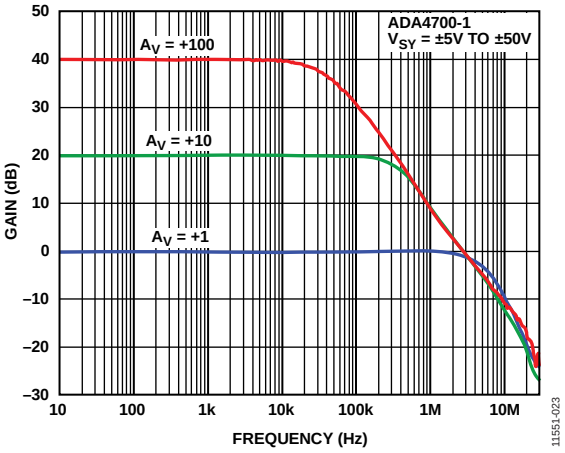

Figure 23. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V to ±50 V

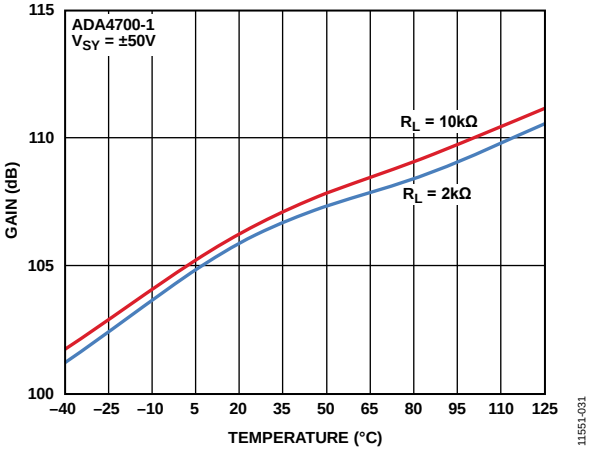

Figure 26. Open-Loop Gain vs. Temperature for Various Load Resistances, V_{SY} = ±50 V

T_A = 25°C, unless otherwise noted.

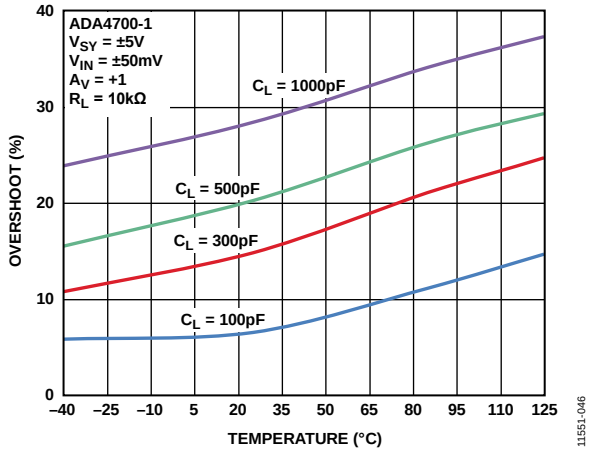

Figure 27. Small Signal Overshoot vs. Temperature for Various Capacitance Loads, V_{SY} = ±5 V

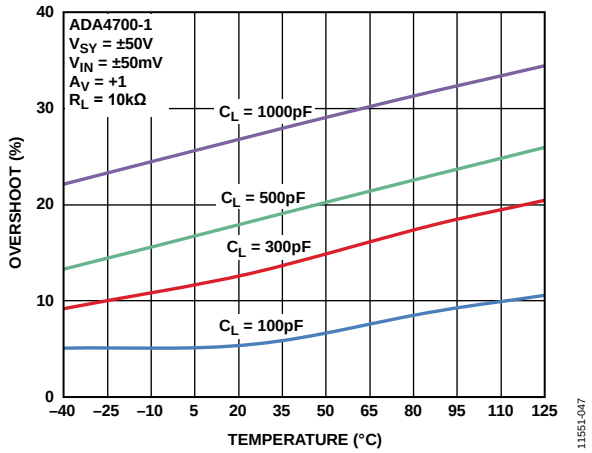

Figure 28. Small Signal Overshoot vs. Temperature for Various Capacitance Loads, V_{SY} = ±50 V

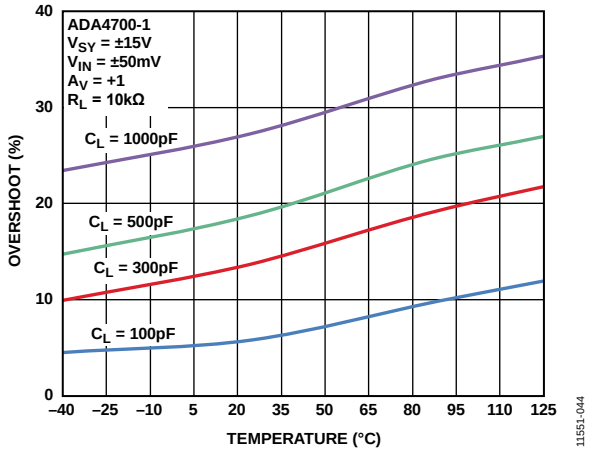

Figure 29. Small Signal Overshoot vs. Temperature for Various Capacitance Loads, V_{SY} = ±15 V

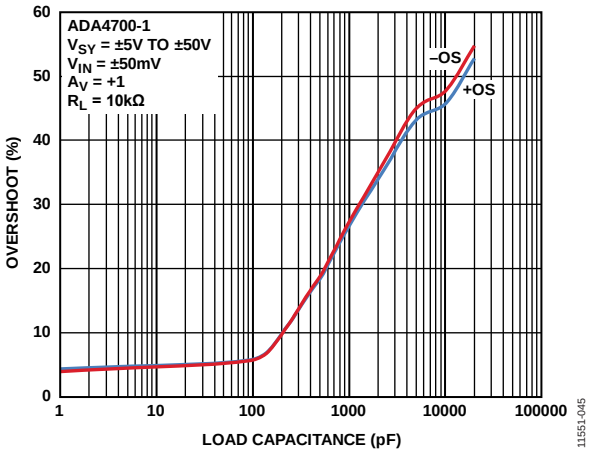

Figure 30. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±5 V to ±50 V

T_A = 25°C, unless otherwise noted.

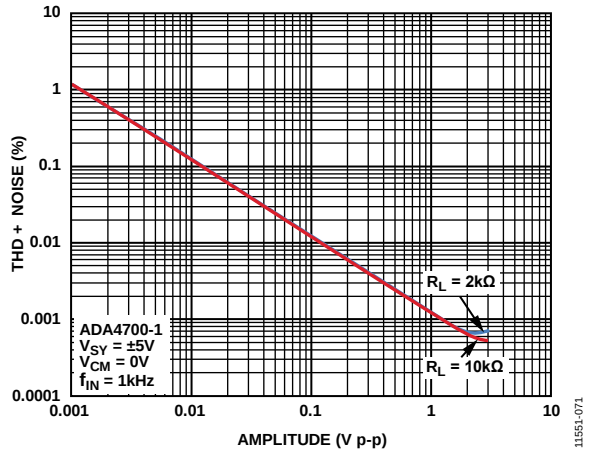

Figure 31. Total Harmonic Distortion + Noise (THD + Noise) vs. Amplitude, V_{SY} = ±5 V

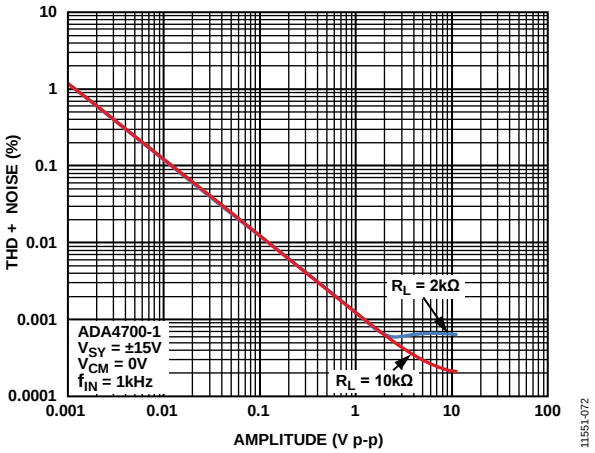

Figure 32. Total Harmonic Distortion + Noise (THD + Noise) vs. Amplitude, V_{SY} = ±15 V

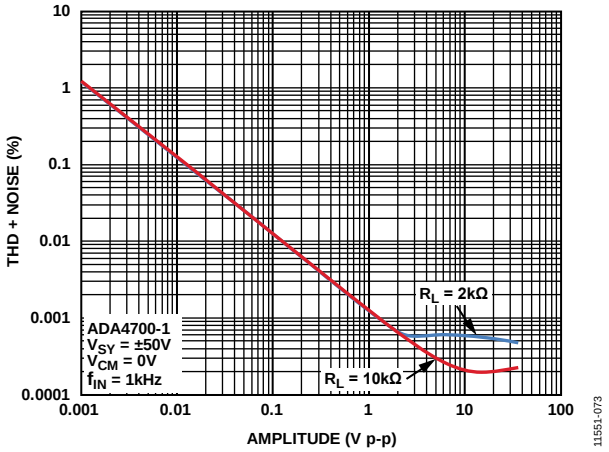

Figure 33. Total Harmonic Distortion + Noise (THD + Noise) vs. Amplitude, V_{SY} = ±50 V

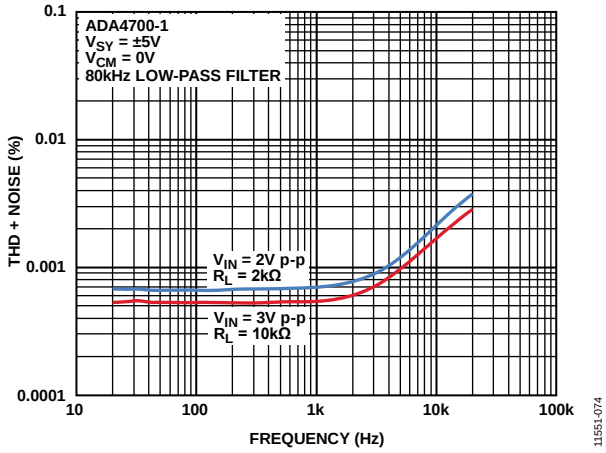

Figure 34. Total Harmonic Distortion + Noise (THD + Noise) vs. Frequency, V_{SY} = ±5 V

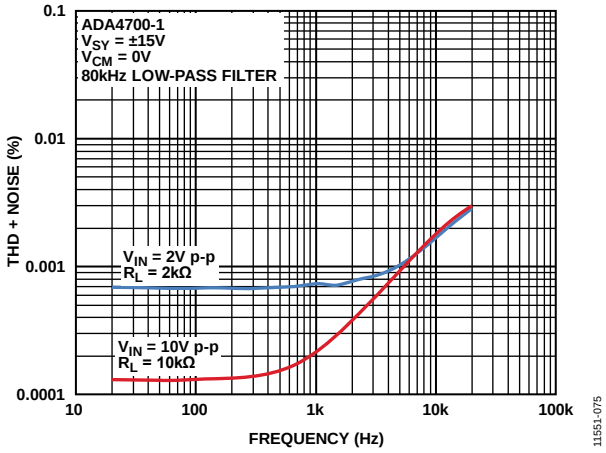

Figure 35. Total Harmonic Distortion + Noise (THD + Noise) vs. Frequency, V_{SY} = ±15 V

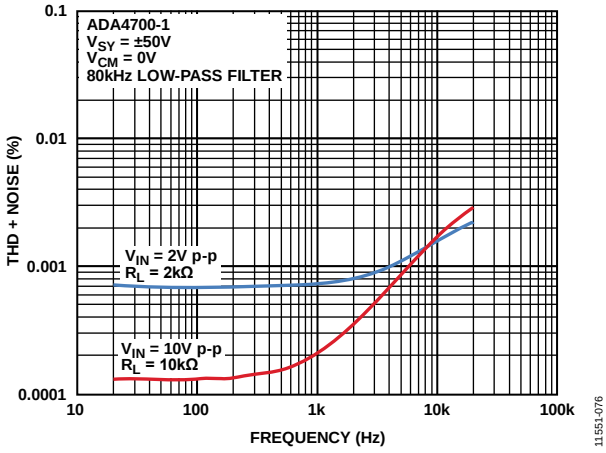

Figure 36. Total Harmonic Distortion + Noise (THD + Noise) vs. Frequency, V_{SY} = ±50 V

T_A = 25°C, unless otherwise noted.

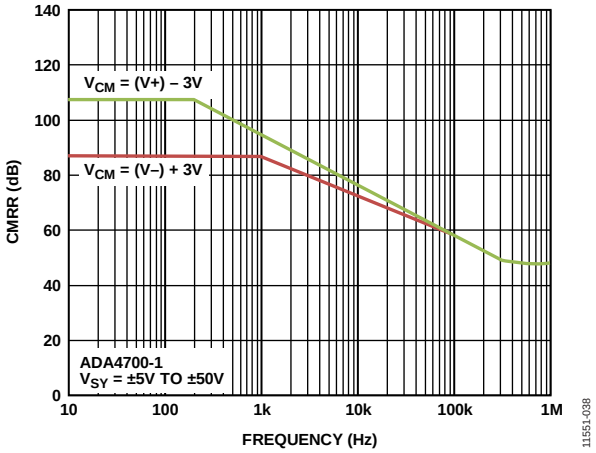

Figure 37. Common-Mode Rejection Ratio (CMRR) vs. Frequency, V_{SY} = ±5 V to ±50 V

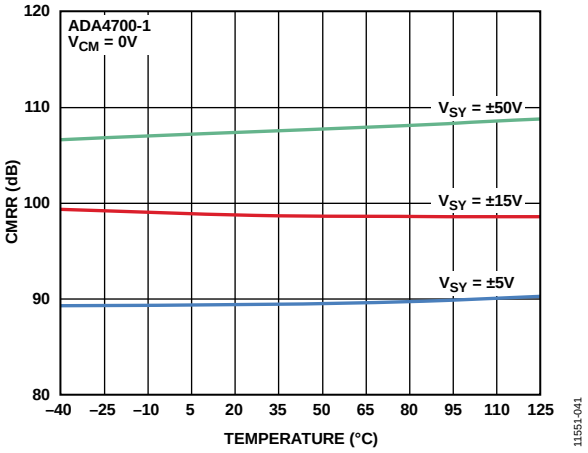

Figure 39. Common-Mode Rejection Ratio (CMRR) vs. Temperature for Various Supply Voltages

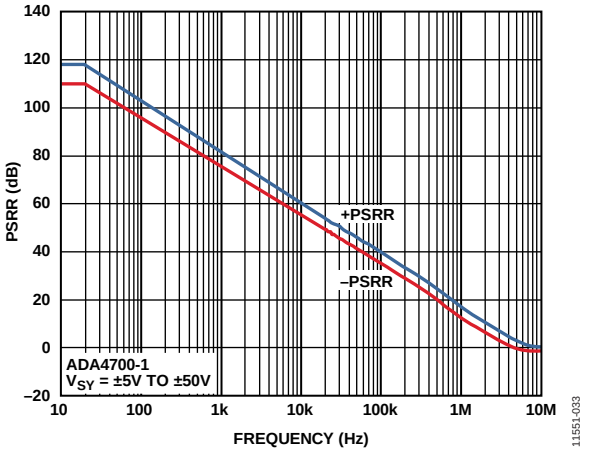

Figure 38. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{SY} = ±5 V to ±50 V

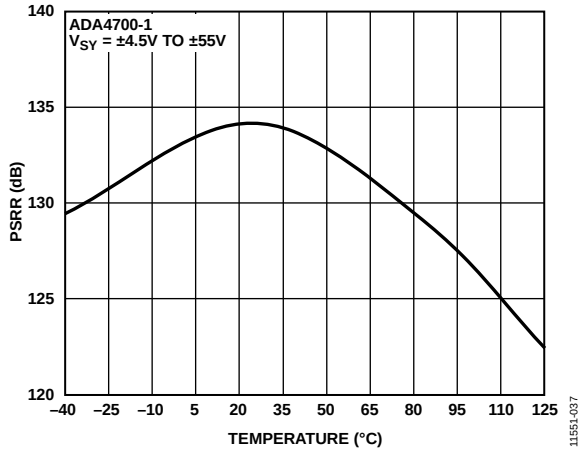

Figure 40. Power Supply Rejection Ratio (PSRR) vs. Temperature

T_A = 25°C, unless otherwise noted.

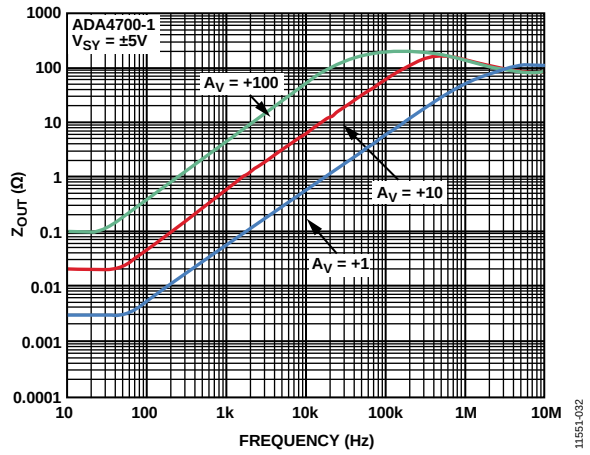

Figure 41. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±5 V

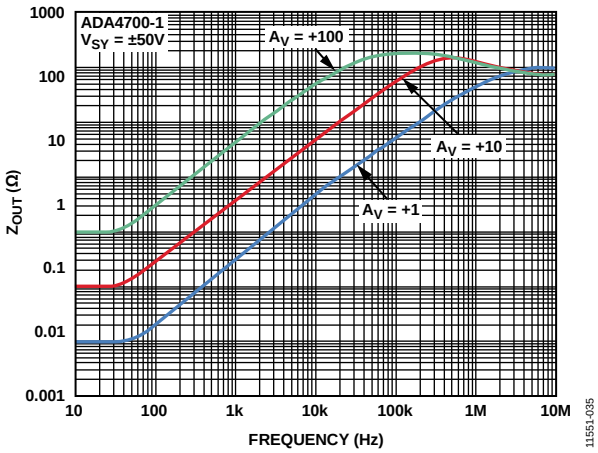

Figure 44. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±50 V

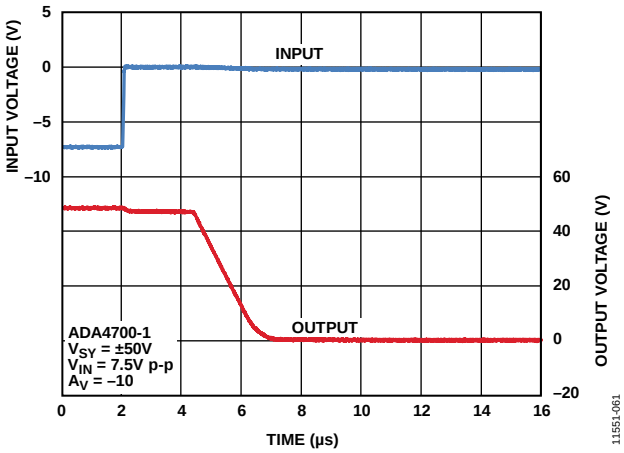

Figure 42. Positive Output Overload Recovery, V_{SY} = ±50 V

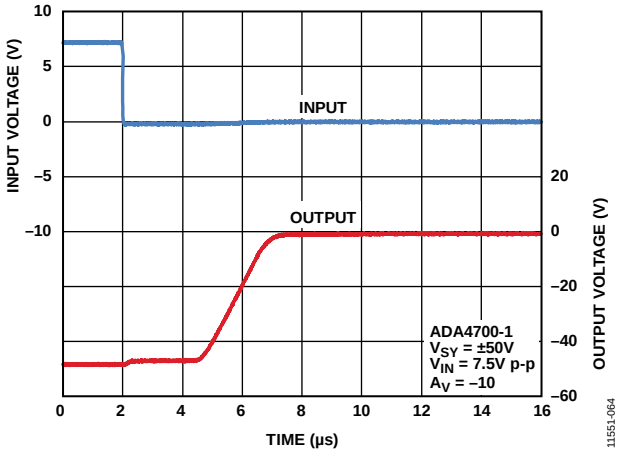

Figure 45. Negative Output Overload Recovery, V_{SY} = ±50 V

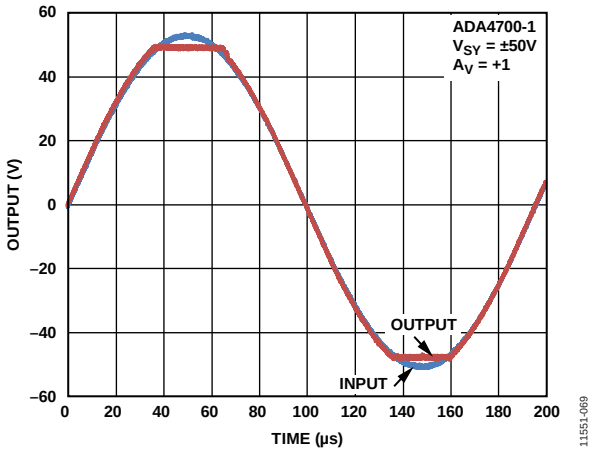

Figure 43. No Phase Reversal, V_{SY} = ±50 V

T_A = 25°C, unless otherwise noted.

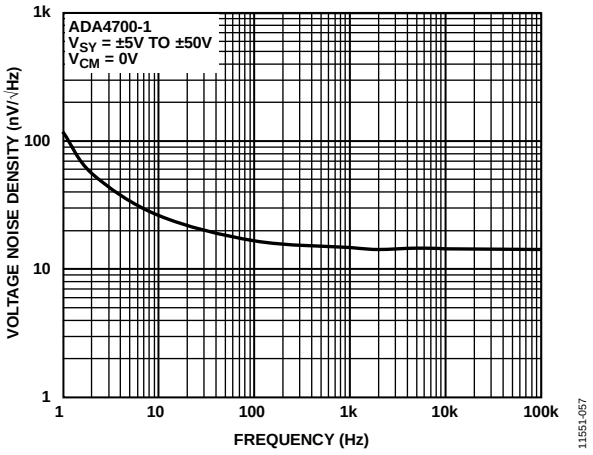

Figure 46. Input Voltage Noise Density vs. Frequency

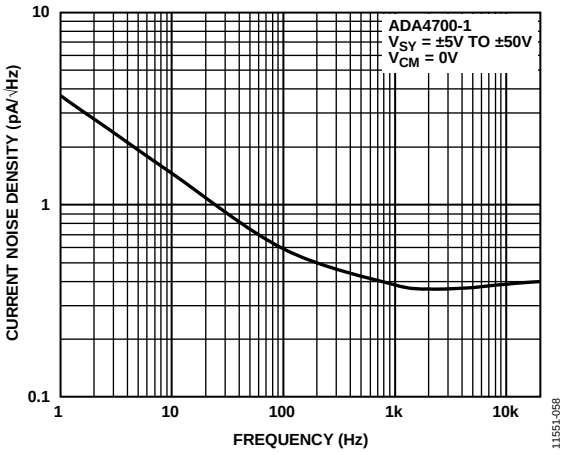

Figure 48. Input Current Noise Density vs. Frequency

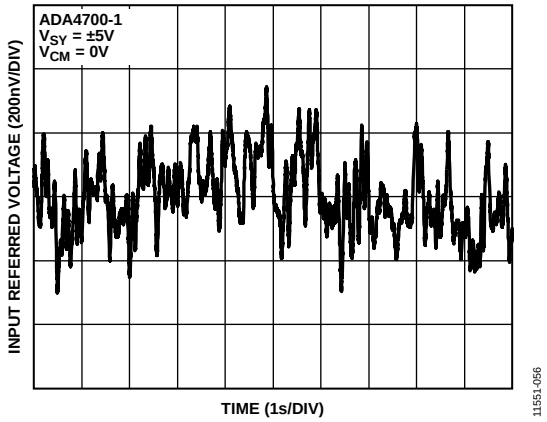

Figure 47. 0.1 Hz to 10 Hz Noise, V_{SY} = ±5 V

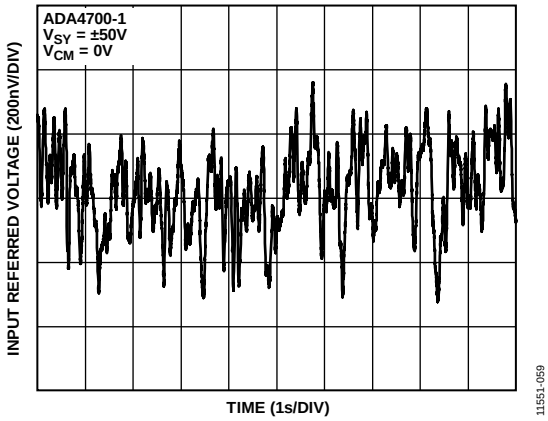

Figure 49. 0.1 Hz to 10 Hz Noise, V_{SY} = ±50 V

T_A = 25°C, unless otherwise noted.

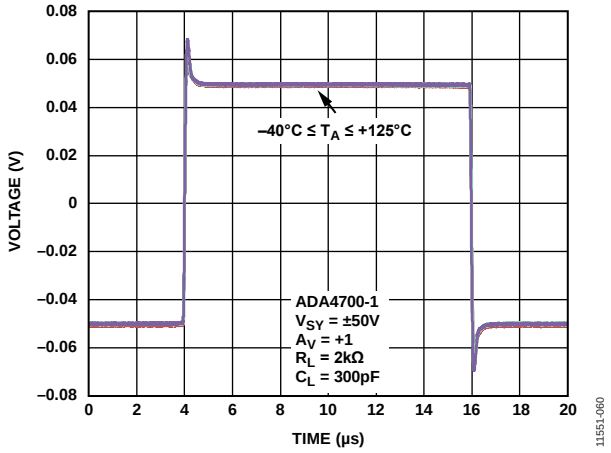

Figure 50. Small Signal Transient Response, V_{SY} = ±50 V

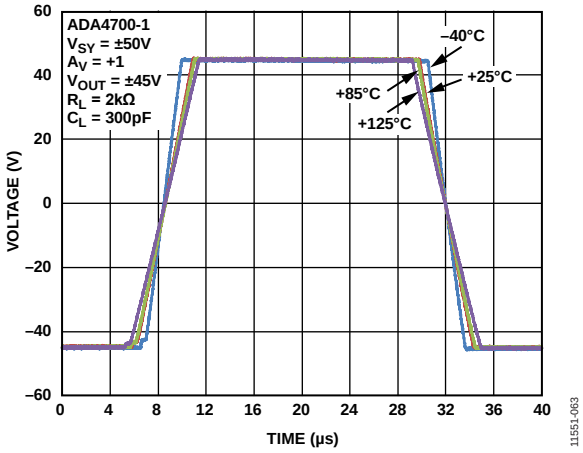

Figure 53. Large Signal Transient Response, V_{SY} = ±50 V

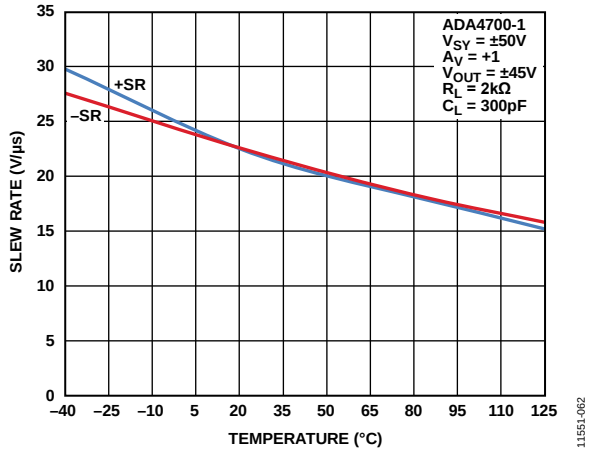

Figure 51. Slew Rate (SR) vs. Temperature, V_{SY} = ±50 V

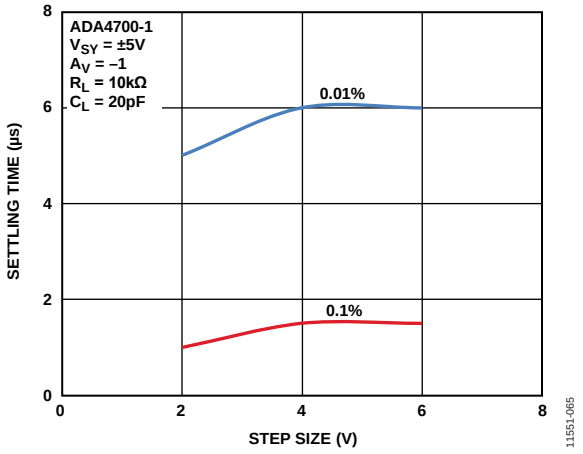

Figure 54. 0.01% and 0.1% Settling Time vs. Step Size, V_{SY} = ±5 V

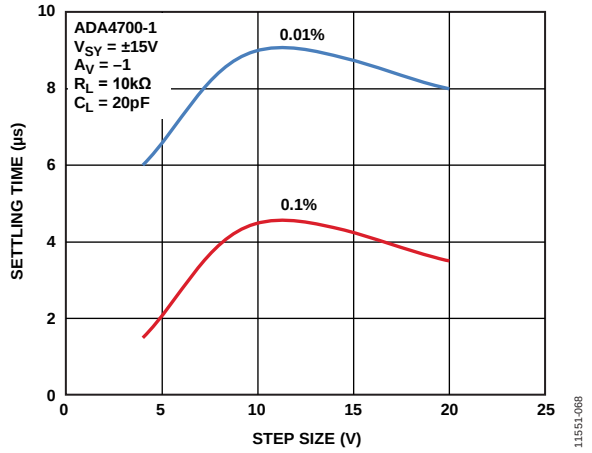

Figure 52. 0.01% and 0.1% Settling Time vs. Step Size, V_{SY} = ±15 V

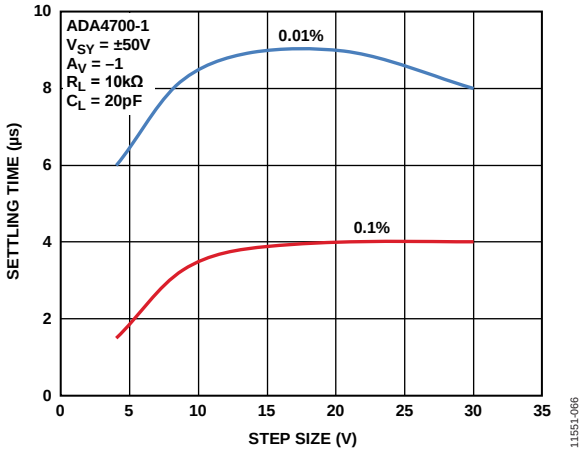

Figure 55. 0.01% and 0.1% Settling Time vs. Step Size, V_{SY} = ±50 V

TEST CIRCUITS

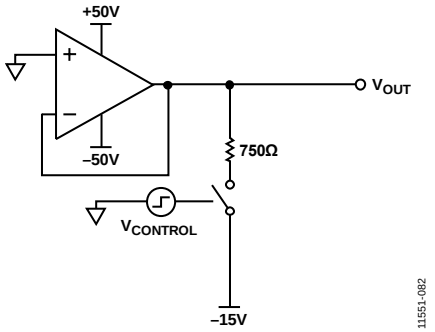

Figure 56. Test Circuit for Output Current Transient Settling Time (Sourcing) Shown in Figure 17

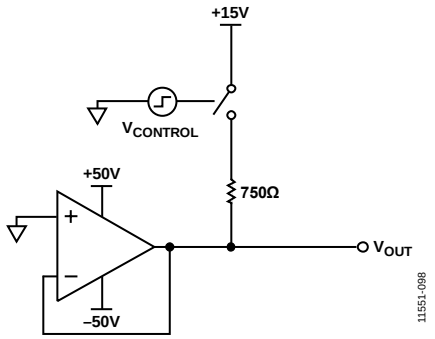

Figure 57. Test Circuit for Output Current Transient Settling Time (Sinking) Shown in Figure 20

THEORY OF OPERATION

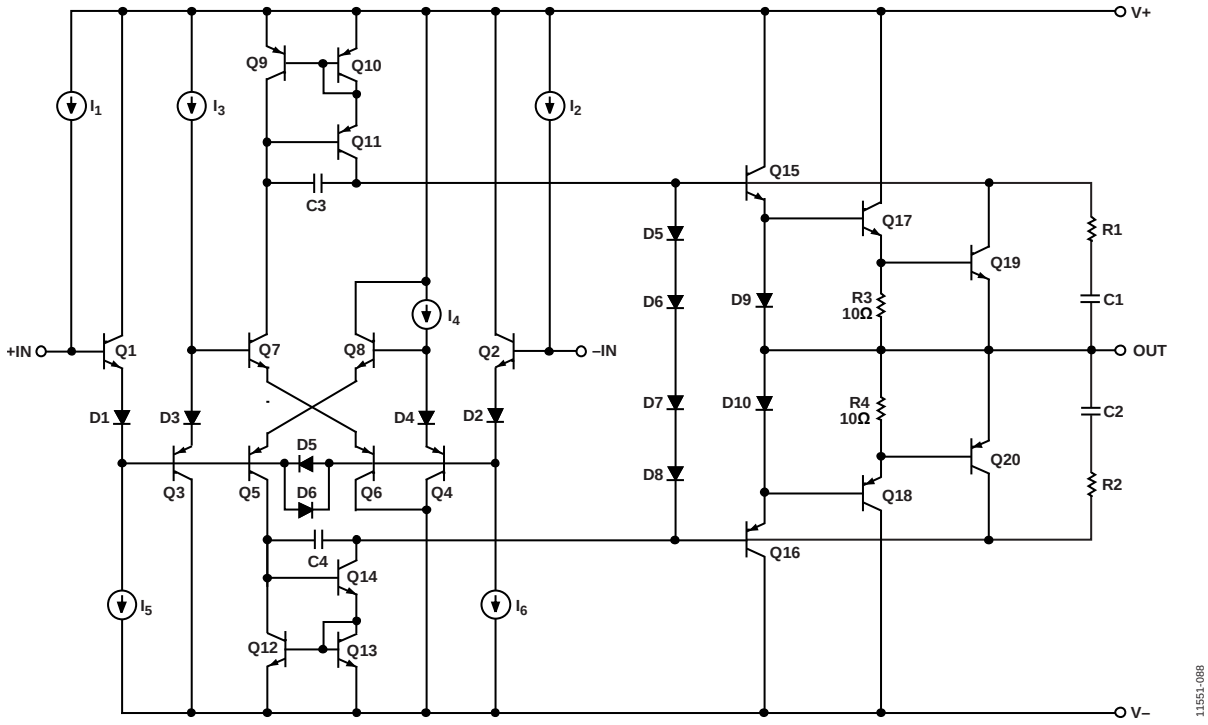

Figure 58. Simplified Schematic of the ADA4700-1

The ADA4700-1 is a high voltage operational amplifier featuring a slew enhanced bipolar input stage that provides all of the voltage gain. Single stage amplifiers are noted for their excellent stability but poor open-loop gain; however, the advanced ADA4700-1 design provides gain comparable to multistage amplifiers and, therefore, combines the advantages of both.

Referring to Figure 58, the input stage is formed by Q5 to Q8 loaded by the current mirrors, Q9 to Q14. The output stage is of the complementary Darlington type formed by Q15 to Q18. Like other bipolar amplifiers, the input stage is internally clamped to prevent degradation with large differential inputs; however, the addition of Q1 and Q2 in conjunction with the high voltage diodes, D1 and D2, maintain high differential input impedance even when the voltage between the inputs is equal to the supply voltage. This configuration makes the ADA4700-1 suitable for applications with unavoidable large differential voltages, such as rectifiers, peak detectors, and comparators.

The ADA4700-1 uses a single-pole compensation set by C3 and C4. The internal snubber networks, R1/C1 and R2/C2, further enhance the stability. This design enables large capacitive loads to be driven without the risk of oscillation.

The Q19 and Q20 transistors in conjunction with the R3 and R4 resistors provide output short-circuit protection. Additionally, a thermal regulating circuit (not shown in Figure 58) limits the die temperature to 145°C or greater to protect against excessive power dissipation.

With approximately equal split supplies up to ±50 V, the output can be shorted to ground unconditionally; however, operating this way is not recommended.

If the voltage between the output and either supply is more than 60 V, avoid a short circuit to the supply. Transient dissipation in the output transistors can exceed their safe operating area and cause subsequent destruction.

THERMAL REGULATION

The circuitry for thermal regulation of the ADA4700-1 is dependent on the ambient temperature and time duration of the current drive. When thermal regulation of the ADA4700-1 is active, the supply current, I_{SY}, reduces from 1.7 mA to 300 µA. The output stage remains biased during thermal regulation due to the parasitics of the output devices in conjunction with the elevated die temperature. For example, with a current drive, I_{OUT}, of 30 mA for 180 seconds and with an ambient temperature of 85°C, the thermal regulation is triggered at a junction temperature of 145°C with an output current level of 22 mA. For additional information, refer to the Thermal Management section and the Safe Operating Area section.

APPLICATIONS INFORMATION

THERMAL MANAGEMENT

Thermal management of high power amplifiers such as the ADA4700-1 is an essential consideration in system design. Two conditions affect junction temperature (T_J): power dissipation (P_D) of the device and ambient temperature (T_A) surrounding the package. This relationship is shown in Equation 1.

$$T_J = P_D \times \theta_{JA} + T_A \quad (1)$$

where θ_{JA} is the thermal resistance between the die and the ambient environment. Power dissipation is the sum of quiescent power of the device and the power required to drive a load. Power dissipation for the sourcing current is shown in Equation 2.

$$P_D = ((V+) - (V-)) \times I_{SY} + ((V+) - V_{OUT}) \times I_{OUT} \quad (2)$$

Replace ((V+) − V_{OUT}) in Equation 2 with ((V−) − V_{OUT}) when sinking current.

The specified thermal resistance of the ADA4700-1 is 45°C/W. Printed circuit board (PCB) layout and an external heat sink can improve thermal performance by reducing θ_{JA}.

To reduce the thermal resistance between the junction and ambient environment, the exposed pad of the ADA4700-1 can be soldered to the V− plane layer of the PCB, which acts as a heat sink. By using the PCB layout shown in Figure 60, θ_{JA} reduces to 26°C/W.

The ADA4700-1 guards the die from exceeding the absolute maximum temperature. When the die reaches a junction temperature greater than 145°C, thermal regulation is triggered, the supply current is reduced, and the output load current is limited.

SAFE OPERATING AREA

The safe operating area (SOA) of Figure 59 is the range of voltages, currents, and temperatures under which an amplifier can safely operate without failure. It is directly dependent on the ambient temperature and the thermal resistance. Figure 59 shows the SOA for the ADA4700-1 at steady state using the PCB shown in Figure 60. The duration of the 30 mA load driven is 180 seconds. Different time intervals produce alternate sets of curves. The guaranteed ambient temperature range of the ADA4700-1 is −40°C to +85°C. The 125°C shown in Figure 59 is for reference only. To maintain normal operation, the ADA4700-1 must remain in the SOA (area under each curve) up to an ambient temperature of 85°C.

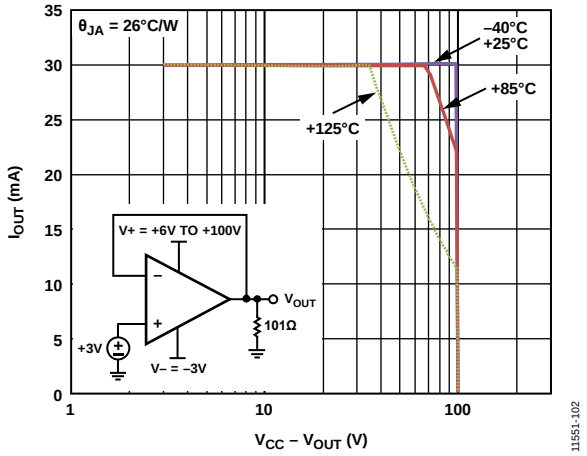

Figure 59. Safe Operating Area with θ_{JA} = 26°C/W

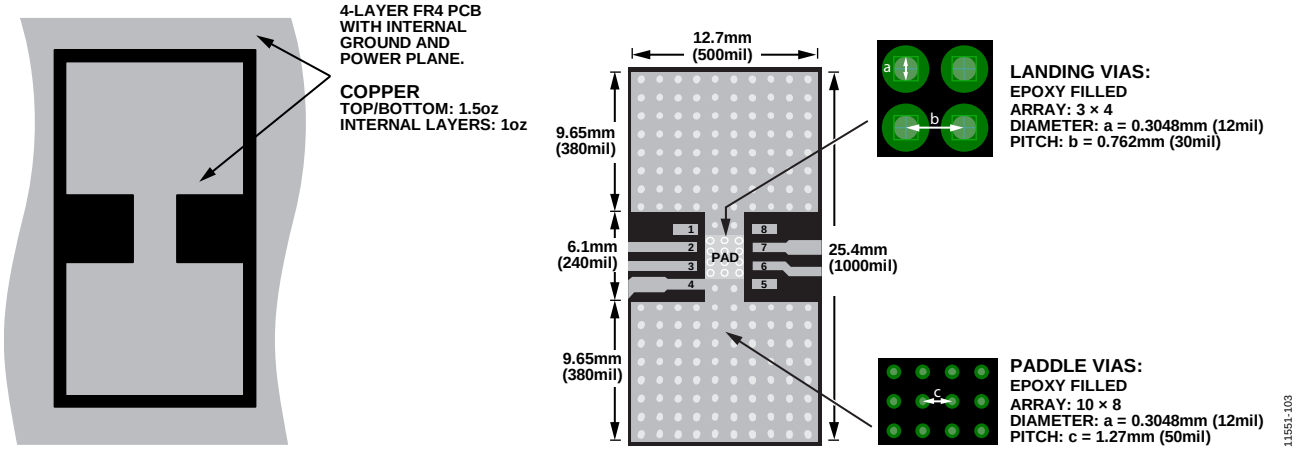

Figure 60. Thermal Landing and PCB Material Used to Obtain a θ_{JA} of 26°C/W

DRIVING CAPACITIVE LOADS

Although the ADA4700-1 behaves well when driving capacitive loads, C_L, as seen in Figure 27 to Figure 30, extra compensation can improve the response when large capacitances need to be accommodated. The simplest way of accomplishing this is with a snubber network, as shown in Figure 61.

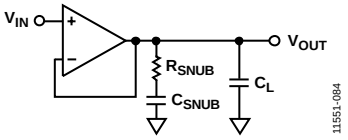

Figure 61. Snubber Network

For unity-gain applications and capacitive loads up to 1 nF, R_{SNUB} = 150 Ω and C_{SNUB} = 10 nF works well. Results for this circuit are shown in Figure 64. With higher closed-loop gains, lighter snubbing can be used. For capacitive loads up to 10 nF, the snubber must be larger. Figure 65 shows the results of using an R_{SNUB} = 22 Ω, C_{SNUB} = 100 nF, and C_L = 10 nF with the ADA4700-1 in a gain of 10. Because the snubber network places an ac load on the amplifier, snubbing does not work well when larger capacitive loads are used, or when large transients are present. A better approach is to use a bypass network in the feedback path, as shown in Figure 62.

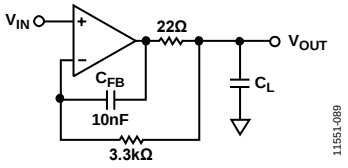

Figure 62. Unity-Gain Configuration with Bypass Network

The bypass network in Figure 62 performs well with loads up to 100 nF. The resulting waveforms are shown in Figure 66 for various output amplitudes. For heavier loads, capacitive feedback, C_{FB}, must be increased. The configuration in Figure 62 can be modified to work with gains greater than 1. Figure 63 shows a bypass network with a gain of 10 system, and results for various output amplitudes are shown in Figure 67.

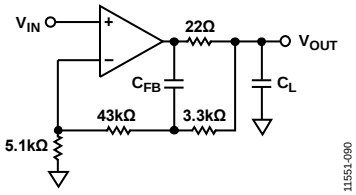

Figure 63. Bypass Network with Gain of 10 System

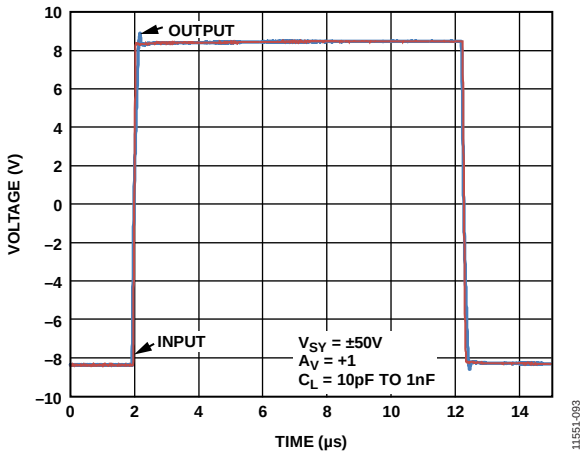

Figure 64. Results from Snubber Network with A_V = +1 and C_L = 10 pF to 1 nF

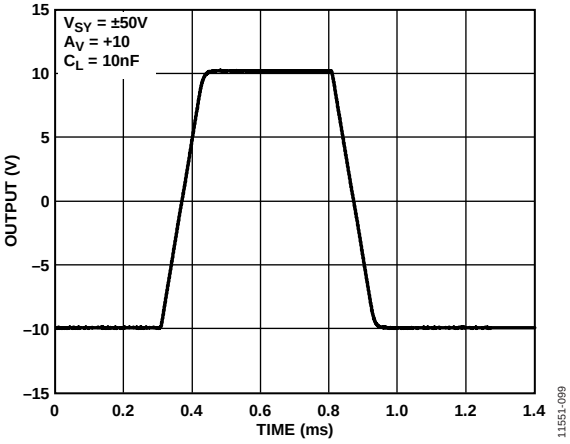

Figure 65. Results from Snubber Network with Higher Gains, C_L = 10 nF

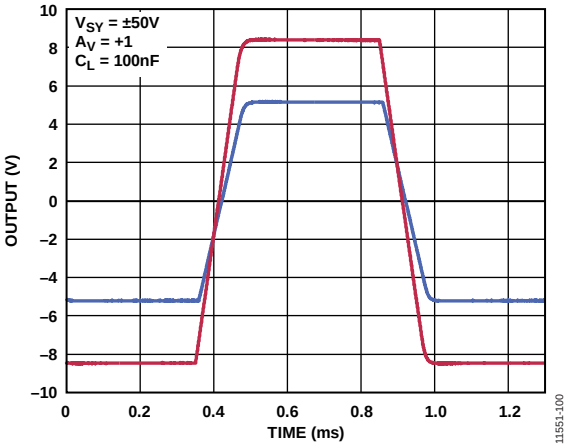

Figure 66. Results of Bypass Network for Various Output Amplitudes, Unity Gain with C_L = 100 nF

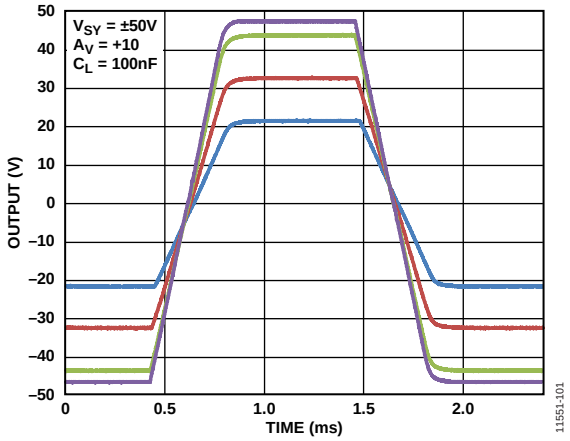

Figure 67. Result of Bypass Network with A_V = +10 and C_L = 100 nF

INCREASING CURRENT DRIVE

Extra output current can be obtained by adding external driver transistors. Crossover distortion is minimized by allowing the amplifier to drive the lower currents directly via the bypass resistor, as is shown in Figure 68. This circuit can provide a few hundred miliamps; however, keep the driver transistors within their safe operating area. For heavier loads (up to 5 A), power Darlingtons can be used, as is shown in Figure 69.

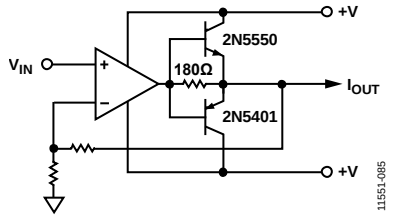

Figure 68. Increasing Current Drive Using Discrete Transistors

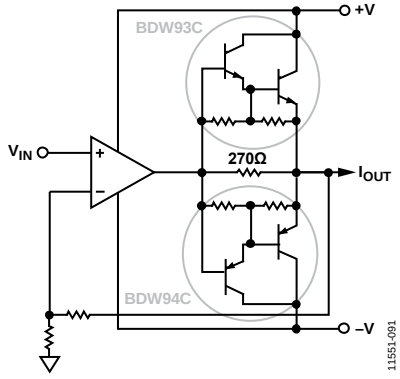

Figure 69. Bilateral Current Source with Transfer Function 1 mA/V

CONSTANT CURRENT APPLICATIONS

When a constant current with high compliance is needed, the ADA4700-1 can be used as a modified Howland current pump. The values shown in Figure 70 yield a transfer function of 1 mA/V. Applying this analysis to the modified Howland current pump in Figure 71 results in an output capability of 1 A/V.

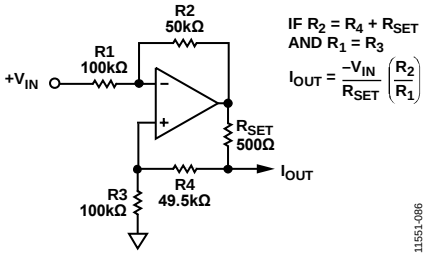

Figure 70. Transfer Function of 1 mA/V

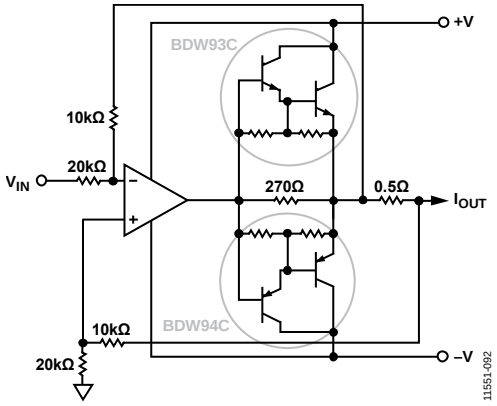

Figure 71. Modified Howland Current Pump

OUTLINE DIMENSIONS

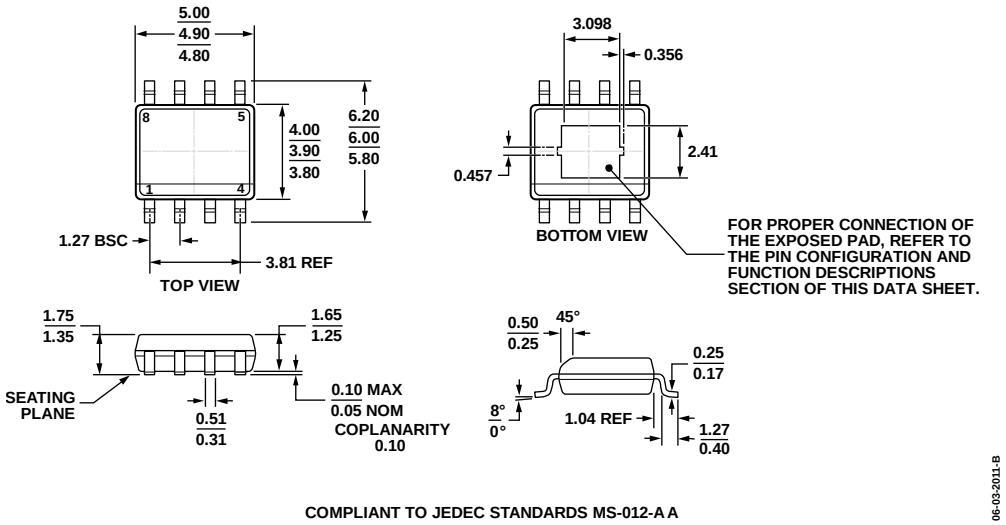

Figure 72. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4700-1ARDZ	−40°C to +85°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-2
ADA4700-1ARDZ-R7	−40°C to +85°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-2
ADA4700-1ARDZ-RL	−40°C to +85°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-2

[1] Z = RoHS Compliant Part.

NOTES

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NOTES

D11551-0-8/13(0)

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Analog Devices Inc.:

ADA4700-1ARDZ ADA4700-1ARDZ-RL ADA4700-1ARDZ-R7 EVALPRAHVOPAMP-1RZ