

Data Sheet

FEATURES

44 V supply maximum ratings V_{SS} to V_{DD} analog signal range Low on resistance (45 Ω max) Low ΔR_{ON} (5 Ω max) Low R_{ON} match (4 Ω max) Low power dissipation Fast switching times t_{ON} < 175 ns t_{OFF} < 145 ns Low leakage currents (5 nA max) Low charge injection (10 pC max) Break-before-make switching action

APPLICATIONS

Audio and video switching Battery-powered systems Test equipment Communication systems

GENERAL DESCRIPTION

The ADG333A is a monolithic complementary metal-oxide semiconductor (CMOS) device comprising four independently selectable single-pole, double-throw (SPDT) switches. It is designed on a linear compatible CMOS (LC²MOS) process, which provides low power dissipation yet achieves a high switching speed and a low on resistance.

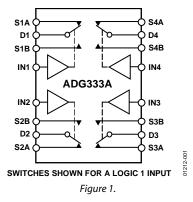
The on-resistance profile is very flat over the full analog input range, ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the device suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the device ideally suited for portable, battery-powered instruments.

When they are on, each switch conducts equally well in both directions and has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Low charge inject is inherent in the design.

Quad SPDT Switch

ADG333A

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

- Extended signal range. The ADG333A is fabricated on an enhanced LC²MOS process, giving an increased signal range which extends to the supply rails.
- 2. Low power dissipation.
- 3. Low Ron.
- 4. Single-supply operation. For applications in which the analog signal is unipolar, the ADG333A can be operated from a single rail power supply. The device is fully specified with a single 12 V supply.

Rev. B

Document Feedback

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REVISION HISTORY

6/2016—Rev. A to Rev. B

Changes to V _{DD} Parameter, Table 2	4
Updated Outline Dimensions	. 12
Changes to Ordering Guide	. 13

3/2005—Rev. 0 to Rev. A

Updated Format	Universal
Changes to Specifications Section	
Updated Outline Dimensions	
Changes to Ordering Guide	

10/1995—Revision 0: Initial Version

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SPECIFICATIONS

DUAL SUPPLY

 V_{DD} = +15 V, V_{SS} = -15 V, GND = 0 V, unless otherwise noted. 1

Table 1.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
Ron	20		Ωtyp	$V_D = \pm 10 \text{ V}, \text{ I}_S = -1 \text{ mA}$
	45	45	Ωmax	
ΔR_{ON}		5	Ωmax	$V_D = \pm 5 V$, $I_S = -10 mA$
Ron Match		4	Ωmax	$V_D = \pm 10 \text{ V}, \text{ I}_S = -10 \text{ mA}$
LEAKAGE CURRENTS				$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$
Source Off Leakage Is (OFF)	±0.1		nA typ	$V_D = \pm 15.5 \text{ V}, V_S = +15.5 \text{ V}$
	±0.25	±3	nA max	Figure 15
Channel On Leakage I _D , I _S (ON)	±0.1		nA typ	$V_{S} = V_{D} = \pm 15.5 V$
	±0.4	±5	nA max	Figure 16
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current				
IINL OR INH		±0.005	μA typ	$V_{IN} = 0 V \text{ or } V_{DD}$
		±0.5	μA max	
DYNAMIC CHARACTERISTICS ²				
ton	90		ns typ	$R_L{=}$ 300 $\Omega,$ C_L = 35 pF; V_S = ± 10 V; Figure 17
		175	ns max	
toff	80		ns typ	R_L = 300 Ω,C_L = 35 pF; V_S = ± 10 V; Figure 17
		145	ns max	
Break-Before-Make Delay, topen	10		ns min	R_L = 300 $\Omega,$ C_L = 35 pF; V_S = +5 V; Figure 18
Charge Injection	2		pC typ	$V_{D} = 0 V, R_{D} = 0 \Omega, C_{L} = 10 \text{ nF}; V_{DD} = +15 V, V_{SS} = -15 V;$ Figure 19
	10		pC max	
Off Isolation	72		dB typ	R_L = 75 $\Omega,$ C_L = 5 pF, f = 1 MHz; V_S = 2.3 V rms; Figure 20
Channel-to-Channel Crosstalk	85		dB typ	$R_L = 75 \ \Omega$, $C_L = 5 \ pF$, $f = 1 \ MHz$; $V_S = 2.3 \ V \ rms$; Figure 21
Cs (OFF)	7		pF typ	
C _D , C _S (ON)	26		pF typ	
POWER REQUIREMENTS				
l _{DD}	0.05		mA typ	Digital inputs = 0 V or 5 V
	0.25	0.35	mA max	
lss	0.01		μA typ	
	1	5	μA max	
V _{DD} /V _{ss}		±3/±20	V min/V max	$ V_{DD} = V_{SS} $

 1 Temperature range is as follows: B version: $-40^\circ C$ to $+85^\circ C.$ 2 Guaranteed by design; not subject to production test.

SINGLE SUPPLY

 V_{DD} = +12 V, V_{SS} = 0 V \pm 10%, GND = 0 V, unless otherwise noted. 1

Table 2.

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
Ron	35		Ωtyp	$V_D = 1 V, 10 V, I_S = -1 mA$
		75	Ωmax	
LEAKAGE CURRENTS				V _{DD} = 13.2 V
Source Off Leakage I _S (OFF)	±0.1		nA typ	$V_D = 12.2 \text{ V/1 V}, V_S = 1 \text{ V/12.2 V}$
	±0.25	±3	nA max	Figure 15
Channel On Leakage I _D , Is (ON)	±0.1		nA typ	$V_{S} = V_{D} = 12.2 \text{ V}/1 \text{ V}$
	±0.4	±5	nA max	Figure 16
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, VINL		0.8	V max	
Input Current				
IINL OF INH		±0.005	μA typ	$V_{IN} = 0 V \text{ or } V_{DD}$
		±0.5	μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}	110		ns typ	R_L = 300 Ω,C_L = 35 pF; V_S = 8 V; Figure 17
		200	ns max	
toff	100		ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$; $V_S = 8 V$; Figure 17
		180	ns max	
Break-Before-Make Delay, topen	10		ns min	$R_L = 300 \Omega$, $C_L = 35 pF$; $V_S = 5 V$; Figure 18
Charge Injection	5		pC typ	$V_D = 6 V$, $R_D = 0 W$, $C_L = 10 nF$; $V_{DD} = 12 V$, $V_{SS} = 0 V$; Figure 19
Off Isolation	72		dB typ	R_L = 75 $\Omega,$ C_L = 5 pF, f = 1 MHz; Vs = 1.15 V rms; Figure 20
Channel-to-Channel Crosstalk	85		dB typ	$R_L = 75 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; $V_S = 1.15 V rms$; Figure 21
Cs (OFF)	12		pF typ	
C _D , C _S (ON)	25		pF typ	
POWER REQUIREMENTS				$V_{DD} = 13.5 V$
lod	0.05		mA typ	Digital inputs = 0 V or 5 V
	0.25	0.35	mA max	
V _{DD}		3/30	V min/V max	

 1 Temperature range is as follows: B Version: -40° C to $+85^\circ$ C. 2 Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

 $T_A = 25^{\circ}C$ unless otherwise noted.

Table 3.

Parameter	Min
V _{DD} to V _{SS}	+44 V
V _{DD} to GND	–0.3 V to +30 V
V _{ss} to GND	+0.3 V to -30 V
Analog, Digital Inputs ¹	V _{SS} – 2 V to V _{DD} + 2 V or 20 mA, whichever occurs first
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Junction Temperature	150°C
θ _{JA} , Thermal Impedance	
PDIP Package	103°C/W
SOIC Package	74°C/W
SSOP Package	130°C/W
Lead Temperature, Soldering	
10 sec	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 4. Truth Table

Logic	Switch A	Switch B
0	Off	On
1	On	Off

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

¹ Overvoltage at IN, S, or D is clamped by internal diodes. Current should be limited to the maximum ratings given.

TERMINOLOGY

Ron

Ohmic resistance between D and S.

ΔR_{ON}

 $R_{\rm ON}$ variation due to a change in the analog input voltage with a constant load current.

 $R_{\rm ON}\,Match$ Difference between the $R_{\rm ON}$ of any two channels.

Is (OFF) Source leakage current with the switch off.

 \mathbf{I}_{D} (OFF) Drain leakage current with the switch off.

 $I_{\rm D},\,I_{\rm S}\left(ON\right)$ Channel leakage current with the switch on.

 $\mathbf{V}_{\mathrm{D}}\left(\mathbf{V}_{S}\right)$ Analog voltage on Terminal D and Terminal S.

Cs (OFF) Off switch source capacitance.

 C_D (OFF) Off switch drain capacitance.

C_D, C_s (ON) On switch capacitance. ton

Delay between applying the digital control input and the output switching on.

toff Delay between applying the digital control input and the output switching off.

tOPEN Break-before-make delay when switches are configured as a multiplexer.

 \mathbf{V}_{INL} Maximum input voltage for Logic 0.

V_{INH} Minimum input voltage for Logic 1.

I_{INL} (I_{INH}) Input current of the digital input.

Crosstalk

A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

ADG333A

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

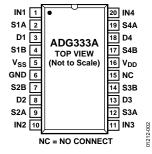
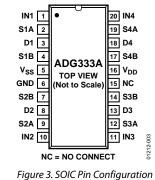


Figure 2. PDIP Pin Configuration



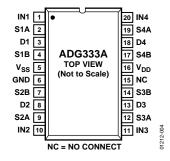
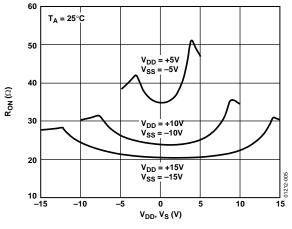


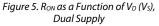
Figure 4. SSOP Pin Configuration

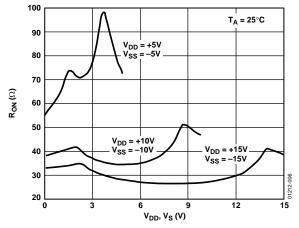
Table 5. Pin Function Descriptions

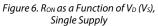
Pin No.	Mnemonic	Description
1, 10, 11, 20	IN1, IN2, IN3, IN4	Logic Control Input.
2, 4, 7, 9, 12, 14, 17, 19	S1A, S1B, S2B, S2A, S3A, S3B, S4B, S4A	Source Terminal. Can be an input or an output.
3, 8, 13, 18	D1, D2, D3, D4	Drain Terminal. Can be an input or an output.
5	V _{ss}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground.
6	GND	Ground (0 V) Reference.
15	NC	No Connect.
16	V _{DD}	Most Positive Power Supply Potential.

TYPICAL PERFORMANCE CHARACTERISTICS









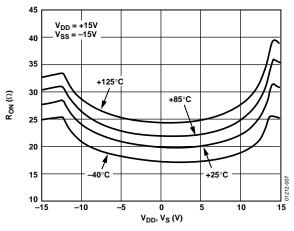


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures, Dual Supply

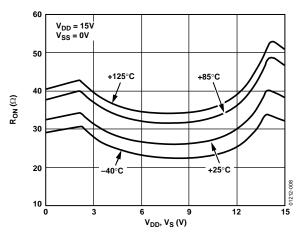


Figure 8. R_{ON} as a Function of V_D (Vs) for Different Temperatures, Single Supply

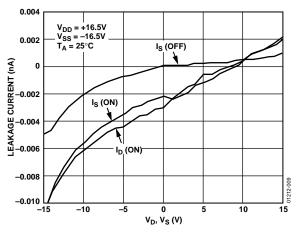


Figure 9. Leakage Currents as a Function of V_D (V_S), Dual Supply

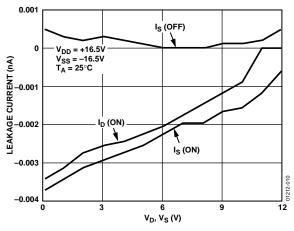


Figure 10. Leakage Currents as a Function of V_D (V_s), Single Supply

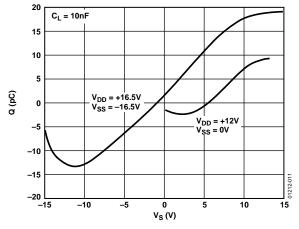


Figure 11. Charge Injection as a Function of V_{S}

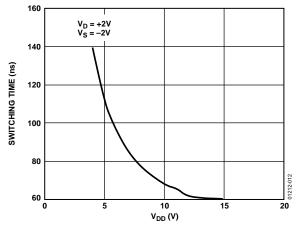


Figure 12. Switching Time as a Function of V_D

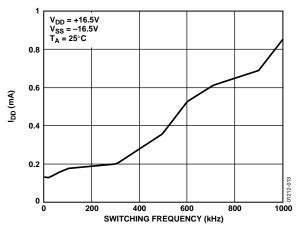
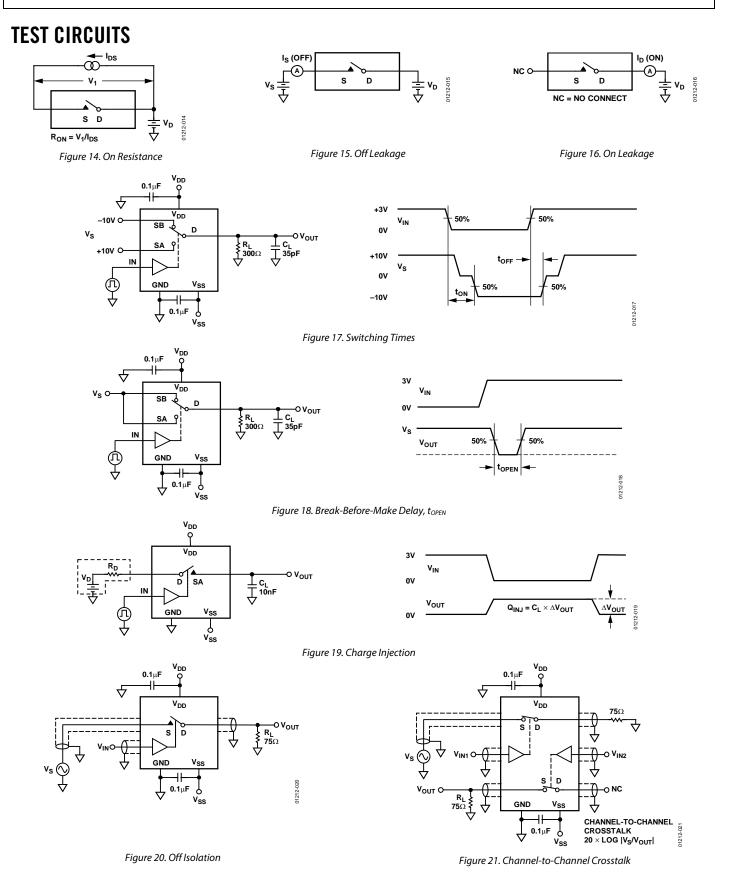


Figure 13. IDD as a Function of Switching Frequency

Data Sheet

ADG333A



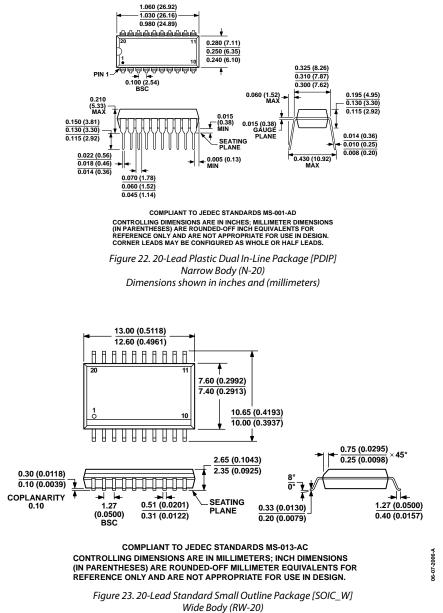
APPLICATIONS INFORMATION ADG333A SUPPLY VOLTAGES

The ADG333A can operate from a dual or signal supply. V_{SS} should be connected to GND when operating with a single supply. When using a dual supply, the ADG333A can also operate with unbalanced supplies; for example V_{DD} = 20 V and V_{SS} = -5 V. The only restrictions are that V_{DD} to GND must not exceed 30 V, V_{SS} to GND must not drop below -30 V, and V_{DD} to V_{SS} must not exceed +44 V. It is important to remember that the ADG333A supply voltage directly affects the input signal range, the switch on resistance and the switching times of the device. The effects of the power supplies on these characteristics can be clearly seen from the Typical Performance Characteristics curves.

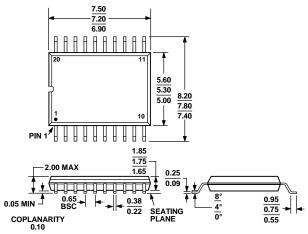
POWER SUPPLY SEQUENCING

When using CMOS devices, care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond those listed in the Absolute Maximum Ratings. This is also true for the ADG333A. Always turn on V_{DD} first, followed by V_{SS} and the logic signals. An external signal within the maximum specified ratings can then be safely presented to the source or drain of the switch.

OUTLINE DIMENSIONS



Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-150AE

Figure 24. 20-Lead Shrink Small Outline Package [SSOP] (RS-20) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹ Temperature Range		Package Description	Package Option
ADG333ABNZ	-40°C to +85°C	20-Lead Plastic Dual In-Line Package [PDIP]	N-20
ADG333ABR	-40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADG333ABR-REEL	-40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADG333ABRZ	-40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADG333ABRZ-REEL	-40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADG333ABRS	-40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG333ABRS-REEL	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG333ABRSZ	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG333ABRSZ-REEL	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20

¹ Z = RoHS Compliant Part.



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