

# ACPL-P347 and ACPL-W347

## 1.0 Amp Output Current SiC/GaN MOSFET and IGBT Gate Drive Optocoupler in Stretched S06

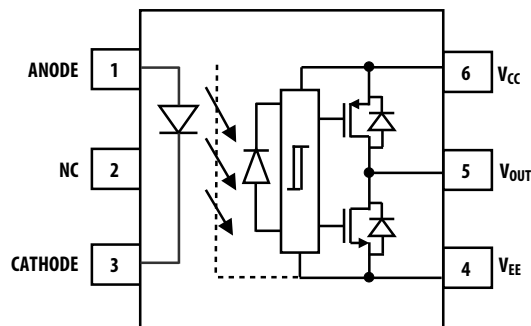


### Data Sheet

#### Description

The ACPL-P347/W347 contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving SiC/GaN (Silicon Carbide / Gallium Nitride) MOSFETs and IGBTs used in power conversion applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving SiC/GaN MOSFET and IGBT with ratings up to 1200V/50A.

#### Functional Diagram



Note: Design Note: A 1  $\mu$ F bypass capacitor must be connected between pins  $V_{CC}$  and  $V_{EE}$ .

#### Truth Table

LED	VCC – VEE "POSITIVE GOING" (i.e., TURN-ON)	VCC – VEE "NEGATIVE GOING" (i.e., TURN-OFF)	VO
OFF	0 – 30 V	30 – 0 V	LOW
ON	0 – 12.1 V	11.1 – 0 V	LOW
ON	12.1 – 13.9 V	12.9 – 11.1 V	TRANSITION
ON	13.9 – 30V	30 – 12.9 V	HIGH

#### Features

- 1.0 A maximum peak output current
- Wide operating  $V_{CC}$  range: 15 to 30 V
- 110 ns maximum propagation delay
- 50 ns maximum propagation delay difference
- Rail-to-rail output voltage
- 50 kV/ $\mu$ s minimum Common Mode Rejection (CMR) at  $V_{CM} = 1500$  V
- LED current input with hysteresis
- $I_{CC} = 4.2$  mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Industrial temperature range:  $-40$  °C to  $105$  °C
- Safety Approval
  - UL Recognized 3750/5000  $V_{RMS}$  for 1 min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5  $V_{IORM} = 891/1140$   $V_{PEAK}$

#### Applications

- SiC/GaN MOSFET and IGBT gate drive
- Motor drives
- Industrial Inverters
- Renewable energy inverters
- Switching power supplies

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments

## Ordering Information

ACPL-P347 is UL Recognized with 3750 V<sub>RMS</sub> for 1 minute per UL1577. ACPL-W347 is UL Recognized with 5000 V<sub>RMS</sub> for 1 minute per UL1577.

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Part numb	Option	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity	
	RoHS Compliant						
ACPL-P347	-000E	Stretched SO-6	X			100 per tube	
ACPL-W347	-500E		X	X		1000 per reel	
	-060E		X			X	100 per tube
	-560E		X	X	X	X	1000 per reel

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To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P347-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

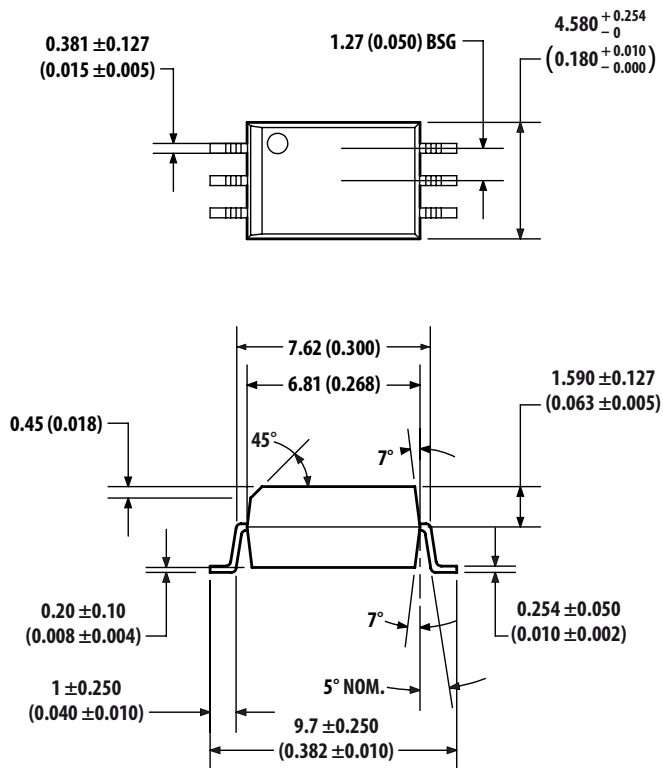
Example 2:

ACPL-W347-000E to order product of Stretched SO-6 Surface Mount package in Tube packaging and RoHS compliant.

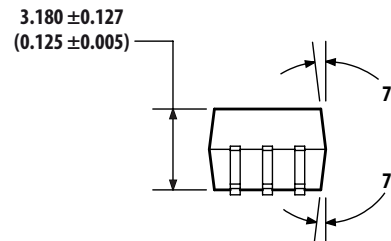
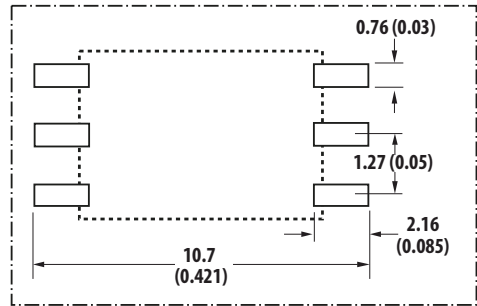
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings

### ACPL-P347 Stretched SO-6 Package (7 mm clearance)

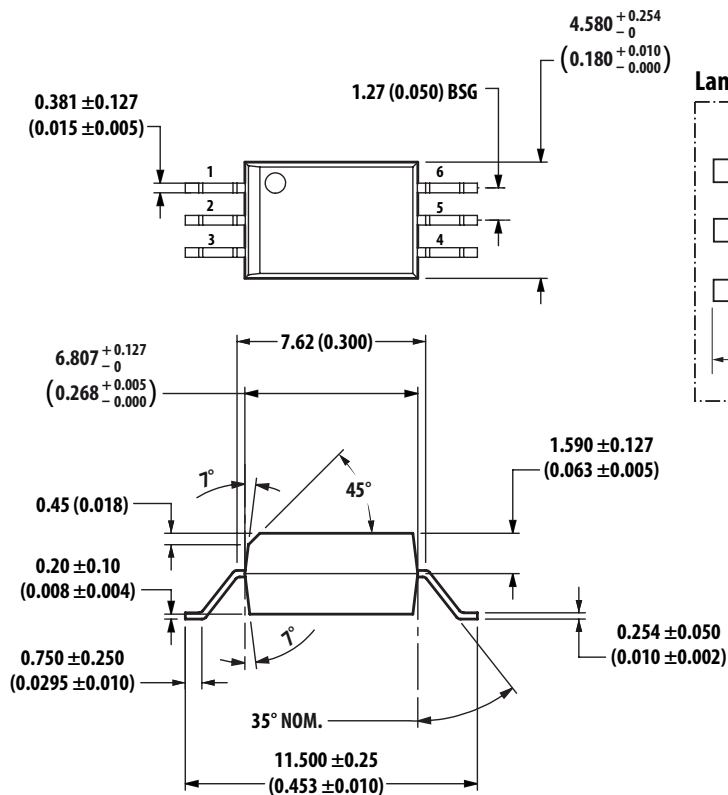


### Land Pattern Recommendation

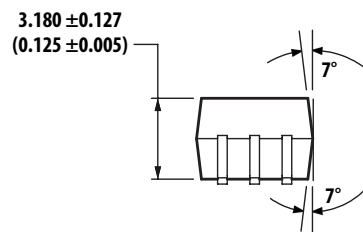
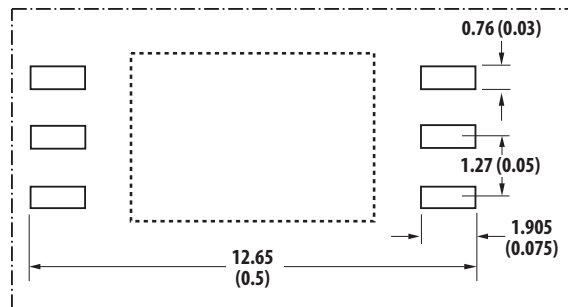


Floating Lead Protrusions max. 0.25 (0.01)  
 Dimensions in Millimeters (Inches)  
 Lead Coplanarity = 0.1 mm (0.004 Inches)

### ACPL-W347 Stretched SO-6 Package (8 mm clearance)



### Land Pattern Recommendation



Floating Lead Protrusions max. 0.25 (0.01)  
 Dimensions in Millimeters (Inches)  
 Lead Coplanarity = 0.1 mm (0.004 Inches)

## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

## Regulatory Information

The ACPL-P347/W347 is approved by the following organizations:

<b>UL</b>	Recognized under UL 1577, component recognition program up to $V_{ISO} = 3750 V_{RMS}$ (ACPL-P347) and $V_{ISO} = 5000 V_{RMS}$ (ACPL-W347).
<b>CSA</b>	CSA Component Acceptance Notice #5, File CA 88324
<b>IEC/EN/DIN EN 60747-5-5 (Option 060 Only)</b>	Maximum Working Insulation Voltage $V_{IORM} = 891 V_{peak}$ (ACPL-P347) and $V_{IORM} = 1140 V_{peak}$ (ACPL-W347)

**Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics\* (Option 060)**

Description	Symbol	ACPL-P347 Option 060	ACPL-W347 Option 060	Unit
Installation classification per DIN VDE 0110/39, Table 1				
for rated mains voltage $\leq 150 V_{rms}$		I – IV	I – IV	
for rated mains voltage $\leq 300 V_{rms}$		I – IV	I – IV	
for rated mains voltage $\leq 450 V_{rms}$		I – III	I – IV	
for rated mains voltage $\leq 600 V_{rms}$		I – III	I – IV	
for rated mains voltage $\leq 1000 V_{rms}$			I – III	
Climatic Classification		40/105/21	40/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	$V_{IORM}$	891	1140	$V_{PEAK}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1671	2137	$V_{PEAK}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1426	1824	$V_{PEAK}$
Highest Allowable Overvoltage* (Transient Overvoltage $t_{ini} = 60$ sec)	$V_{IOTM}$	6000	8000	$V_{PEAK}$
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	$T_S$	175	175	$^{\circ}C$
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at $T_S, V_{IO} = 500$ V	RS	$>10^9$	$>10^9$	$\Omega$

\* Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Avago Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

Note: These optocouplers are suitable for “safe electrical isolation” only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

**Table 2. Insulation and Safety Related Specifications**

Parameter	Symbol	ACPL-P347	ACPL-W347	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

**Notes:**

1. All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	$T_S$	-55	125	°C	
Operating Temperature	$T_A$	-40	105	°C	
Output IC Junction Temperature	$T_J$		125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 $\mu$ s pulse width, 300pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	$V_R$		5	V	
“High” Peak Output Current	$I_{OH(PEAK)}$		1.0	A	2
“Low” Peak Output Current	$I_{OL(PEAK)}$		1.0	A	2
Total Output Supply Voltage	$(V_{CC} - V_{EE})$	0	35	V	
Output Voltage	$V_{O(PEAK)}$	-0.5	$V_{CC}$	V	
Output IC Power Dissipation	$P_O$		500	mW	3
Total Power Dissipation	$P_T$		550	mW	4

**Table 4. Recommended Operating Conditions**

Parameter	Symbol	Min	Max.	Units	Note
Operating Temperature	$T_A$	- 40	105	°C	
Output Supply Voltage	$(V_{CC} - V_{EE})$	15	30	V	
Input Current (ON)	$I_{F(ON)}$	7	11	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	

**Table 5. Electrical Specifications (DC)**

All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 15\text{ V}$ ,  $V_{EE} = \text{Ground}$ . All minimum and maximum specifications are at recommended operating conditions ( $T_A = -40\text{ to }105\text{ }^\circ\text{C}$ ,  $I_{F(\text{ON})} = 7\text{ to }11\text{ mA}$ ,  $V_{F(\text{OFF})} = -3.6\text{ to }0.8\text{ V}$ ,  $V_{EE} = \text{Ground}$ ,  $V_{CC} = 15\text{ to }30\text{ V}$ ), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Peak Output Current	$I_{OH}$	-0.8			A	$V_{CC} - V_O = 15\text{ V}$		5
Low Level Peak Output Current	$I_{OL}$	0.8			A	$V_O - V_{EE} = 15\text{ V}$		5
High Level Output Voltage	$V_{OH}$	$V_{CC} - 0.4$	$V_{CC} - 0.2$		V	$I_O = -100\text{ mA}$ , $I_F = 9\text{ mA}$	1	6, 7
High Level Output Voltage	$V_{OH}$		$V_{CC}$		V	$I_O = 0\text{ mA}$ , $I_F = 9\text{ mA}$	1	
Low Level Output Voltage	$V_{OL}$		0.1	0.25	V	$I_O = 100\text{ mA}$	2	
High Level Supply Current	$I_{CCH}$		2.6	4.2	mA	$I_F = 9\text{ mA}$	3, 4	
Low Level Supply Current	$I_{CCL}$		2.6	4.2	mA	$V_F = 0\text{ V}$		
Threshold Input Current Low to High	$I_{FLH}$	0.4	1.3	4.0	mA	$V_O > 5\text{ V}$	5, 6	
Threshold Input Voltage High to Low	$V_{FHL}$	0.8			V			
Input Forward Voltage	$V_F$	1.2	1.55	1.95	V	$I_F = 9\text{ mA}$	13	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F / \Delta T_A$		-1.7		mV/ $^\circ\text{C}$			
Input Reverse Breakdown Voltage	$BV_R$	5			V	$I_R = 100\text{ }\mu\text{A}$		
Input Capacitance	$C_{IN}$		70		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$		
UVLO Threshold	$V_{UVLO+}$	12.1	13	13.9	V	$V_O > 5\text{ V}$ , $I_F = 9\text{ mA}$		
	$V_{UVLO-}$	11.1	12	12.9				
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0		V			

**Table 6. Switching Specifications (AC)**

All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 15\text{ V}$ ,  $V_{EE} = \text{Ground}$ . All minimum and maximum specifications are at recommended operating conditions ( $T_A = -40\text{ to }105\text{ }^\circ\text{C}$ ,  $I_{F(ON)} = 7\text{ to }11\text{ mA}$ ,  $V_{F(OFF)} = -3.6\text{ to }0.8\text{ V}$ ,  $V_{EE} = \text{Ground}$ ,  $V_{CC} = 15\text{ to }30\text{ V}$ ), unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	$t_{PLH}$	30	55	110	ns	$R_g = 15\ \Omega$ , $C_g = 10\text{ nF}$ , $f = 20\text{ kHz}$ , Duty Cycle = 50%, $V_{CC} = 15\text{ V}$	7, 8, 9, 10, 11	
Propagation Delay Time to Low Output Level	$t_{PHL}$	30	55	110	ns			
Pulse Width Distortion	PWD		0	40	ns			
Propagation Delay Difference Between Any Two Parts	PDD ( $t_{PHL} - t_{PLH}$ )	-50		50	ns		16, 17	9
Propagation Delay Skew	$t_{PSK}$			50	ns			10
Rise Time	$t_R$		8	28	ns	$C_g = 1\text{ nF}$ , $f = 20\text{ kHz}$ , Duty Cycle = 50%, $V_{CC} = 15\text{ V}$		
Fall Time	$t_F$		8	28	ns			
Output High Level Common Mode Transient Immunity	$ CM_H $	50	70		kV/ $\mu\text{s}$	$T_A = 25\text{ }^\circ\text{C}$ , $I_F = 9\text{ mA}$ , $V_{CC} = 30\text{ V}$ , $V_{CM} = 1500\text{ V}$ with split resistors	13	11, 12
Output Low Level Common Mode Transient Immunity	$ CM_L $	50	70		kV/ $\mu\text{s}$	$T_A = 25\text{ }^\circ\text{C}$ , $V_F = 0\text{ V}$ , $V_{CC} = 30\text{ V}$ , $V_{CM} = 1500\text{ V}$ with split resistors		11, 13

**Table 7. Package Characteristics**

All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ . All minimum/maximum specifications are at recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	$V_{ISO}$	ACPL-P347	3750			$V_{RMS}$	$RH < 50\%$ , $t = 1\text{ min.}$ , $T_A = 25\text{ }^\circ\text{C}$		14, 16
		ACPL-W347	5000			$V_{RMS}$	$RH < 50\%$ , $t = 1\text{ min.}$ , $T_A = 25\text{ }^\circ\text{C}$		15, 16
Input-Output Resistance	$R_{I-O}$			$>10^{14}$		$\Omega$	$V_{I-O} = 500\text{ V}_{DC}$		16
Input-Output Capacitance	$C_{I-O}$			0.6		pF	$f = 1\text{ MHz}$		
LED-to-Ambient Thermal Resistance	$R_{11}$			135		$^\circ\text{C/W}$			17
LED-to-Detector Thermal Resistance	$R_{12}$			27					
Detector-to-LED Thermal Resistance	$R_{21}$			39					
Detector-to-Ambient Thermal Resistance	$R_{22}$			47					

\* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 85 °C free-air temperature at a rate of 0.3 mA/ °C.
2. Maximum pulse width = 10 μs. This value is intended to allow for component tolerances for designs with IO peak minimum = 1.0 A. See applications section for additional details on limiting I<sub>OH</sub> peak.
3. Derate linearly above 85 °C free-air temperature at a rate of 12.5 mW/ °C .
4. Derate linearly above 85 °C free-air temperature at a rate of 13.75 mW/ °C . The maximum LED junction temperature should not exceed 125 °C.
5. Maximum pulse width = 10 μs.
6. In this test V<sub>OH</sub> is measured with a dc load current. When driving capacitive loads, V<sub>OH</sub> will approach V<sub>CC</sub> as I<sub>OH</sub> approaches zero amps.
7. Maximum pulse width = 1 ms.
8. Pulse Width Distortion (PWD) is defined as |t<sub>PHL</sub>-t<sub>PLH</sub>| for any given device.
9. Propagation Delay Difference (PDD) is the difference between t<sub>PHL</sub> and t<sub>PLH</sub> between any two units under the same test condition.
10. Propagation Delay Skew (t<sub>PSK</sub>) is the difference in t<sub>PHL</sub> or t<sub>PLH</sub> between any two units under the same test condition.
11. Pin 2 needs to be connected to LED common. Split resistor network in the ratio 1.5:1 with 232 Ω at the anode and 154 Ω at the cathode.
12. Common mode transient immunity in the high state is the maximum tolerable dV<sub>CM</sub>/dt of the common mode pulse, V<sub>CM</sub>, to assure that the output will remain in the high state (i.e., V<sub>O</sub> > 15.0 V).
13. Common mode transient immunity in a low state is the maximum tolerable dV<sub>CM</sub>/dt of the common mode pulse, V<sub>CM</sub>, to assure that the output will remain in a low state (i.e., V<sub>O</sub> < 1.0 V).
14. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V<sub>RMS</sub> for 1 second (leakage detection current limit, I<sub>L-O</sub> ≤ 5 μA).
15. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥6000 V<sub>RMS</sub> for 1 second (leakage detection current limit I<sub>L-O</sub> ≤ 5 μA).
16. Device considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5 and 6 shorted together.
17. The device was mounted on a high conductivity test board as per JEDEC 51-7.



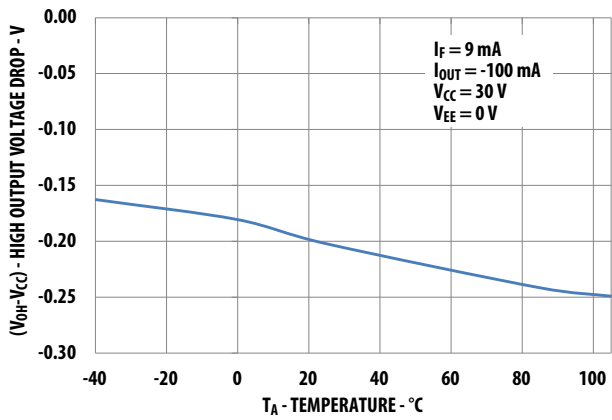


Figure 1.  $V_{OH}$  vs. temperature

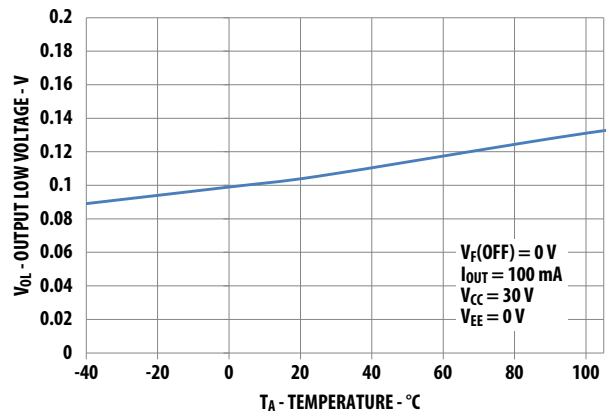


Figure 2.  $V_{OL}$  vs. Temperature

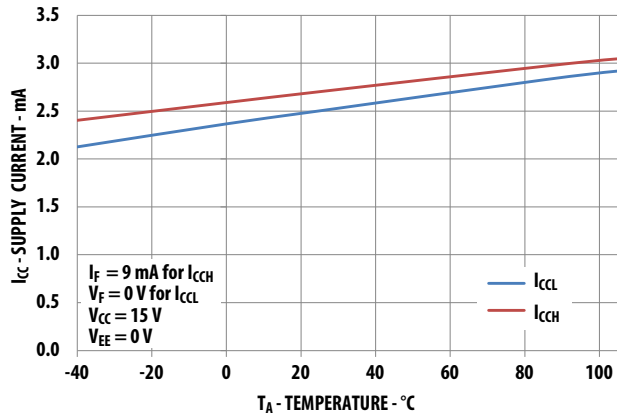


Figure 3.  $I_{CC}$  vs. temperature

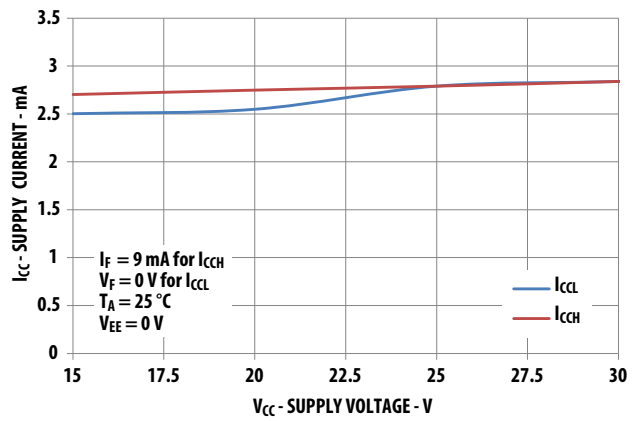


Figure 4.  $I_{CC}$  vs.  $V_{CC}$

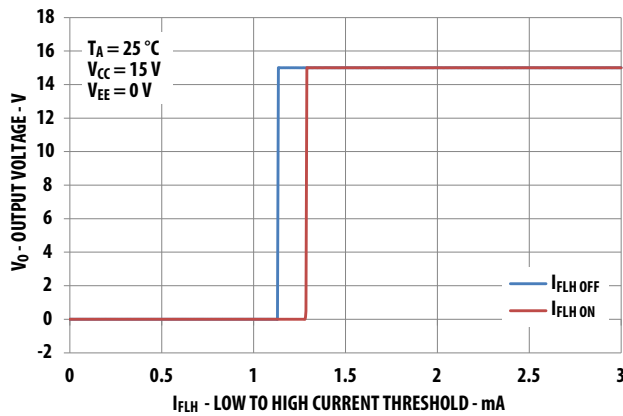


Figure 5.  $I_{FLH}$  hysteresis

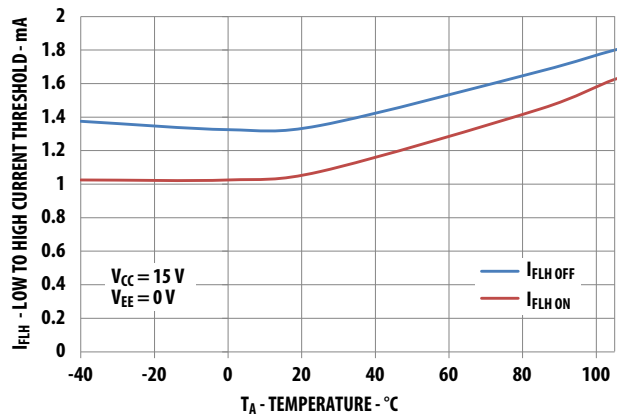


Figure 6.  $I_{FLH}$  vs. temperature

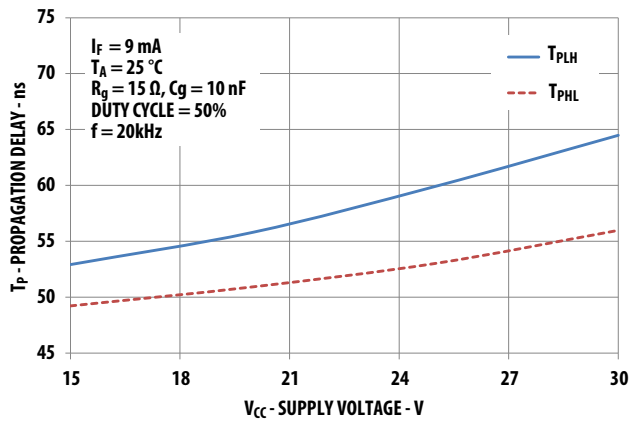


Figure 7. Propagation delay vs.  $V_{CC}$

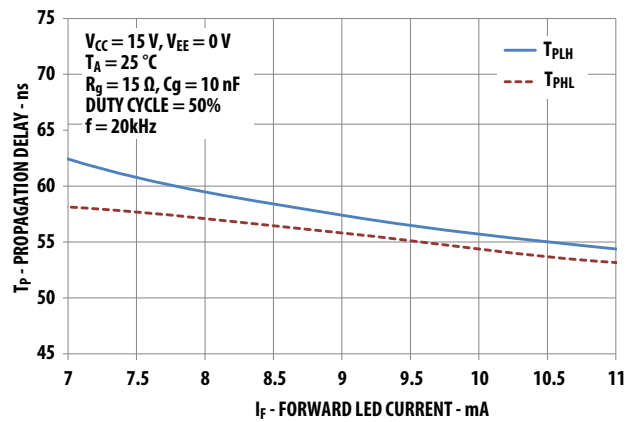


Figure 8. Propagation delay vs.  $I_F$

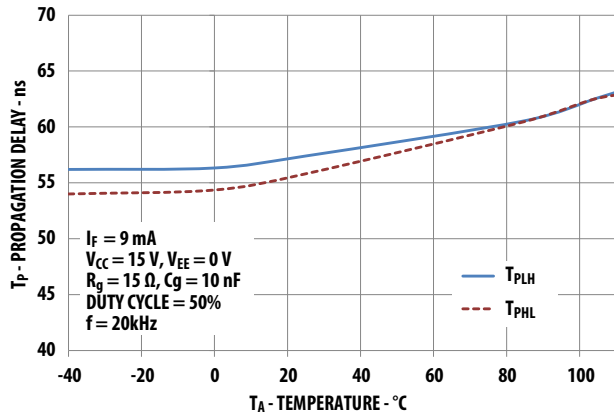


Figure 9. Propagation delay vs. temperature

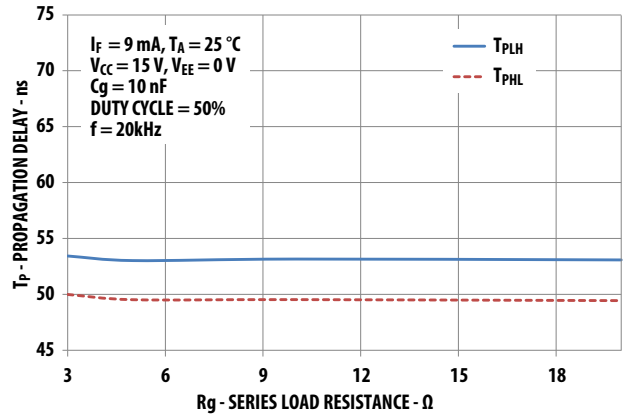


Figure 10. Propagation delay vs.  $R_g$

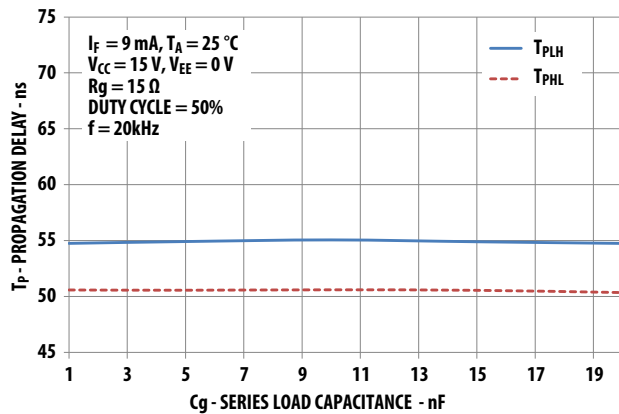


Figure 11. Propagation delay vs.  $C_g$

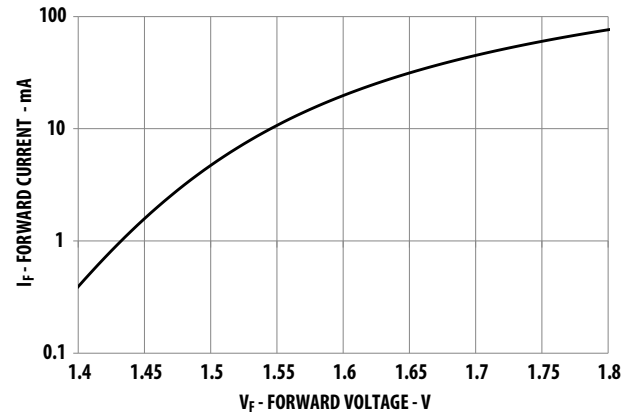


Figure 12. Input Current vs. forward voltage

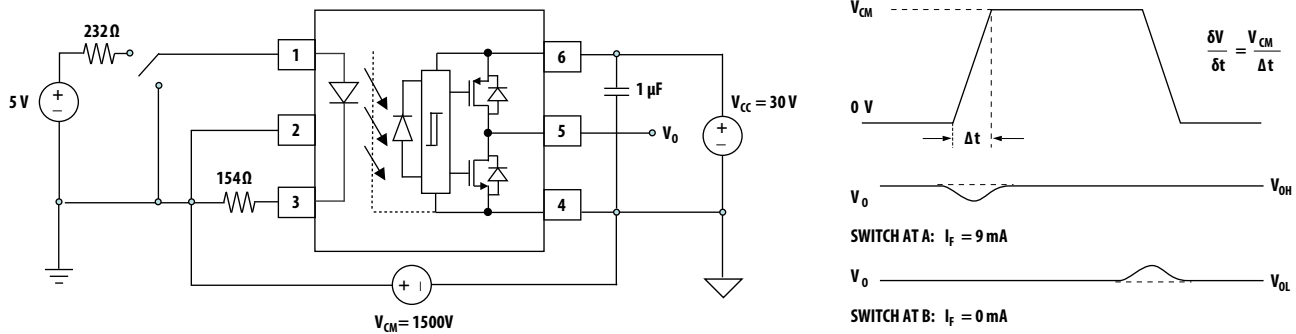


Figure 13. CMR test circuit with split resistors network and waveforms

## Application Information

### Product Overview Description

The ACPL-P347/W347 is an optically isolated power output stage capable of driving SiC/GaN MOSFET or IGBT. Based on BCDMOS technology, this gate drive optocoupler delivers higher peak output current, better rail-to-rail output voltage performance and two times faster speed than the previous generation products.

The high peak output current and short propagation delay are needed for fast SiC/GaN MOSFET switching to reduce dead time and improve system overall efficiency. Rail-to-rail output voltage ensures that the SiC/GaN MOSFET or IGBT's gate voltage is driven to the optimum intended level with no power loss. This helps the designer lower the system power which is suitable for bootstrap power supply operation.

It has very high CMR (common mode rejection) rating which allows the microcontroller and the SiC/GaN MOSFET or IGBT to operate at very large common mode noise found in industrial motor drives and other power switching applications. The input is driven by direct LED current and has a hysteresis that prevents output oscillation if insufficient LED driving current is applied. This will eliminate the need of additional Schmitt trigger circuit at the input LED.

The stretched SO6 package which is up to 50% smaller than conventional DIP package facilitates smaller more compact design. These stretched packages are compliant to many industrial safety standards such as IEC/EN/DIN EN 60747-5-5, UL 1577 and CSA.

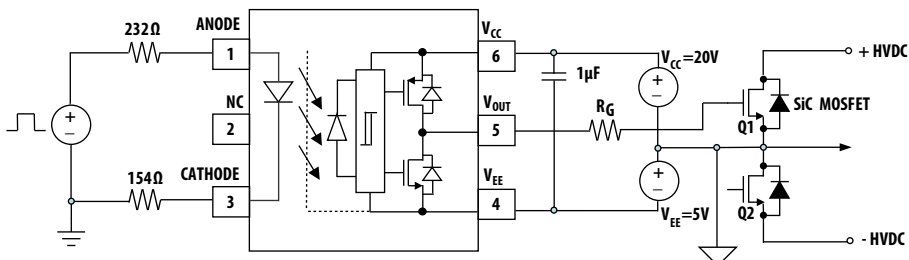


Figure 14. Recommended application circuit with split resistors LED drive.

### Recommended Application Circuit

The recommended application circuit shown in Figure 14 illustrates a typical gate drive implementation using the ACPL-P347/W347.

The supply bypass capacitors (1 μF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (4.2 mA) power supply will be enough to power the device. The split resistors (in the ratio of 1.5:1) across the LED will provide a high CMR response by providing a balanced resistance network across the LED.

The gate resistor  $R_G$  serves to limit gate charge current and controls the MOSFET switching times.

In PC board design, care should be taken to avoid routing the SiC/GaN MOSFET drain or source traces close to the ACPL-P347/W347 input as this can result in unwanted coupling of transient signals into ACPL-P347/W347 and degrade performance.

## Selecting the Gate Resistor (R<sub>G</sub>)

Step 1: Calculate R<sub>G</sub> minimum from the I<sub>OL</sub> peak specification. The SiC/GaN MOSFET and R<sub>G</sub> in Figure 14 can be analyzed as a simple RC circuit with a voltage supplied by ACPL-P347/W347.

$$R_G \geq \frac{V_{CC} - V_{EE}}{I_{OLPEAK}}$$

$$= \frac{20 - (-5)V}{1A}$$

$$= 25\Omega$$

The external gate resistor, R<sub>G</sub> will ensure the output current will not exceed the device absolute maximum rating of 1 A.

## LED Drive Circuit Considerations for High CMR Performance

Figure 15 shows the recommended drive circuit for the ACPL-P347/W347 that gives optimum common-mode rejection. The two current setting resistors balance the common mode impedances at the LED's anode and cathode. The balanced I<sub>LED</sub>-setting resistors help equalize the common mode voltage change at the anode and cathode. The shunt drive input circuit will also help to achieve high CML performance by shunting the LED in the off state.

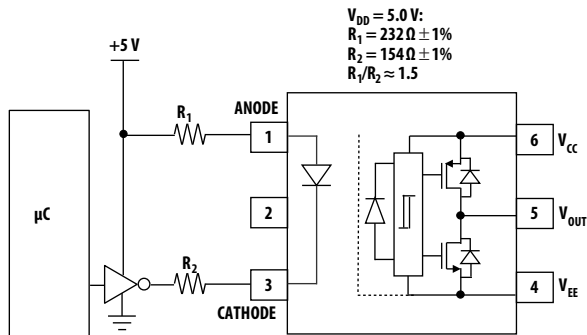


Figure 15. Recommended high-CMR drive circuit for the ACPL-P347/W347.

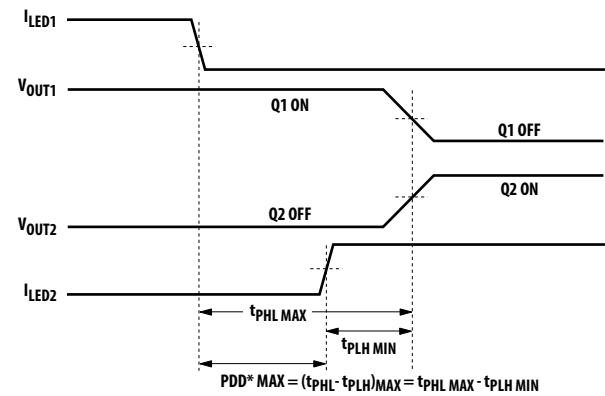
## Dead Time and Propagation Delay Specifications

The ACPL-P347/W347 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 14) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 16. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD<sub>MAX</sub>, which is specified to be 100 ns over the operating temperature range of 40 °C to 105 °C.

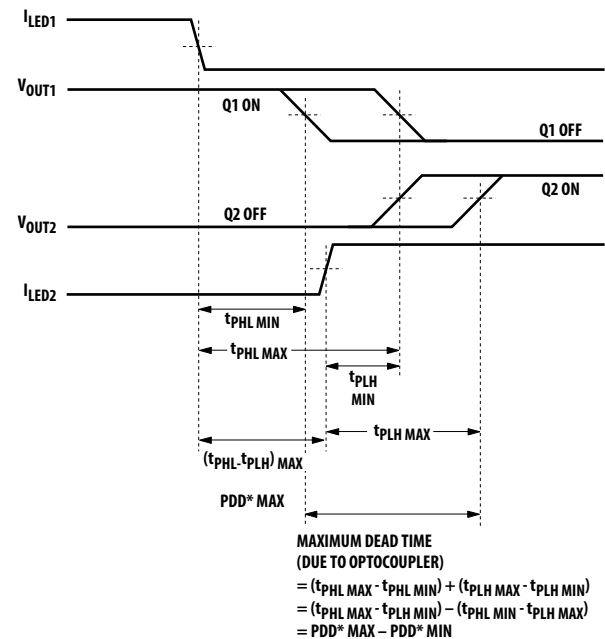
Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 17. The maximum dead time for the ACPL-P347/W347 is 100 ns (= 50 ns - (-50 ns)) over an operating temperature range of -40 °C to 105 °C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical MOSFETs.



\*PDD = PROPAGATION DELAY DIFFERENCE  
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 16. Minimum LED skew for zero dead time.



\*PDD = PROPAGATION DELAY DIFFERENCE  
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 17. Waveforms for dead time.

## LED Current Input with Hysteresis

The detector has optical receiver input stage with built in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 5) provides differential mode noise immunity and minimizes the potential for output signal chatter.

## Thermal Model for ACPL-P347/W347 Stretched S06 Package Optocoupler

Definitions:

R<sub>11</sub>: Junction to Ambient Thermal Resistance of LED due to heating of LED

R<sub>12</sub>: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)

R<sub>21</sub>: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.

R<sub>22</sub>: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).

P<sub>1</sub>: Power dissipation of LED (W).

P<sub>2</sub>: Power dissipation of Detector / Output IC (W).

T<sub>1</sub>: Junction temperature of LED (°C).

T<sub>2</sub>: Junction temperature of Detector (°C).

T<sub>A</sub>: Ambient temperature.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23 °C in still air

Thermal Resistance	°C/W
R <sub>11</sub>	135
R <sub>12</sub>	27
R <sub>21</sub>	39
R <sub>22</sub>	47

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB) per JEDEC standards. The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} * P_1 + R_{12} * P_2) + T_A \text{ -- (1)}$$

$$T_2 = (R_{21} * P_1 + R_{22} * P_2) + T_A \text{ -- (2)}$$

Using the given thermal resistances and thermal model formula in this datasheet, we can calculate the junction temperature for both LED and the output detector. Both junction temperatures should be within the absolute maximum rating.

For example, given P<sub>1</sub> = 17 mW, P<sub>2</sub> = 214 mW, T<sub>A</sub> = 85 °C:

LED junction temperature,

$$\begin{aligned} T_1 &= (R_{11} * P_1 + R_{12} * P_2) + T_A \\ &= (135 * 0.017 + 27 * 0.214) + 85 \\ &= 93.1^\circ\text{C} \end{aligned}$$

Output IC junction temperature,

$$\begin{aligned} T_2 &= (R_{21} * P_1 + R_{22} * P_2) + T_A \\ &= (39 * 0.017 + 47 * 0.214) + 85 \\ &= 95.7^\circ\text{C} \end{aligned}$$

T<sub>1</sub> and T<sub>2</sub> should be limited to 125 °C based on the board layout and part placement.

## Related Application Notes

AV02-0421EN	AN-5336	Gate Drive Optocoupler Basic Design for IGBT / MOSFET
AV02-3698EN	AN-1043	Common-Mode Noise: Sources and Solutions
AV02-0310EN	Reliability Data	Plastics Optocouplers Product ESD and Moisture Sensitivity

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