



100V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _C = +25°C
100V	$28m\Omega$ @ $V_{GS} = 10V$	55A

Description

This new generation MOSFET features low on-resistance and fast switching, making it ideal for high-efficiency power management applications.

Applications

- Engine Management Systems
- Body Control Electronics
- DC-DC Converters

Features

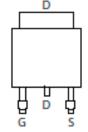
- Rated to +175°C Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching Ensures More Reliable and Robust End Application
- Low R_{DS(ON)} Minimises Power Losses
- Low Q_a Minimises Switching Losses
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- An Automotive-Compliant Part is Available Under Separate Datasheet (<u>DMNH10H028SK3Q</u>)

Mechanical Data

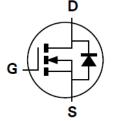
- Case: TO252
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.33 grams (Approximate)



Top View



Pin Out Top View



Equivalent Circuit

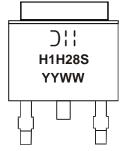
Ordering Information (Note 4)

Part Number	Case	Packaging
DMNH10H028SK3-13	TO252	2,500/Tape & Reel

Notes:

- 1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Dil = Manufacturer's Marking
H1H28S = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Digit of Year (ex: 15 = 2015)
WW = Week Code (01 to 53)



Maximum Ratings $(@T_A = +25^{\circ}C, \text{ unless otherwise specified.})$

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V _{GS} = 10V	$T_{C} = +25^{\circ}C$ $T_{C} = +100^{\circ}C$	I _D	55 39	А
Pulsed Drain Current (10μs Pulse, Duty Cycle = 1%)		I _{DM}	58	Α
Maximum Continuous Body Diode Forward Current (Note 5)		Is	2.2	Α
Avalanche Current, L = 0.1mH		I _{AS}	29	Α
Avalanche Energy, L = 0.1mH		E _{AS}	43	mJ

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)		P_{D}	2.0	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	В	74	°C/W
Thermal Resistance, Junction to Ambient (Note 3)	t<10s	$R_{ hetaJA}$	25	
Total Power Dissipation (Note 6)		P _D	3.7	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	D.	40	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{ hetaJA}$	13	
Thermal Resistance, Junction to Case		$R_{ heta JC}$	1.2	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +175	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	100	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current, T _J = +25°C	I _{DSS}	_	_	1	μA	V _{DS} = 100V, V _{GS} = 0V	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)				•			
Gate Threshold Voltage	V _{GS(TH)}	2.0	2.5	3.3	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	20	28	mΩ	$V_{GS} = 10V, I_D = 20A$	
Diode Forward Voltage	V _{SD}	_	0.7	1.2	V	V _{GS} = 0V, I _S = 1.0A	
DYNAMIC CHARACTERISTICS (Note 8)				•			
Input Capacitance	C _{iss}	_	2245	_	pF	V _{DS} = 50V, V _{GS} = 0V, -f = 1MHz	
Output Capacitance	Coss	_	173	_	pF		
Reverse Transfer Capacitance	C _{rss}	_	68	_	pF		
Gate Resistance	R_g	_	1.9	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 10V)	Qg	_	36	_	nC		
Total Gate Charge (V _{GS} = 6V)	Qg	_	22	_	nC	\/ 50\/ I= -20A	
Gate-Source Charge	Q_{gs}	_	7.3	_	nC	$V_{DS} = 50V, I_{D} = 20A$	
Gate-Drain Charge	Q_{gd}	_	9.2	_	nC	1	
Turn-On Delay Time	t _{D(ON)}	_	6.4	_	ns		
Turn-On Rise Time	t _R	_	5.8	_	ns	$V_{GS} = 10V, V_{DS} = 50V,$	
Turn-Off Delay Time	t _{D(OFF)}	_	17.8	_	ns	$R_G = 3\Omega$, $I_D = 20A$	
Turn-Off Fall Time	t _F	_	4.8	_	ns		
Body Diode Reverse Recovery Time	t _{RR}	_	35	_	ns	I _F = 20A, di/dt = 100A/µs	
Body Diode Reverse Recovery Charge	Q_{RR}	_	47	_	nC	I _F = 20A, di/dt = 100A/µs	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

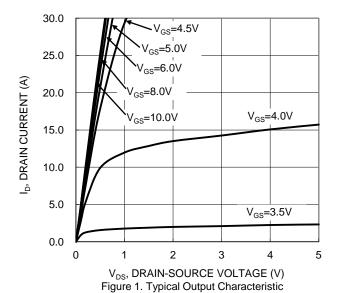
7. Short duration pulse test used to minimize self-heating effect.

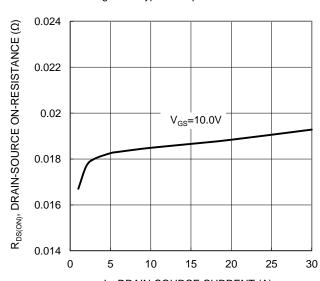
^{6.} Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

7. Short direction pulse test used to minimize self-hosting effect.

^{8.} Guaranteed by design. Not subject to product testing.







I_D, DRAIN-SOURCE CURRENT (A)
Figure 3. Typical On-Resistance vs. Drain Current and
Gate Voltage

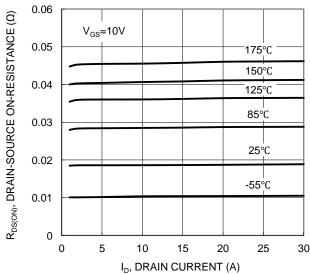
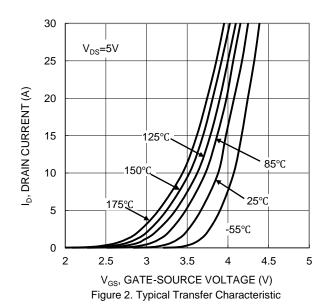
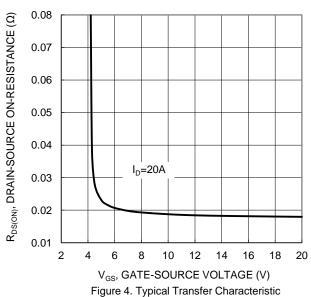
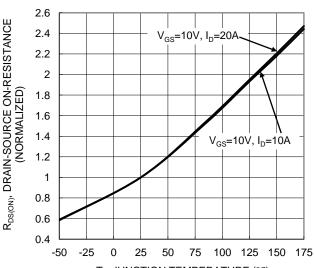


Figure 5. Typical On-Resistance vs. Drain Current and Temperature







T_J, JUNCTION TEMPERATURE (°C) Figure 6. On-Resistance Variation with Temperature

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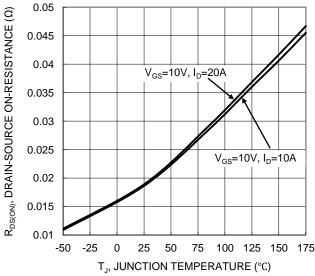


Figure 7. On-Resistance Variation with Temperature

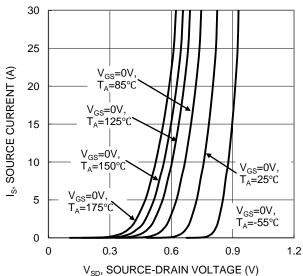
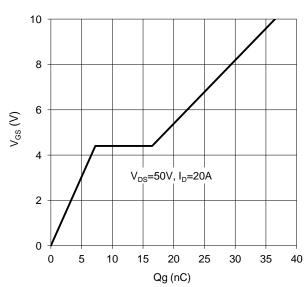
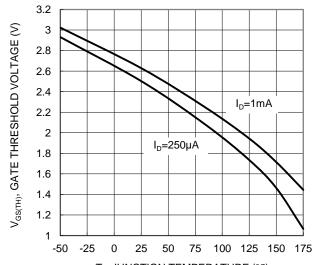


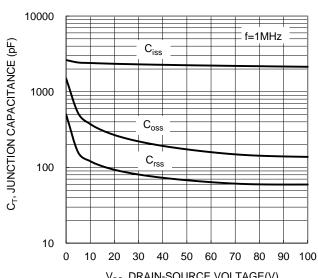
Figure 9. Diode Forward Voltage vs. Current



DMN Figure 11. Gate Charge



T_J, JUNCTION TEMPERATURE (°C) Figure 8. Gate Threshold Variation vs. Junction Temperature



V_{DS}, DRAIN-SOURCE VOLTAGE(V) Figure 10. Typical Junction Capacitance

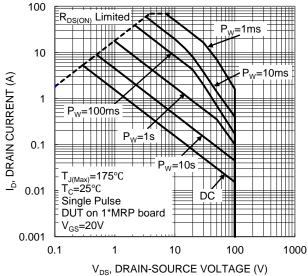


Figure 12. SOA, Safe Operation Area



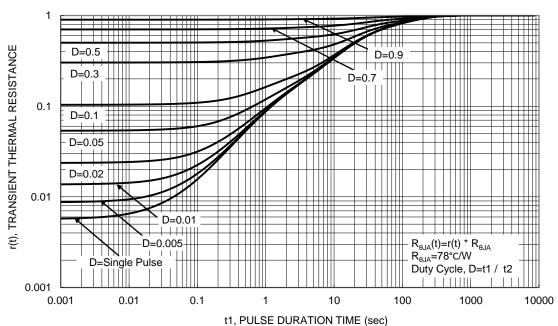
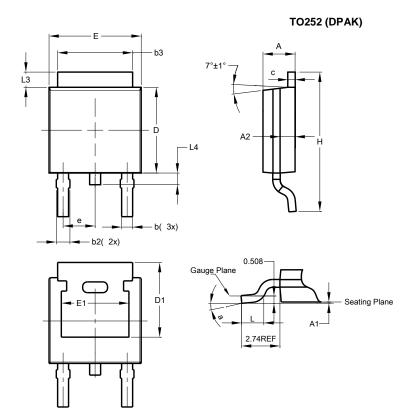


Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

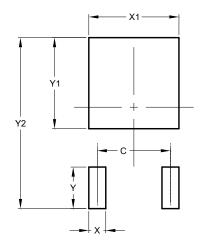


TO252 (DPAK)						
Dim	Min	Max	Тур			
Α	2.19	2.39	2.29			
A1	0.00	0.13	0.08			
A2	0.97	1.17	1.07			
b	0.64	0.88	0.783			
b2	0.76	1.14	0.95			
b3	5.21	5.46	5.33			
С	0.45	0.58	0.531			
D	6.00	6.20	6.10			
D1	5.21	-	-			
е	-	-	2.286			
Е	6.45	6.70	6.58			
E1	4.32	-	-			
Н	9.40	10.41	9.91			
L	1.40	1.78	1.59			
L3	0.88	1.27	1.08			
L4	0.64	1.02	0.83			
а	0°	10°	-			
All Dimensions in mm						

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

TO252 (DPAK)



Dimensions	Value (in mm)			
С	4.572			
Х	1.060			
X1	5.632			
Υ	2.600			
Y1	5.700			
Y2	10.700			



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