



### P-CHANNEL ENHANCEMENT MODE MOSFET

## **Product Summary**

V <sub>(BR)DSS</sub>	R <sub>DS(on)max</sub>	I <sub>D</sub> T <sub>A</sub> = +25°C
-30V	$14m\Omega @ V_{GS} = -10V$	-10.4A
-30 V	$25m\Omega$ @ $V_{GS} = -4.5V$	-7.8A

## **Description**

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## **Applications**

- Load Switch
- Power Management Functions
- DC-DC Converters

## **Features and Benefits**

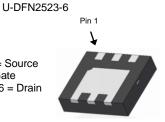
- Low On-Resistance
- Low Input Capacitance
- Low Input/Output Leakage
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- · Qualified to AEC-Q101 Standards for High Reliability

### **Mechanical Data**

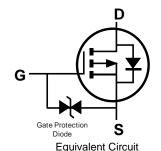
- Case: U-DFN2523-6
- Case Material: Molded Plastic, "Green" Molding Compound;
   UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 64
- Weight: 0.008 grams (Approximate)



Pin 1, 2 = Source Pin 3 = Gate Pin 4, 5, 6 = Drain



Bottom View



## **Ordering Information (Note 4)**

Part Number	Case	Packaging
DMP3017SFK-7	U-DFN2523-6	3,000 / Tape & Reel
DMP3017SFK-13	U-DFN2523-6	10,000 / Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant
- See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

## **Marking Information**

### U-DFN2523-6



P7 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: B = 2014) M = Month (ex: 9 = September)

Date Code Key

Year	201	4	2015		2016	20	17	2018		2019	2	2020	
Code	В		С		D		Ε	F		G		Н	
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	
Code	1	2	3	4	5	6	7	8	9	0	N	D	



## **Maximum Ratings** (@ $T_A = +25^{\circ}C$ , unless otherwise specified.)

Characteristic	Symbol	Value	Units		
Drain-Source Voltage	$V_{DSS}$	-30	V		
Gate-Source Voltage			$V_{GSS}$	±25	V
Continuous Drain Current (Note 6) $V_{GS} = -10V$ Steady $T_A = +25^{\circ}C$ State $T_A = +70^{\circ}C$			I <sub>D</sub>	-10.4 -8.3	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	I <sub>D</sub>	-7.8 -6.2	А		
Maximum Continuous Body Diode Forward Current (N	Is	-3	Α		
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I <sub>DM</sub>	-80	A		
Avalanche Current (Note 7)	I <sub>AS</sub>	-14	А		
Avalanche Energy (Note 7)	E <sub>AS</sub>	104	mJ		

## Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)		P <sub>D</sub>	1	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	123	°C/W
Total Power Dissipation (Note 6)		P <sub>D</sub>	2.2	W
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	55	°C/W
Total Power Dissipation (Note 6)	T <sub>C</sub> = +25°C	P <sub>D</sub>	17	W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	7.2	°C/W
Operating and Storage Temperature Range		T <sub>J,</sub> T <sub>STG</sub>	-55 to +150	°C

## Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

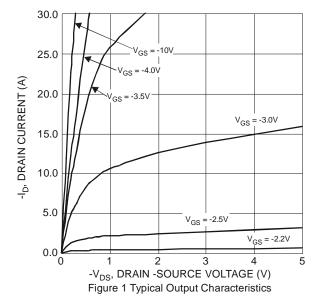
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	_	_	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -10mA	
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C			_	-1		V 24V V 0V	
Zero Gate Voltage Drain Current T <sub>J</sub> = +150°C (Note 9)	I <sub>DSS</sub>		_	-100	μA	$V_{DS} = -24V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±10	μΑ	$V_{GS} = \pm 25V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)	•		•	•			
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1	-1.6	-2.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
Static Drain-Source On-Resistance	D	_	9.5	14	mΩ	$V_{GS} = -10V, I_D = -9.5A$	
Static Dialit-Source Off-Resistance	R <sub>DS(ON)</sub>	_	15	25	11122	$V_{GS} = -4.5V, I_{D} = -6.9A$	
Diode Forward Voltage	V <sub>SD</sub>	_	-0.7	-1.2	V	$V_{GS} = 0V$ , $I_S = -1A$	
On State Drain Current (Note 9)	I <sub>D(ON)</sub>	-20	_	_	Α	V <sub>D</sub> S ≦-5V, V <sub>G</sub> S = -10V	
DYNAMIC CHARACTERISTICS (Note 9)						•	
Input Capacitance	Ciss	1	2207	4414		15)/ )/ 0)/	
Output Capacitance	Coss	_	390	780	pF	$V_{DS} = -15V, V_{GS} = 0V,$ f = 1MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	343	686		1 - 11011 12	
Gate Resistance	Rg	_	8.4	20	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge (V <sub>GS</sub> = -10V)	Qg	_	42.7	90			
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Qg	_	21.6	45	nC	V <sub>DS</sub> = -15V. I <sub>D</sub> = -9.5A	
Gate-Source Charge	Q <sub>gs</sub>	_	7.9	16	IIC	V <sub>DS</sub> = -15V, I <sub>D</sub> = -9.5A	
Gate-Drain Charge	Q <sub>gd</sub>	_	10	20			
Turn-On Delay Time	t <sub>D(on)</sub>	_	7.35	15			
Turn-On Rise Time	t <sub>r</sub>	_	16.4	30		$V_{DD} = -15V, V_{GS} = -10V,$	
Turn-Off Delay Time	t <sub>D(off)</sub>	-	67.2	110	ns	$R_{GEN} = 6\Omega$ , $I_D = -9.5A$	
Turn-Off Fall Time	t <sub>f</sub>	_	37.5	60	1		
Reverse Recovery Time	t <sub>rr</sub>	-	18.6	35	ns	0.54 45/44 4004/	
Reverse Recovery Charge	Q <sub>rr</sub>	_	8.6	17.5	$I_{S} = -9.5A$ , di/dt = 100A/ $\mu$ s		

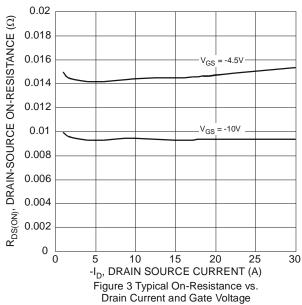
Notes:

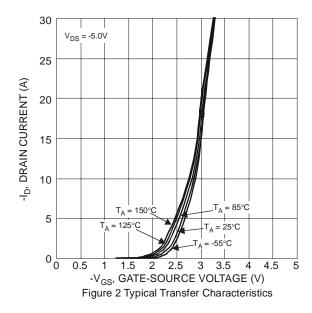
- 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1-inch square copper plate.
  7. UIS in production with L = 1mH, T<sub>J</sub> = +25°C.
  8. Short duration pulse test used to minimize self-heating effect.

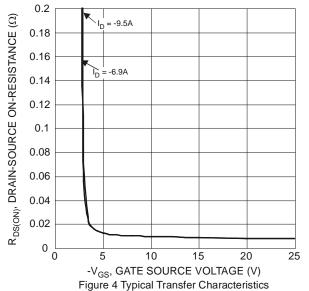
- 9. Guaranteed by design. Not subject to production testing.

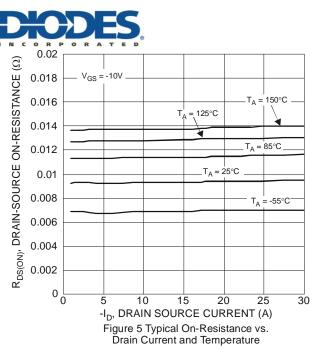


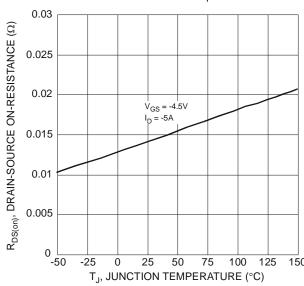


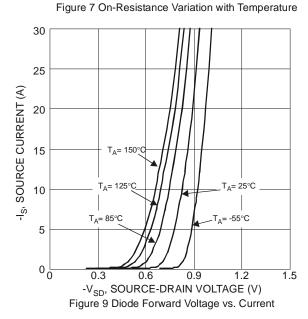












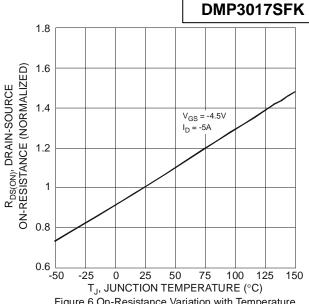


Figure 6 On-Resistance Variation with Temperature

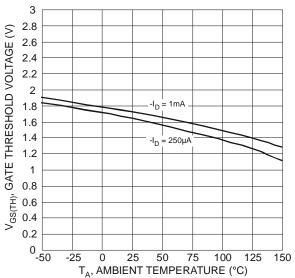
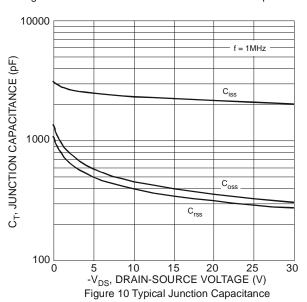
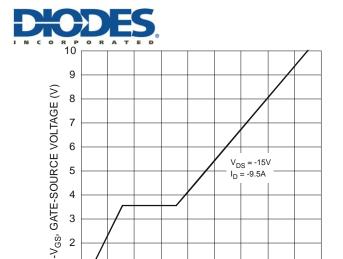


Figure 8 Gate Threshold Variation vs. Ambient Temperature





20 25

Q<sub>q</sub>, TOTAL GATE CHARGE (nC)

Figure 11 Gate-Charge Characteristics

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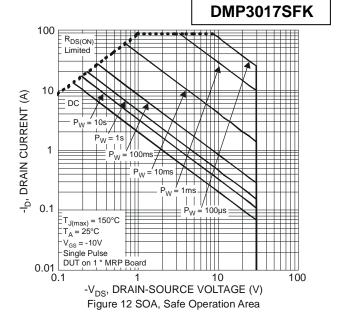
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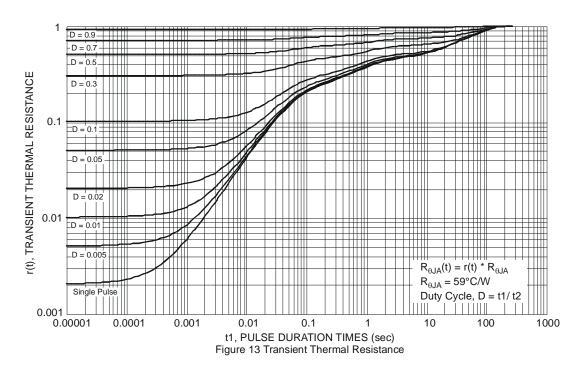
40 45

1

0

0 5

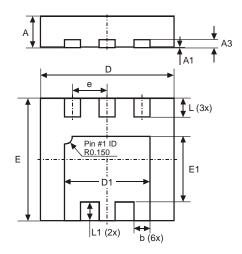






## **Package Outline Dimensions**

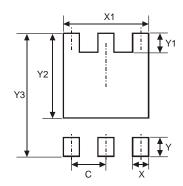
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



	U-DFN2523-6							
Dim	Min	Max	Тур					
Α	0.57	0.63	0.60					
A1	0	0.05	0.02					
A3	-	_	0.152					
b	0.25	0.35	0.30					
D	2.45	2.55	2.50					
D1	1.55	1.65	1.60					
е	_	_	0.65					
Е	2.25	2.35	2.30					
E1	1.18	1.28	1.23					
L	0.30	0.40	0.35					
L1	0.30	0.40	0.35					
All Dimensions in mm								

## **Suggested Pad Layout**

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



Dimensions	Value (in mm)
С	0.650
Х	0.400
X1	1.700
Υ	0.650
Y1	0.450
Y2	1.830
Y3	2.700



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