40V P-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI®

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D T_A = +25°C
-40V	11mΩ @ V_{GS} = -10V	-17.0A
	15mΩ @ V_{GS} = -4.5V	-14.5A

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **PPAP Capable (Note 4)**

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

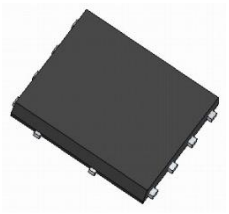
Mechanical Data

- Case: PowerDI®5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – 100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

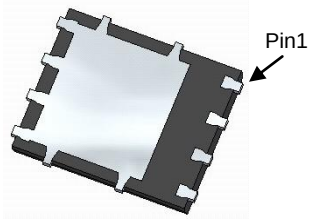
Applications

- DC-DC Converters
- Power Management Functions
- Analog Switch

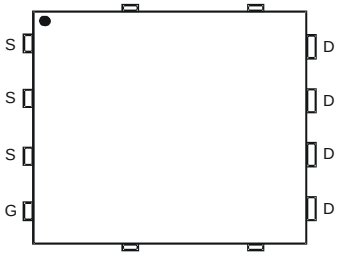
PowerDI5060-8



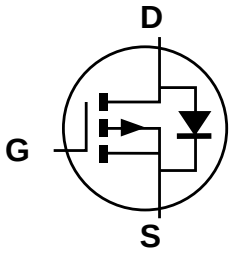
Top View



Bottom View



Top View
Pin Configuration



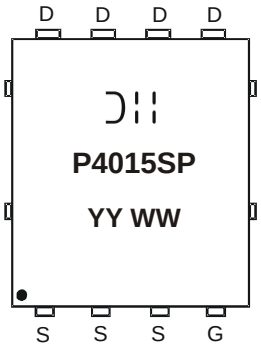
Internal Schematic

Ordering Information (Note 5)

Part Number	Compliance	Case	Packaging
DMP4015SPSQ-13	Automotive	PowerDI5060-8	2,500/Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q101 qualified and are PPAP capable. Refer to http://www.diodes.com/quality/product_compliance_definitions/.
5. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



= Manufacturer's Marking
P4015SP = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 13 = 2013)
WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-40	V
Gate-Source Voltage			V_{GSS}	±25	V
Continuous Drain Current (Note 6) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-8.5 -6.8	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	-13.0 -10.5	A
Continuous Drain Current (Note 7) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-11.0 -8.7	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	-17.0 -13.5	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-100	A
Maximum Body Diode Continuous Current (Note 7)			I_S	-3.5	A
Avalanche Current (Note 8)			I_{AS}	-22	A
Avalanche Energy (Note 8)			E_{AS}	242	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.3	W
	T_A = +70°C		0.8	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	96.4	°C/W
	t<10s		40.6	°C/W
Total Power Dissipation (Note 7)	T_A = +25°C	P_D	2.1	W
	T_A = +70°C		1.4	
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	$R_{\theta JA}$	55.0	°C/W
	t<10s		24.0	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	4.15	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 6. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
8. UIS in production with L = 0.1mH, TJ = +25°C.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±25V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(th)}$	-1.5	-2	-2.5	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	7	11	mΩ	V_{GS} = -10V, I_D = -9.8A
		—	9	15		V_{GS} = -4.5V, I_D = -9.8A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	26	—	S	V_{DS} = -20V, I_D = -9.8A
Diode Forward Voltage	V_{SD}	—	-0.7	-1	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	4,234	—	pF	V_{DS} = -20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	1,036	—		
Reverse Transfer Capacitance	C_{rss}	—	526	—		
Gate Resistance	R_G	—	7.77	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	47.5	—	nC	V_{DS} = -20V, V_{GS} = -5V I_D = -9.8A
Gate-Source Charge	Q_{gs}	—	14.2	—		
Gate-Drain Charge	Q_{gd}	—	13.5	—		
Turn-On Delay Time	$t_{D(on)}$	—	13.2	—	ns	V_{GS} = -10V, V_{DD} = -20V, R_G = 6Ω, I_D = -1A, R_L = 20Ω
Turn-On Rise Time	t_r	—	10	—		
Turn-Off Delay Time	$t_{D(off)}$	—	302.7	—		
Turn-Off Fall Time	t_f	—	137.9	—		

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to production testing.

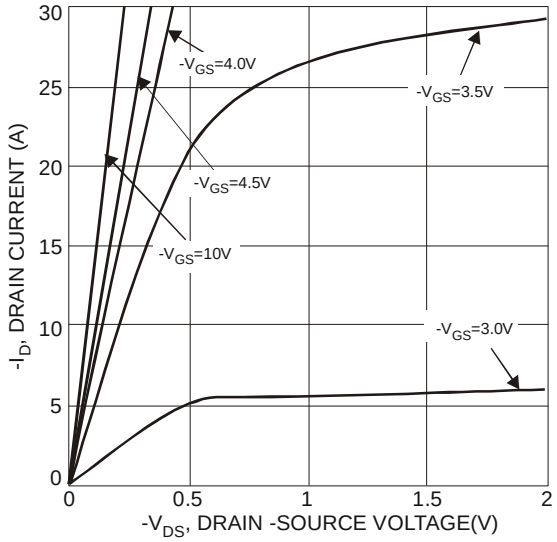


Fig. 1 Typical Output Characteristics

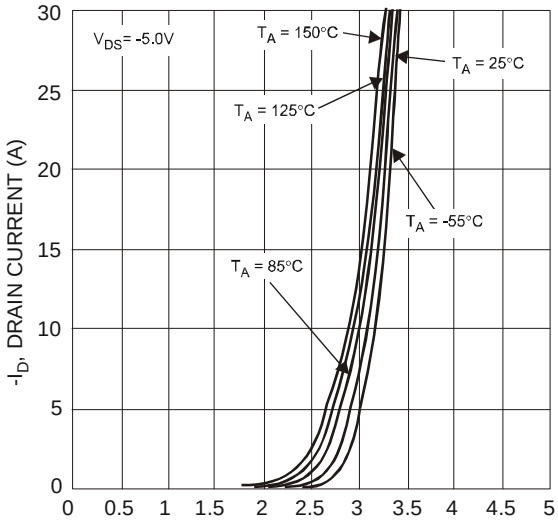


Fig. 2 Typical Transfer Characteristics

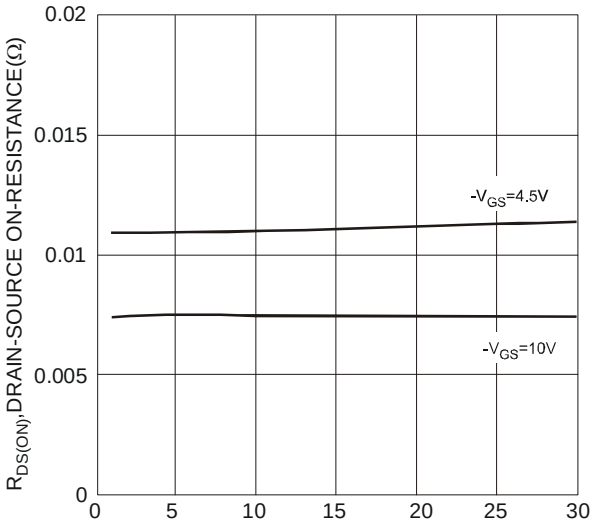


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

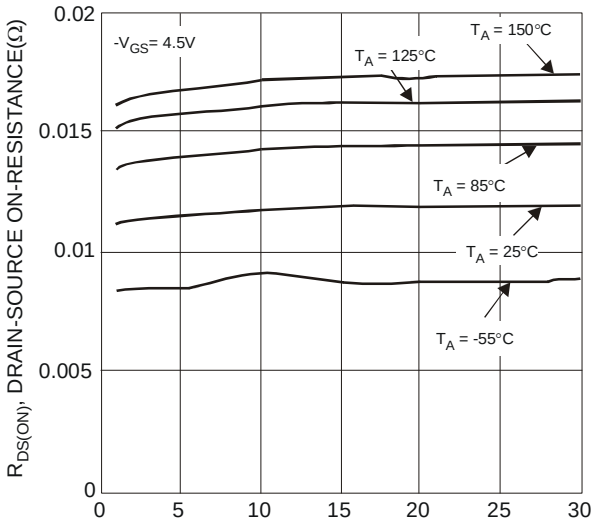


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

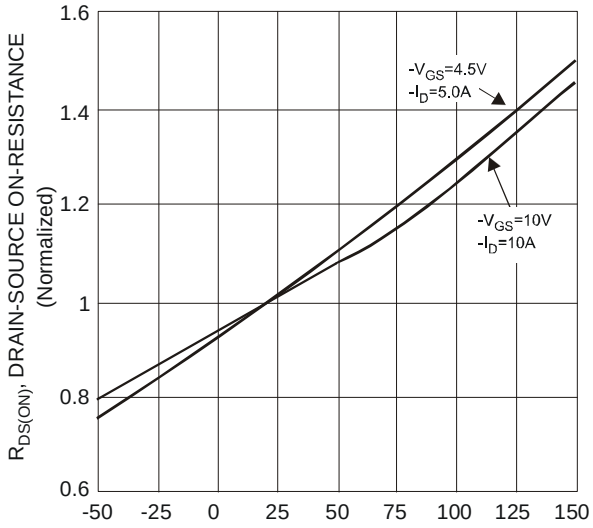


Fig. 5 On-Resistance Variation with Temperature

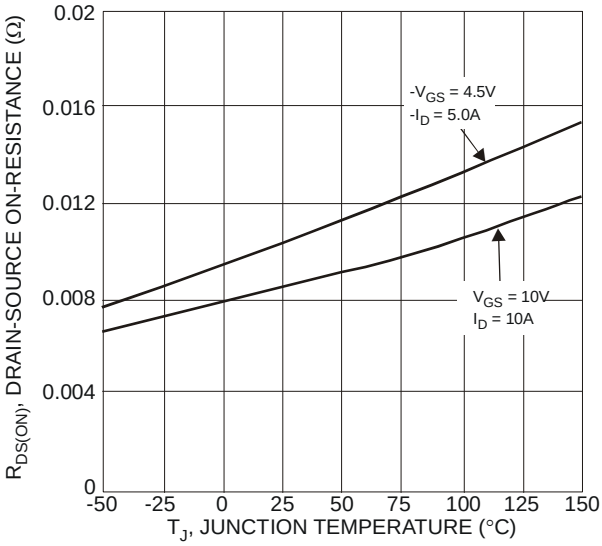


Fig. 6 On-Resistance Variation with Temperature

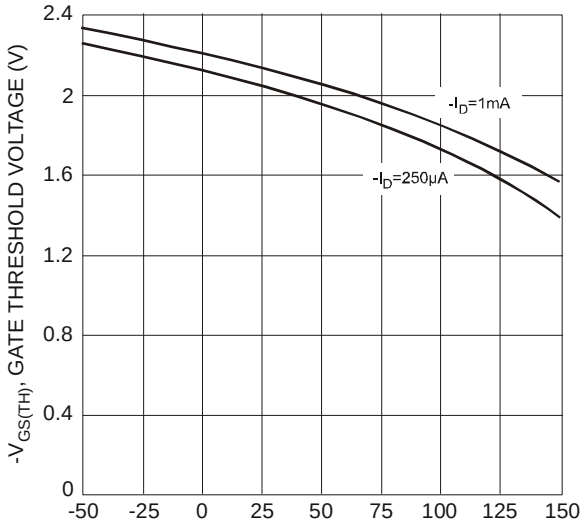


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

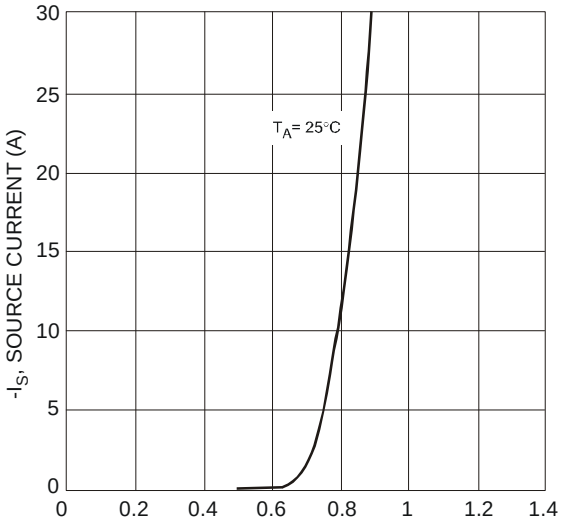


Fig. 8 Diode Forward Voltage vs. Current

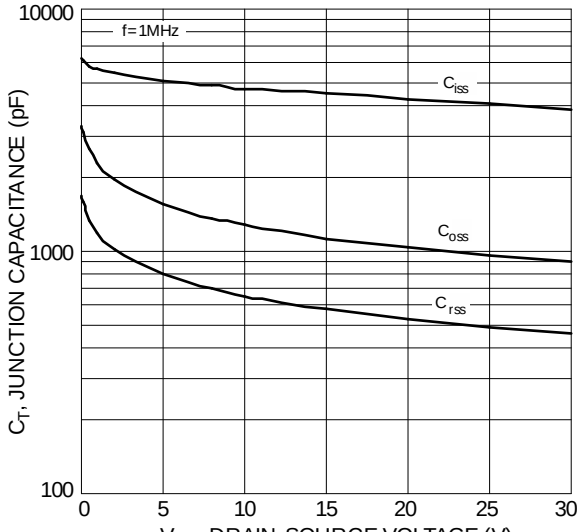


Fig. 9 Typical Junction Capacitance

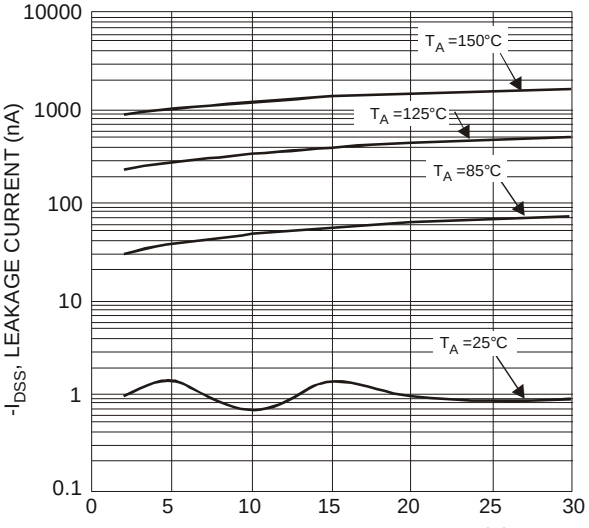


Fig. 10 Typical Drain-Source Leakage Current vs. Voltage

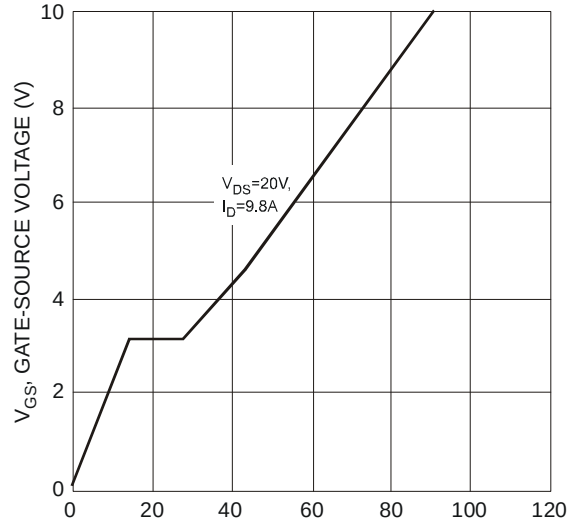


Fig. 11 Gate-Charge Characteristics

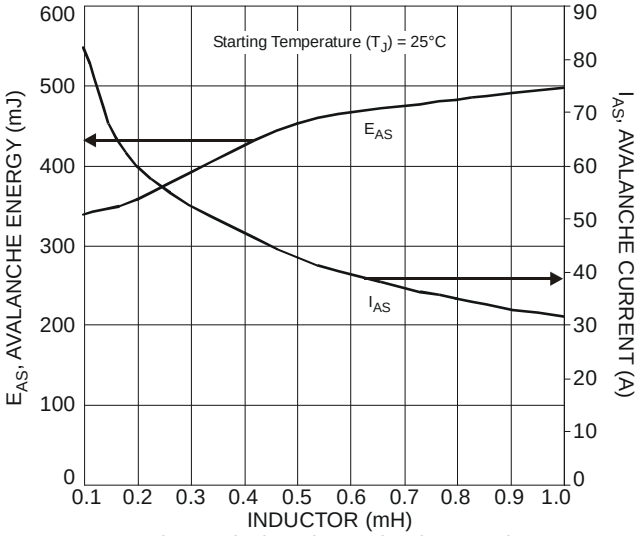


Fig. 12 Single-Pulse Avalanche Tested

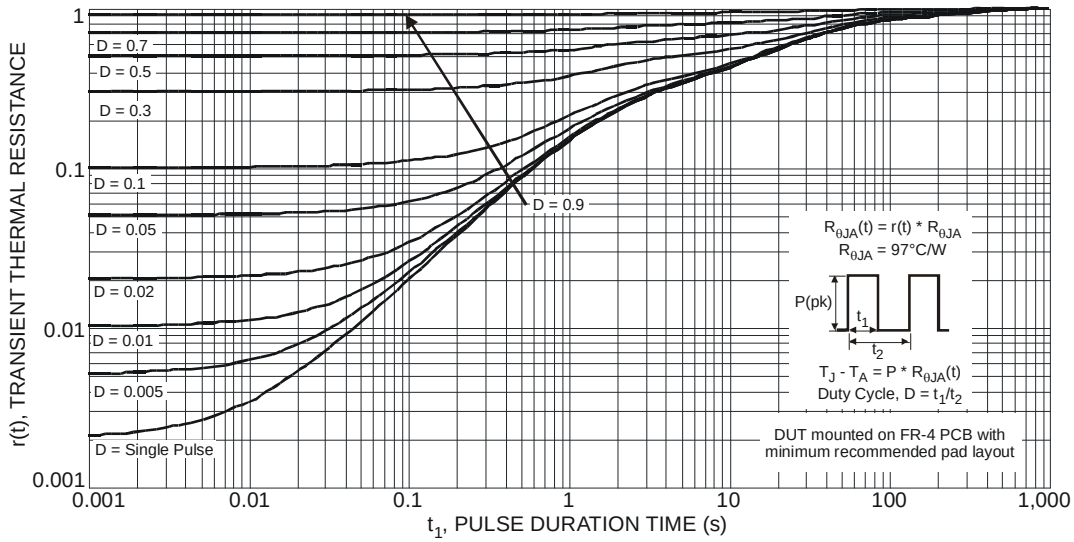
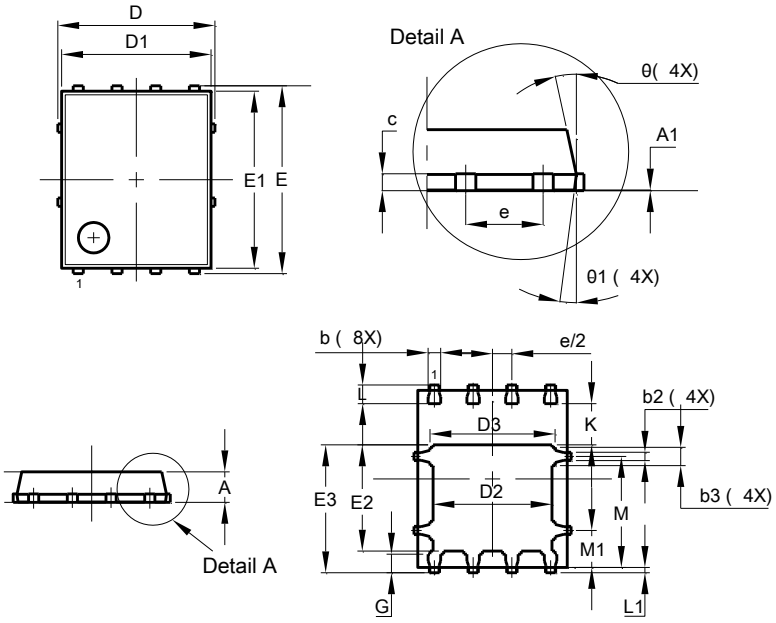


Fig. 13 Transient Thermal Response

Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

PowerDI5060-8

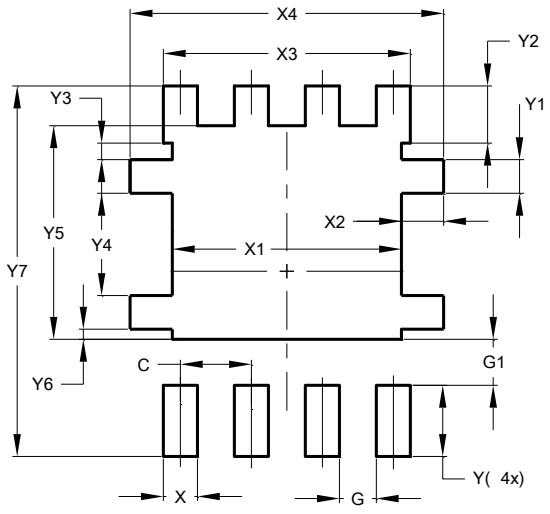


PowerDI5060-8			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	–
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	–	–
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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