





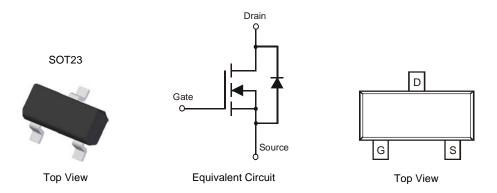
N-CHANNEL ENHANCEMENT MODE MOSFET

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Notes 3 & 4)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208
 - Weight: 0.008 grams (approximate)



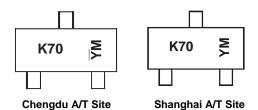
Ordering Information (Note 5)

Part Number	Case	Packaging
BS870-7-F	SOT23	3000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. Product manufactured with Date Code V9 (week 33, 2008) and newer are built with Green Molding Compound. Product manufactured prior to Date Code V9 are built with Non-Green Molding Compound and may contain Halogens or Sb₂O₃ Fire Retardants.
- 5. For packaging details, go to our website at http://www.diodes.com/products/packages.html

Marking Information



K70 = Product Type Marking Code

 \underline{YM} = Date Code Marking for SAT (Shanghai Assembly/ Test site) \overline{YM} = Date Code Marking for CAT (Chengdu Assembly/ Test site) \underline{Y} or \overline{Y} = Year (ex: A = 2013)

M = Month (ex: 9 = September)

Date Code Kev

Year	1998	1999	2000	2001	2002	2003	2004		2011	2012	2013	2014	2015	2016	2017
Code	J	K	L	М	N	Р	R		Υ	Z	Α	В	С	D	Е
Month	Jan	Fe	b	Mar	Apr	May	Ju	n	Jul	Aug	Sep	Ос	t I	Nov	Dec
Code	1	2		3	4	5	6		7	8	9	0		N	D



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units	
Drain-Source Voltage		V_{DSS}	60	V
Drain-Gate Voltage $R_{GS} \le 1.0 M\Omega$		V_{DGR}	60	V
Gate-Source Voltage	Continuous	V _{GSS}	±20	V
Drain Current (Note 6)	Continuous	I _D	250	mA

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 6)	P_{D}	300	mW
Thermal Resistance, Junction to Ambient	$R_{ hetaJA}$	417	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

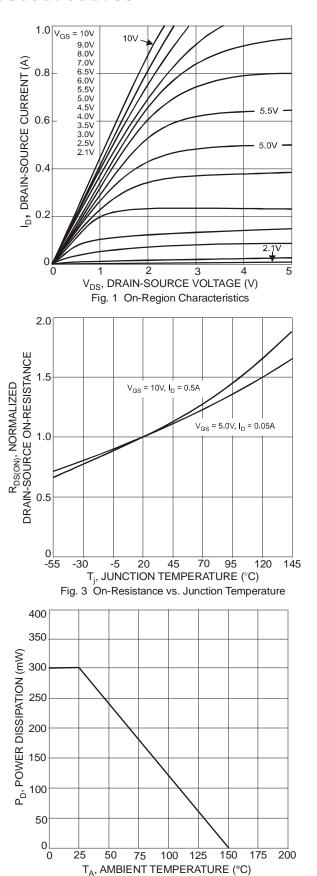
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	60	80		V	$V_{GS} = 0V, I_D = 100 \mu A$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	0.5	μA	$V_{DS} = 25V, V_{GS} = 0V$	
Gate-Body Leakage	I _{GSS}	_	_	±10	nA	$V_{GS} = \pm 15V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(th)}	1.0	2.0	3.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Static Drain-Source On-Resistance	R _{DS} (ON)	_	3.5	5.0	Ω	$V_{GS} = 10V, I_D = 0.2A$	
On-State Drain Current	$I_{D(ON)}$	0.5	1.0	_	Α	$V_{GS} = 10V, V_{DS} = 7.5V$	
Forward Transconductance	g _{FS}	80	_		mS	$V_{DS} = 10V, I_D = 0.2A$	
DYNAMIC CHARACTERISTICS							
Input Capacitance	C _{iss}	_	22	50	pF	101/11/01/	
Output Capacitance	Coss	_	11	25	pF	$V_{DS} = 10V, V_{GS} = 0V$ f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}	_	2.0	5.0	pF	pF I = 1.0WHZ	
SWITCHING CHARACTERISTICS							
Turn-On Delay Time	t _{D(ON)}		2.0	20	ns	$V_{ES} = 10V, R_L = 150\Omega,$	
Turn-Off Delay Time	t _{D(OFF)}	_	5.0	20	ns	$V_{DS} = 10V$, $R_D = 100\Omega$	

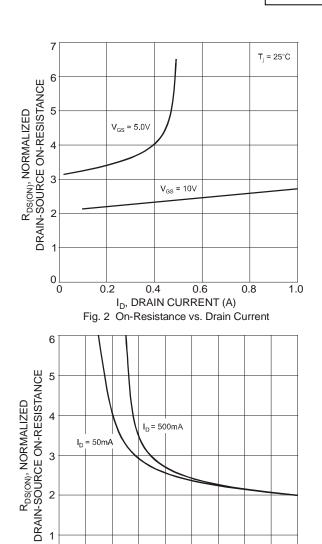
Notes:

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^{6.} Device mounted on FR-4 PCB 1.0 x 0.75 x 0.062 inch pad layout as shown on Diodes, Inc. suggested pad layout AP02001, which can be found on our website at http://www.diodes.com.
7. Short duration pulse test used to minimize self-heating effect.







 $\frac{2}{2}$ $\frac{4}{6}$ $\frac{6}{8}$ $\frac{8}{10}$ $\frac{12}{14}$ $\frac{16}{16}$ $\frac{16}{16}$

Fig. 4 On-Resistance vs. Gate-Source Voltage

Fig. 5 Max Power Dissipation vs. Ambient Temperature

BS870

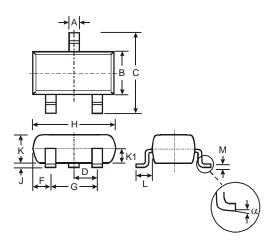
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Package Outline Dimensions

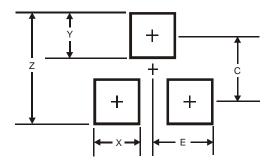
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT23								
Dim	Min	Max	Тур					
Α	0.37	0.51	0.40					
В	1.20	1.40	1.30					
С	2.30	2.50	2.40					
D	0.89	1.03	0.915					
F	0.45	0.60	0.535					
G	1.78	2.05	1.83					
Н	2.80	3.00	2.90					
J	0.013	0.10	0.05					
K	0.903	1.10	1.00					
K1	-	-	0.400					
L	0.45	0.61	0.55					
M	0.085	0.18	0.11					
α	0°	8°	-					
All Dimensions in mm								

Suggested Pad Layout

 $Please see AP02001 \ at \ http://www.diodes.com/datasheets/ap02001.pdf \ for \ the \ latest \ version.$



Dimensions	Value (in mm)
Z	2.9
Х	0.8
Υ	0.9
С	2.0
E	1.35

August 2013

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