



DMC2004VK

COMPLEMENTARY PAIR ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

### **Features**

- Low On-Resistance
- Low Gate Threshold Voltage V<sub>GS(th)</sub> <1V
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Complementary Pair MOSFET
- Ultra-Small Surface Mount Package
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- **ESD Protected Gate**
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

### **Mechanical Data**

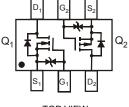
- Case: SOT-563
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.006 grams (approximate)



TOP VIEW



BOTTOM VIEW



TOP VIEW Internal Schematic

### Ordering Information (Note 4)

Part Number	Case	Packaging
DMC2004VK-7	SOT-563	3000/Tape & Reel

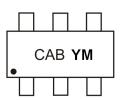
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.

2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and

<1000ppm antimony compounds.

4. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

# **Marking Information**



CAB = Product Type Marking Code YM = Date Code Marking Y = Year ex: U = 2007 M = Month ex: 9 = September

#### Date Code Kev

Notes:

Year	20	07	20	08	20	09	20	10	20	11	20	12
Code	ι	J	١	/	V	V	)	X	١	(	2	7
Month	Jan	Feb	Mar	Apr	Мау	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



# Maximum Ratings N-CHANNEL – Q<sub>1</sub> (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain Source Voltage		V <sub>DSS</sub>	20	V
Gate-Source Voltage		V <sub>GSS</sub>	±8	V
Drain Current (Note 5)	T <sub>A</sub> = +25°C T <sub>A</sub> = +85°C	Ι <sub>D</sub>	670 480	mA

# Maximum Ratings P-CHANNEL – Q<sub>2</sub> (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	±8	V
Drain Current (Note 5) $T_A = +25^{\circ}$ $T_A = +85^{\circ}$		-530 -380	mA

### **Thermal Characteristics**

Characteristic	Symbol	Value	Units	
Total Power Dissipation (Note 5)		PD	0.45	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	Р	281	°C/W
Thermal Resistance, Junction to Amblent (Note 5)	t<10s	$R_{ ext{ heta}JA}$	210	°C/W
Total Power Dissipation (Note 6)		PD	1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	D	129	°C/W
t<10s		$R_{ extsf{ heta}JA}$	97	°C/W
Operating and Storage Temperature Range		T <sub>J,</sub> T <sub>STG</sub>	-55 to +150	°C

# Electrical Characteristics N-CHANNEL – Q1 (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Мах	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)			•				
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	_	_	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 10μA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		_	1.0	μA	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V	
Gate-Source Leakage	I <sub>GSS</sub>		_	± 1.0	μA	$V_{GS}$ = ±4.5V, $V_{DS}$ = 0V	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.5	_	1.0	V	$V_{DS}$ = $V_{GS}$ , $I_D$ = 250 $\mu$ A	
Static Drain-Source On-Resistance	R <sub>DS (ON)</sub>		0.4 0.5 0.7	0.55 0.70 0.90	Ω	$V_{GS}$ = 4.5V, I <sub>D</sub> = 540mA $V_{GS}$ = 2.5V, I <sub>D</sub> = 500mA $V_{GS}$ = 1.8V, I <sub>D</sub> = 350mA	
Forward Transfer Admittance (Note 8)	Y <sub>fs</sub>	200	_	_	mS	V <sub>DS</sub> =10V, I <sub>D</sub> = 0.2A	
Diode Forward Voltage	V <sub>SD</sub>	0.5	_	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 115mA	
DYNAMIC CHARACTERISTICS							
Input Capacitance	C <sub>iss</sub>		_	150	pF		
Output Capacitance	C <sub>oss</sub>		_	25	pF	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V f = 1.0MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	_	20	pF		

Notes:

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

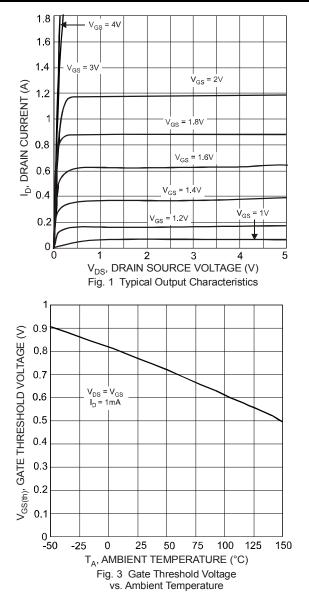
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8. Guaranteed by design. Not subject to product testing.

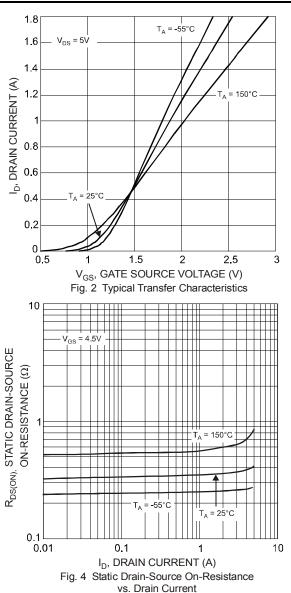


# Electrical Characteristics P-CHANNEL – Q2 (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)				•	•	
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	_	_	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	-1.0	μA	$V_{DS}$ = -20V, $V_{GS}$ = 0V
Gate-Source Leakage	IGSS			± 1.0	μA	$V_{GS}$ = ±4.5V, $V_{DS}$ = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.5	_	-1.0	V	$V_{DS} = V_{GS}, I_D = -250 \mu A$
Static Drain-Source On-Resistance	R <sub>DS (ON)</sub>	_	0.7 1.1 1.7	0.9 1.4 2.0	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -430mA V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -300mA V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -150mA
Forward Transfer Admittance	Y <sub>fs</sub>	200	_	_	mS	V <sub>DS</sub> =10V, I <sub>D</sub> = 0.2A
Diode Forward Voltage	V <sub>SD</sub>	-0.5	_	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -115mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C <sub>iss</sub>	_	_	175	pF	
Output Capacitance	C <sub>oss</sub>		_	30	pF	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V f = 1.0MHz
Reverse Transfer Capacitance	C <sub>rss</sub>			20	pF	

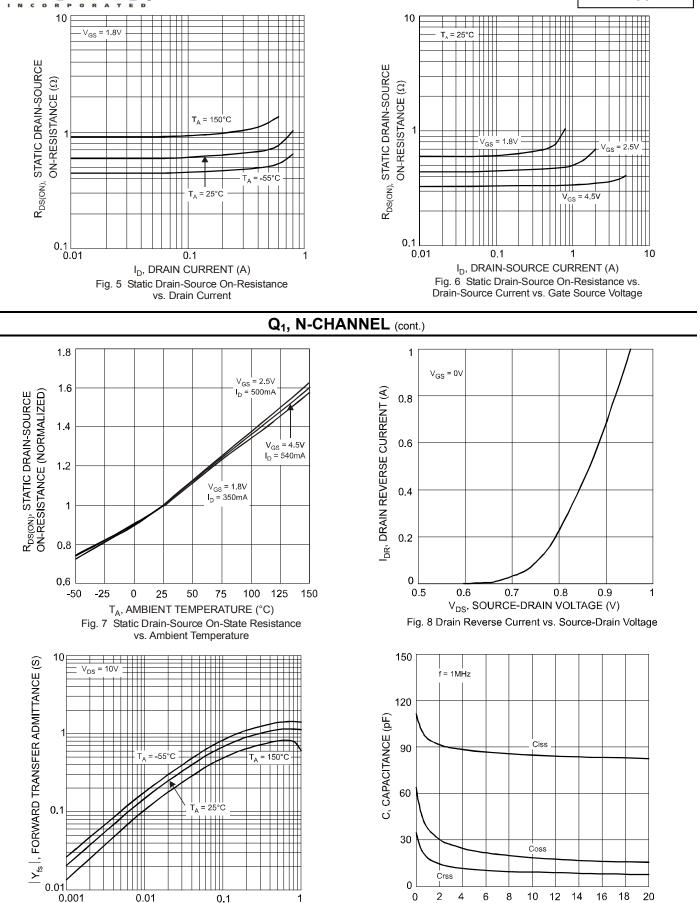


# **Q1, N-CHANNEL**





## DMC2004VK



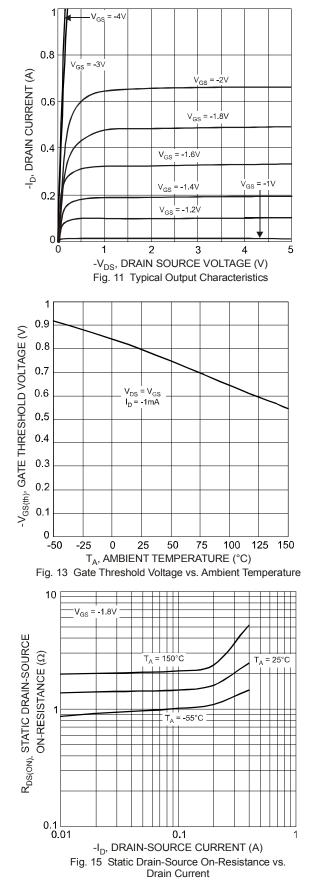
DMC2004VK Document number: DS30925 Rev. 6 - 2

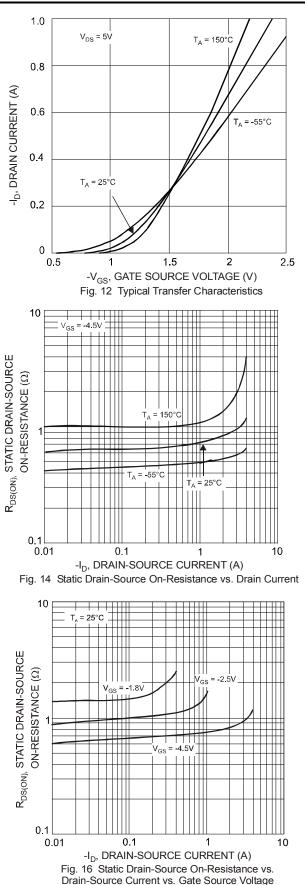
I<sub>D</sub>, DRAIN CURRENT (A) Fig. 9 Forward Transfer Admittance vs. Drain Current V<sub>DS</sub>, DRAIN-SOURCE VOLTAGE (V)

Fig. 10 Typical Capacitance



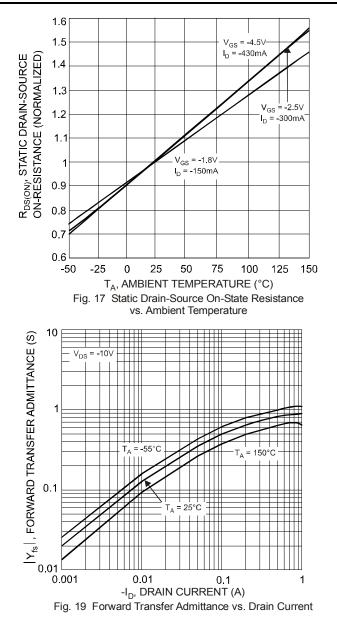
# Q<sub>2</sub>, P-CHANNEL







# Q2, P-CHANNEL (cont.)



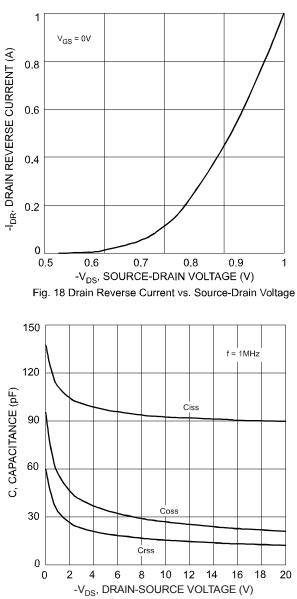
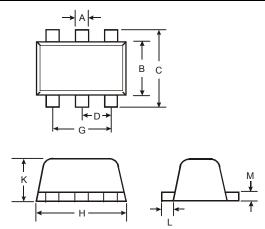


Fig. 20 Typical Capacitance

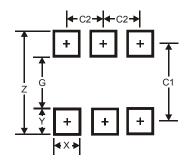


# **Package Outline Dimensions**



	SO	T563	
Dim	Min	Max	Тур
Α	0.15	0.30	0.20
в	1.10	1.25	1.20
С	1.55	1.70	1.60
D	-	-	0.50
G	0.90	1.10	1.00
Н	1.50	1.70	1.60
Κ	0.55	0.60	0.60
L	0.10	0.30	0.20
Μ	0.10	0.18	0.11
All	Dimens	sions in	mm

# Suggested Pad Layout



Dimensions	Value (in mm)
Z	2.2
G	1.2
Х	0.375
Y	0.5
C1	1.7
C2	0.5



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