

November 2013

FDB5800

N-Channel Logic Level PowerTrench® MOSFET 60 V, 80 A, 6 m Ω

Features

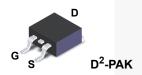
- $R_{DS(on)}$ = 4.6 m Ω (Typ.), V_{GS} = 10 V, I_D = 80 A
- High Performance Trench Technology for Extermly Low $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$
- · Low Gate Charge
- · High Power and Current Handing Capability
- · RoHs Compliant

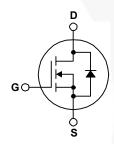
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Power tools
- · Motor drives and Uninterruptible Power Supplies





Absolute Maximum Ratings T_c = 25°C unless otherwise noted.

Symbol	Parameter		FDB5800	Unit
V _{DSS}	Drain to Source Voltage		60	V
V_{GS}	Gate to Source Voltage		±20	V
	Drain Current - Continuous (T _C < 102°C, V _{GS} = 10 V)		80	А
I _D	- Continuous (T_C < 90° C, V_{GS} = 5 V)		80	Α
	- Continuous (T_{amb} = 25°C, V_{GS} = 10V, with $R_{\theta JA}$ = 43°C/W)		14	Α
	- Pulsed		Figure 4	Α
E _{AS}	Single Pulse Avalanche Energy (Not	te 1)	652	mJ
	- Power Dissipation		242	W
P_{D}	- Derate above 25°C		1.61	W/°C
T _J , T _{STG}	- Operating and Storage Temperature		-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-263, Max.	0.62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, Max. (Note 2)	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in ² copper pad area	43	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB5800	FDB5800	D ² -PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Parameter Test Conditions		Тур.	Max.	Unit
Off Char	racteristics					
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60	-	-	V
1	Zero Gate Voltage Drain Current	V _{DS} = 48 V	-	-	1	μА
DSS	Zelo Gale Vollage Dialii Culient	$V_{GS} = 0 V$ $T_{C} = 150^{\circ}C$	-	-	250	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$	-	-	±100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1.0	-	2.5	V
r _{DS(ON)}		I _D = 80 A, V _{GS} = 10 V	-	4.6	6.0	-
		$I_D = 80 \text{ A}, V_{GS} = 4.5 \text{ V}$	-	5.8	7.2	
	Drain to Source On Resistance	I _D = 80 A, V _{GS} = 5 V	•	5.5	7.0	mΩ
		$I_D = 80 \text{ A}, V_{GS} = 10 \text{ V},$ $T_1 = 175^{\circ}\text{C}$	-	10	12.6	
		1j = 170 O				

Dynamic Characteristics

C _{ISS}	Input Capacitance	V -45 V V -0 V	-	6625	-	pF
C _{OSS}	Output Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	- \	628	-	pF
C _{RSS}	Reverse Transfer Capacitance	1 - 1 1011 12	-	262	-	pF
R_G	Gate Resistance	$V_{GS} = 0.5 V, f = 1 MHz$	1	1.4		Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V _{GS} = 0 V to 10 V	-	104	135	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V _{GS} = 0 V to 5 V	-	55	72	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ V to 1 V}$ $V_{DD} = 30 \text{ V}$ $I_{D} = 80 \text{ A}$	-	6.0	-	nC
Q_{gs}	Gate to Source Gate Charge	$I_0 = 30 \text{ A}$	-	18.4	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	.g	-	12.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		1	20.1		nC

Switching Characteristics $(V_{GS} = 5V)$

t _{ON}	Turn-On Time		- /	-	62.1	ns
t _{d(ON)}	Turn-On Delay Time		-/	20.3	-	ns
t _r	Rise Time	V _{DD} = 30 V, I _D = 80 A	-	22.0	-	ns
t _{d(OFF)}	Turn-Off Delay Time	$V_{GS} = 5 \text{ V}, R_{GS} = 2 \Omega$	-	27.1	- 9	ns
t _f	Fall Time		-	12.1	-/	ns
t _{OFF}	Turn-Off Time		-	-	59.0	ns

Drain-Source Diode Characteristics

V _{SD} Source to Drain Diode Voltage	Source to Drain Diode Voltage	I _{SD} = 80 A	ı	-	1.25	V
	Source to Drain Diode Voltage	I _{SD} = 40 A	-	-	1.0	V
t _r	Reverse Recovery Time	$I_{SD} = 60 \text{ A}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}$	-	-	44	ns
$Q_{_{\rm SD}}$	Reverse Recovered Charge	I_{SD} = 60 A, dI_{SD}/dt = 100 A/ μ s	ı		57	nC

Notes: 1: Starting T_J = 25°C, L = 1mH, I_{AS} = 36A, V_{DD} = 54V, V_{GS} = 10V. 2: Pulse width = 100s.

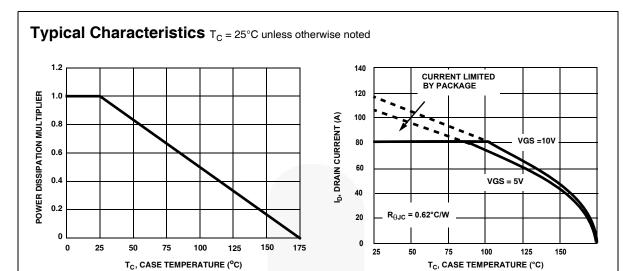


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

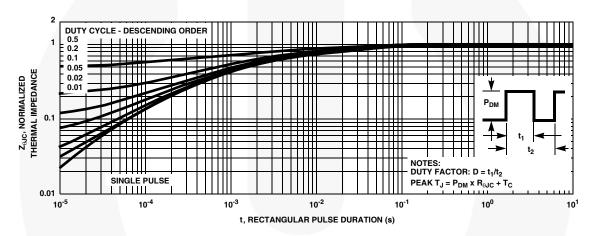


Figure 3. Normalized Maximum Transient Thermal Impedance

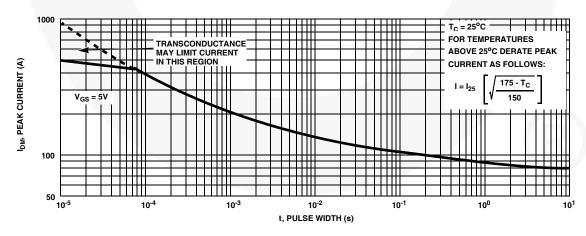


Figure 4. Peak Current Capability



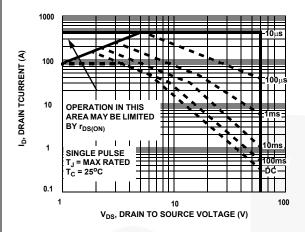
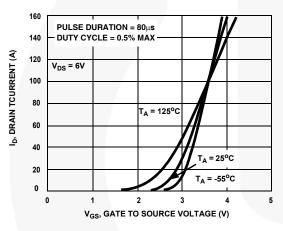


Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability



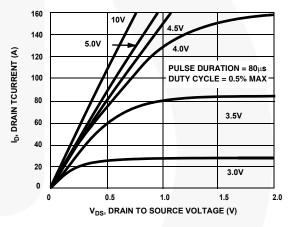
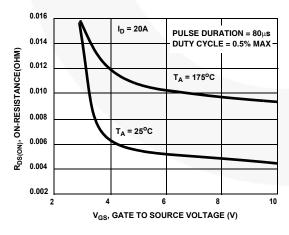


Figure 7. Transfer Characteristics

Figure 8. Saturation Characteristics



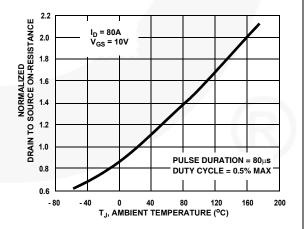


Figure 9. On-Resistance Variation vs Gate-to-

Figure 10. Normalized Drain to Source On

Typical Characteristics T_C = 25°C unless otherwise noted

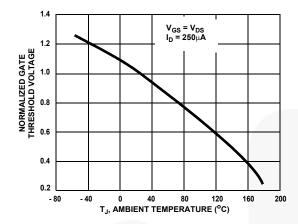


Figure 11. Normalized Gate Threshold Voltage vs
Junction Temperature

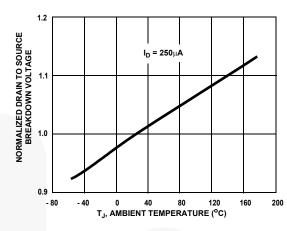


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

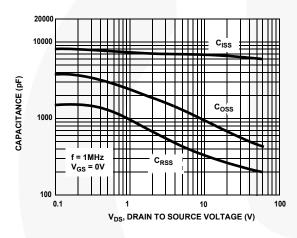


Figure 13. Capacitance vs Drain to Source Voltage

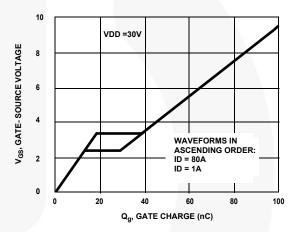


Figure 14. Gate Charge Waveforms for Constant Gate Current

Mechanical Dimensions

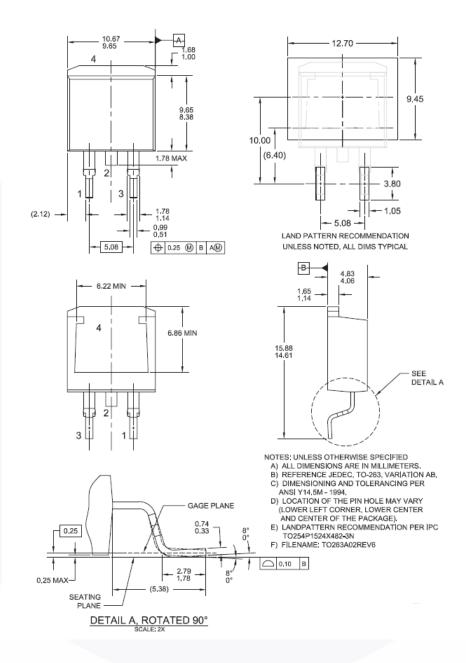


Figure 15. TO263 (D²PAK), Molded, 2-Lead, Surface Mount

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