June 2016

FDMD8900

N-Channel PowerTrench® MOSFET

Q1: 30 V, 66 A, 4 mΩ   Q2: 30 V, 42 A, 5.5 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 4 mΩ at V_{GS} = 10 V, I_D = 19 A
- Max $r_{DS(on)}$ = 5 mΩ at V_{GS} = 4.5 V, I_D = 17 A
- Max $r_{DS(on)}$ = 6.5 mΩ at V_{GS} = 3.8 V, I_D = 15 A
- Max $r_{DS(on)}$ = 8.3 mΩ at V_{GS} = 3.5 V, I_D = 14 A

Q2: N-Channel

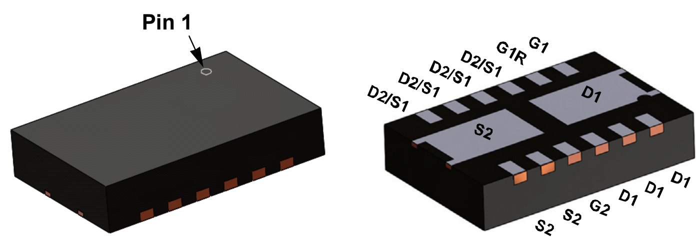
- Max $r_{DS(on)}$ = 5.5 mΩ at V_{GS} = 10 V, I_D = 17 A
- Max $r_{DS(on)}$ = 6.5 mΩ at V_{GS} = 4.5 V, I_D = 15 A
- Max $r_{DS(on)}$ = 9 mΩ at V_{GS} = 3.8 V, I_D = 13 A
- Max $r_{DS(on)}$ = 12 mΩ at V_{GS} = 3.5 V, I_D = 12 A
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- Termination is Lead-free and RoHS Compliant
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability

General Description

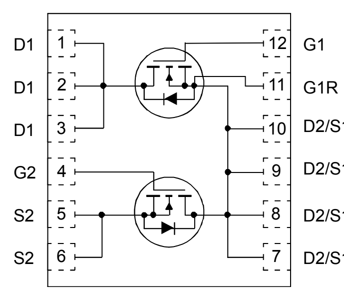
This devices utilizes two optimized N-ch FETs in a dual 3.3x5mm thermally enhanced power package. The HS Source and LS drain are internally connected providing a low source inductance package, helping to provide the best FOM.

Applications

- Computing
- Buck, Boost and Buck/Boost Applications
- General Purpose POL



Power 3.3 x 5



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage	±12	±12	V
I_D	Drain Current -Continuous T_C = 25 °C (Note 5)	66	42	A
	-Continuous T_C = 100°C (Note 5)	42	26	
	-Continuous T_A = 25 °C (Note 1a)	19	17	
	-Pulsed (Note 4)	280	210	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	73	54	mJ
P_D	Power Dissipation T_C = 25 °C	27	15	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.1		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

Symbol	Parameter	Q1	Q2	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.7	8.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60		

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8900	FDMD8900	Power 3.3 x 5	13 ”	12 mm	3000 units

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Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 250 μA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 250 μA, referenced to 25 °C	Q1 Q2	14 13			mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12 V, V_{DS}= 0 V V_{GS} = ±12 V, V_{DS}= 0 V	Q1 Q2			±100 ±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 250 μA	Q1 Q2	0.8 1	1.3 1.4	2.5 2.5	mV
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 250 μA, referenced to 25 °C	Q1 Q2	-4 -4			mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 19 A V_{GS} = 4.5 V, I_D = 17 A V_{GS} = 3.8 V, I_D = 15 A V_{GS} = 3.5 V, I_D = 14 A V_{GS} = 10 V, I_D = 19 A,T_J =125 °C	Q1		3.4 4 4.3 4.6 4.6	4 5 6.5 8.3 6	mΩ
		V_{GS} = 10 V, I_D = 17 A V_{GS} = 4.5 V, I_D = 15 A V_{GS} = 3.8 V, I_D = 13 A V_{GS} = 3.5 V, I_D = 12 A V_{GS} = 10 V, I_D = 17 A ,T_J =125 °C	Q2		4.5 5.4 6 6.6 5.8	5.5 6.5 9 12 6.9	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 19 A V_{DS} = 5 V, I_D = 17 A	Q1 Q2		86 80		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1735 1210	2605 1815	pF
C_{oss}	Output Capacitance		Q1 Q2		462 356	695 535	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		47 52	75 80	pF
R_g	Gate Resistance		Q1 Q2		0.8 1.9		Ω

Switching Characteristics

Symbol	Parameter	Test Conditions		Type	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 15 V, I_D = 19 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 17 A, R_{GEN} = 6 Ω		Q1 Q2		8.7 7.1	17 14	ns
t_r	Rise Time			Q1 Q2		2.3 2	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time			Q1 Q2		25 22	40 35	ns
t_f	Fall Time			Q1 Q2		2.4 2.3	10 10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1: V_{DD} = 15 V, I_D = 19 A Q2: V_{DD} = 15 V, I_D = 17 A	Q1 Q2		25 19	35 27	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V		Q1 Q2		12 8.8	17 12	nC
Q_{gs}	Gate to Source Gate Charge			Q1 Q2		3.6 2.7		nC
Q_{gd}	Gate to Drain "Miller" Charge			Q1 Q2		2.7 2.6		nC

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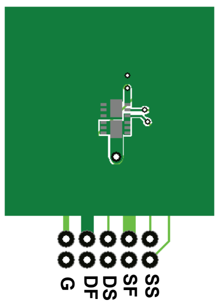
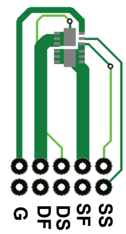
Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 19 A (Note 2) V_{GS} = 0 V, I_S = 17 A (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1: I_F = 19 A, di/dt = 100 A/μs	Q1 Q2		26 22	42 35	ns
Q_{rr}	Reverse Recovery Charge	Q2: I_F = 17 A, di/dt = 100 A/μs	Q1 Q2		10 7.8	20 16	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 130 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Q1: E_{AS} of 73 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 7 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 25 A.
   Q2: E_{AS} of 54 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 6 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 20 A.
4. Pulse Id refers to Figure "Forward Bias Safe Operation Area".
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

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Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

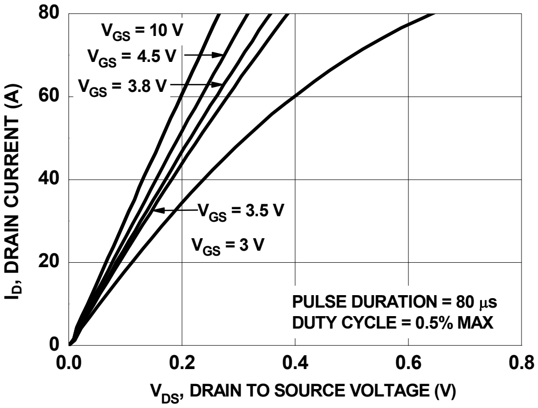


Figure 1. On-Region Characteristics

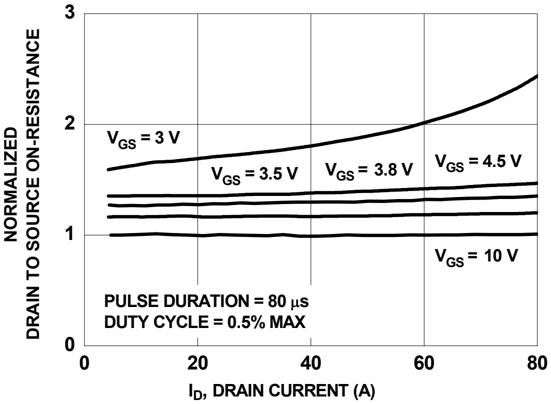


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

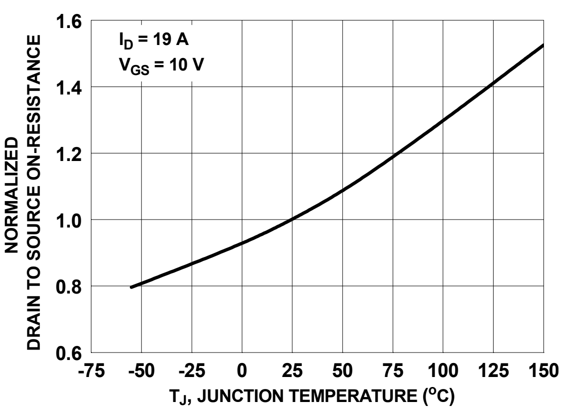


Figure 3. Normalized On Resistance vs. Junction Temperature

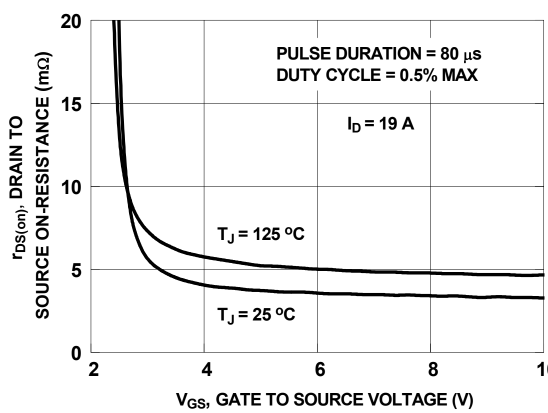


Figure 4. On Resistance vs. Gate to Source Voltage

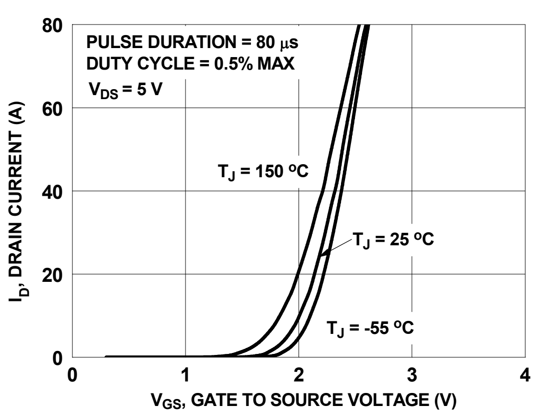


Figure 5. Transfer Characteristics

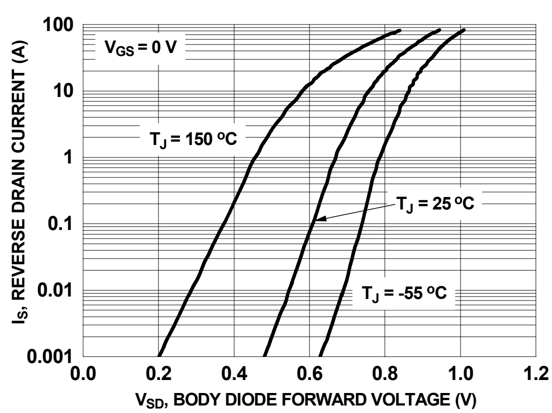


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

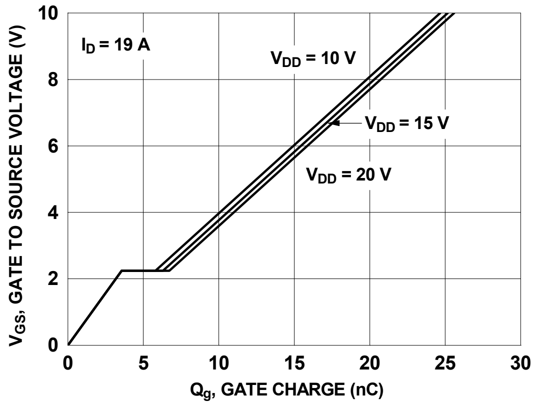


Figure 7. Gate Charge Characteristics

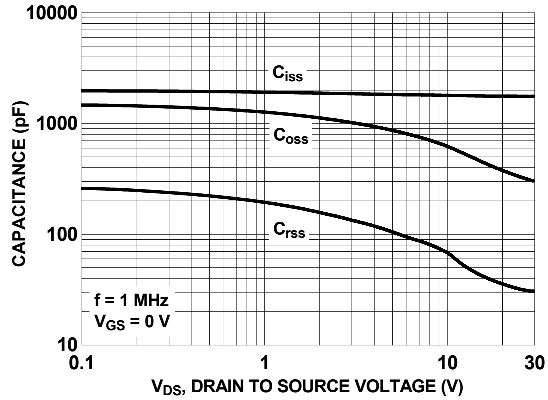


Figure 8. Capacitance vs. Drain to Source Voltage

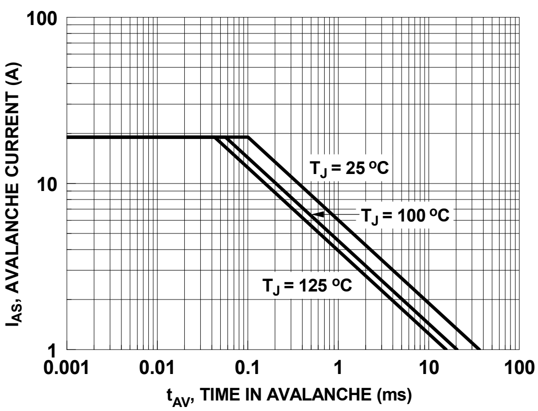


Figure 9. Unclamped Inductive
Figure 10. Switching Capability

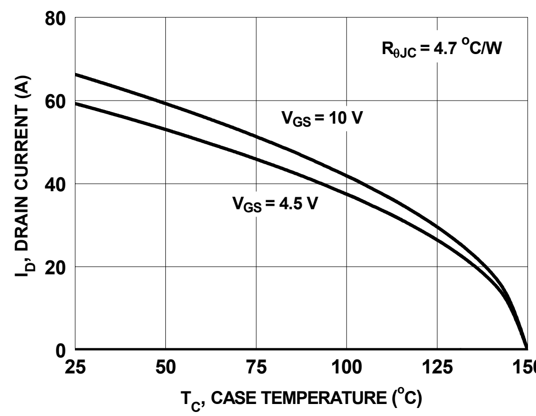


Figure 11. Maximum Continuous Drain Current vs. Case Temperature

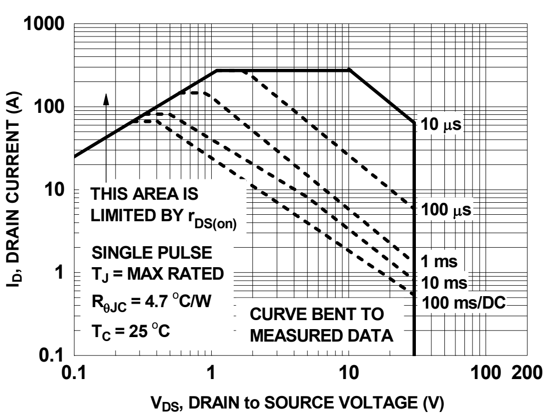


Figure 12. Forward Bias Safe Operating Area

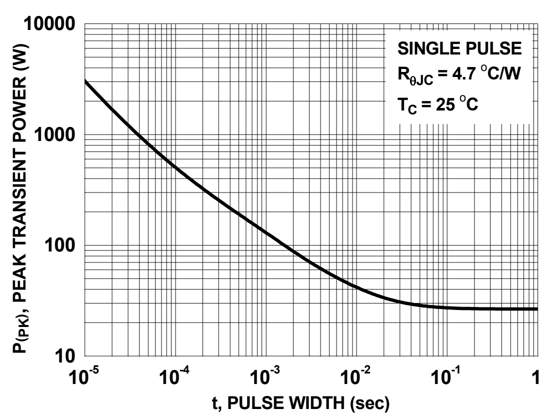


Figure 13. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

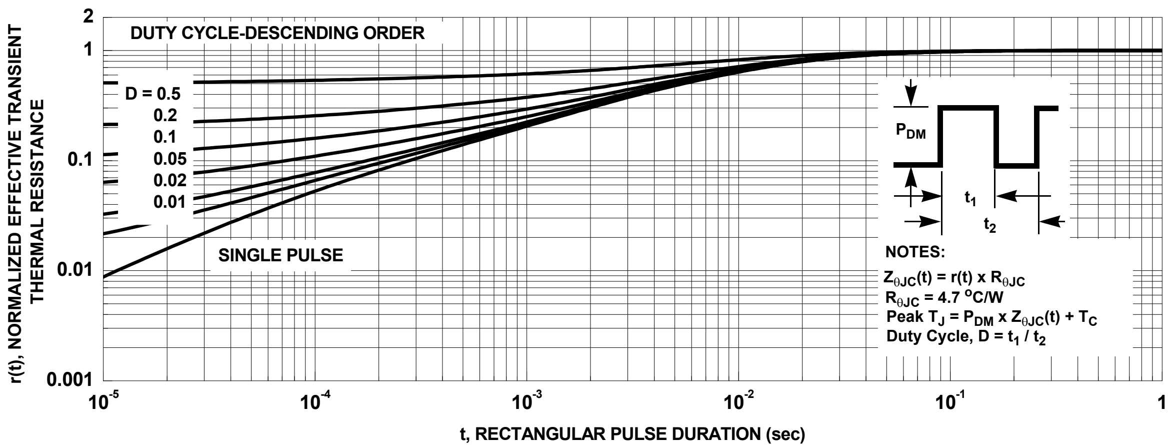


Figure 14. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

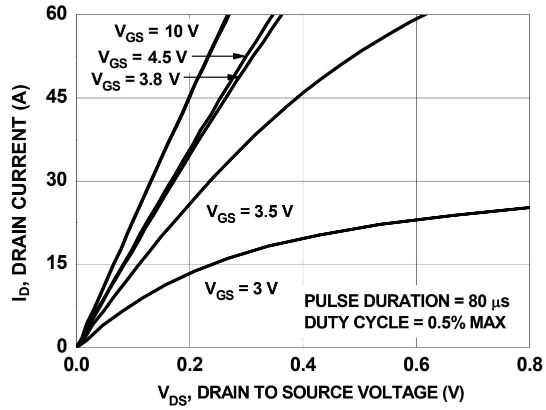


Figure 14. On- Region Characteristics

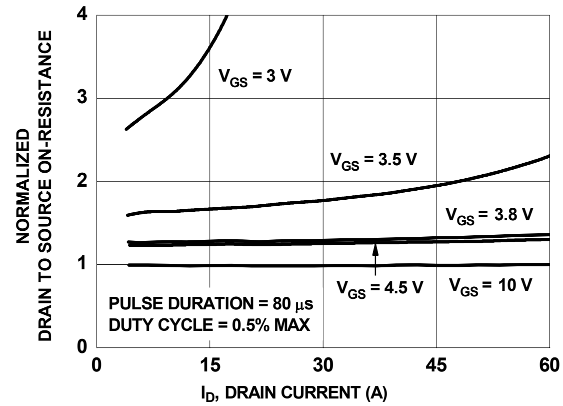


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

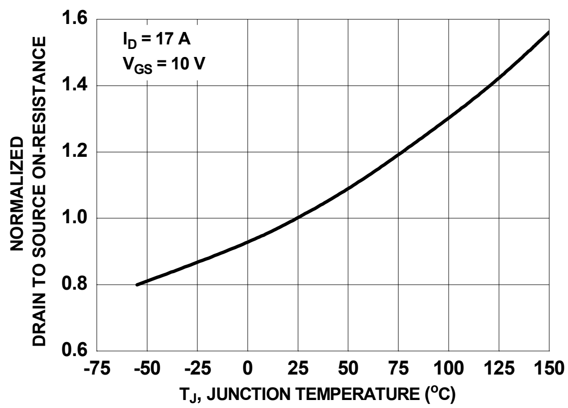


Figure 16. Normalized On-Resistance vs. Junction Temperature

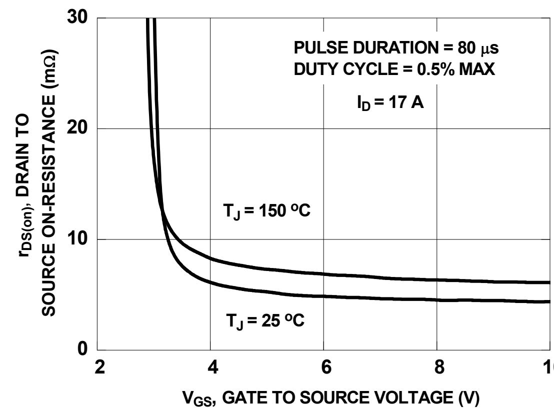


Figure 17. On-Resistance vs. Gate to Source Voltage

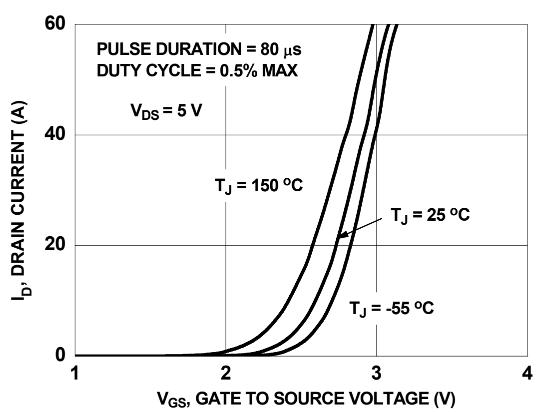


Figure 18. Transfer Characteristics

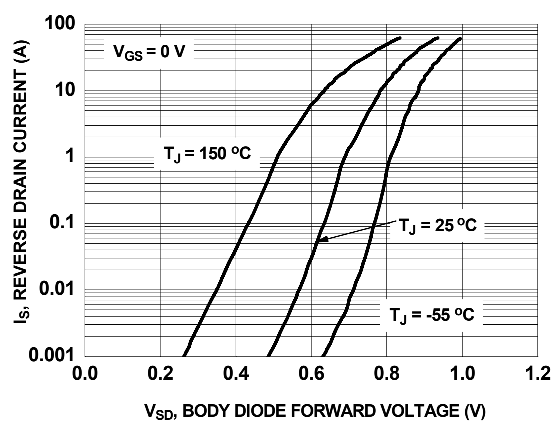


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted.

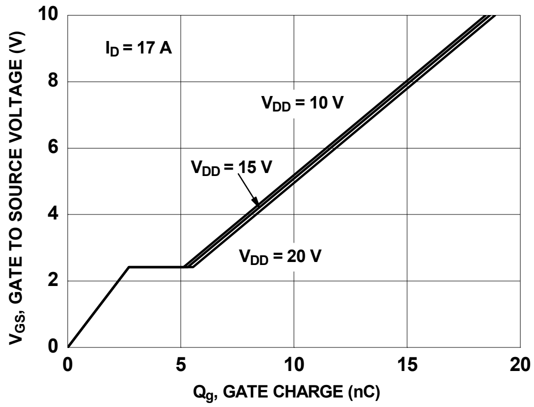


Figure 20. Gate Charge Characteristics

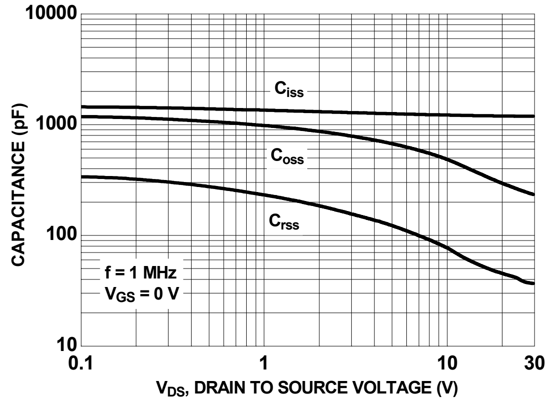


Figure 21. Capacitance vs. Drain to Source Voltage

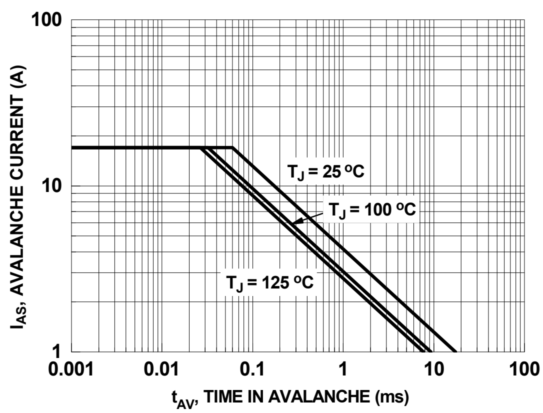


Figure 22. Unclamped Inductive Switching Capability

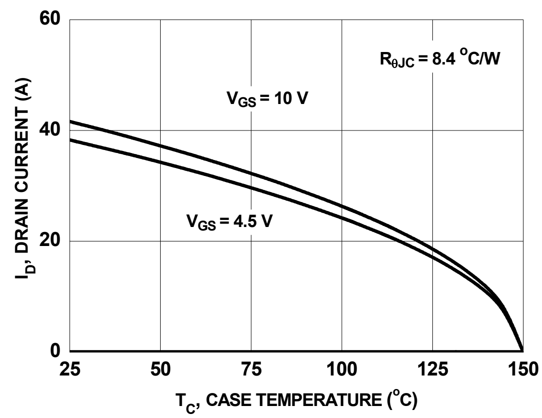


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

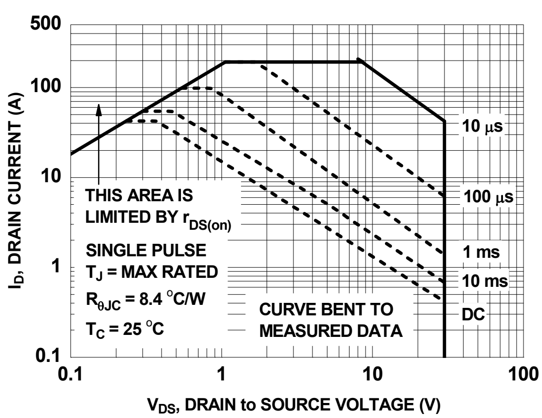


Figure 24. Forward Bias Safe Operating Area

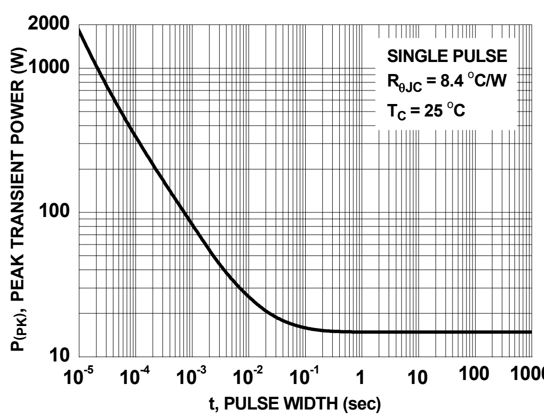


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

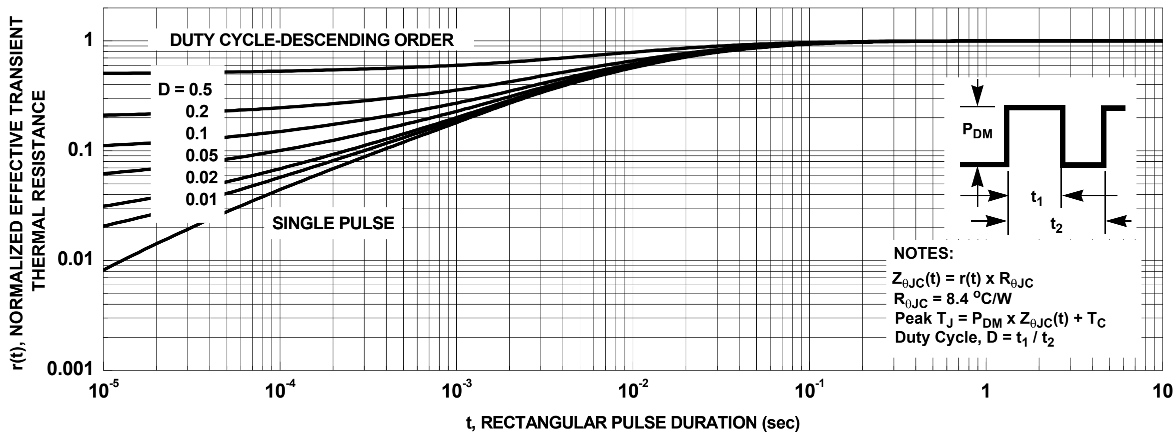
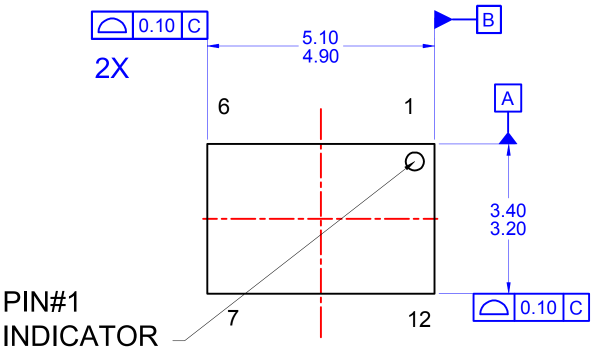
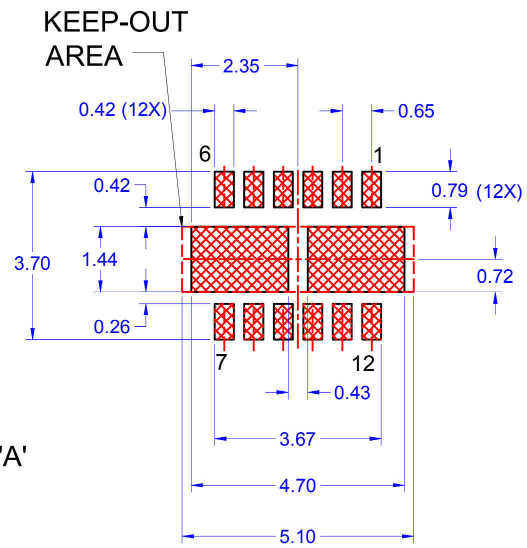


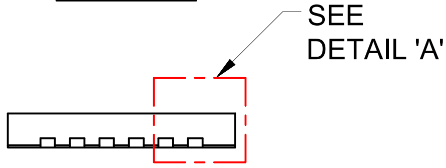
Figure 26. Junction-to-Case Transient Thermal Response Curve



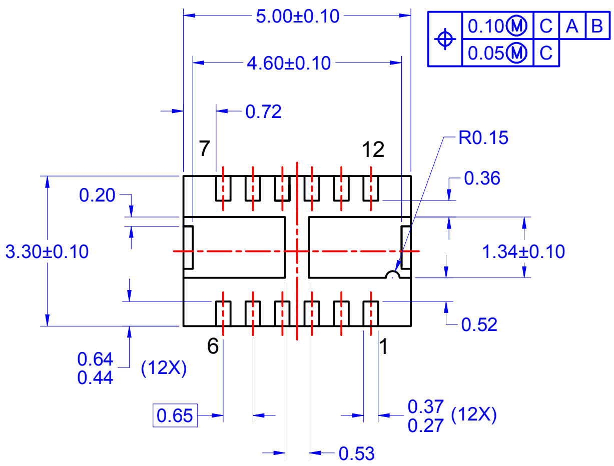
TOP VIEW



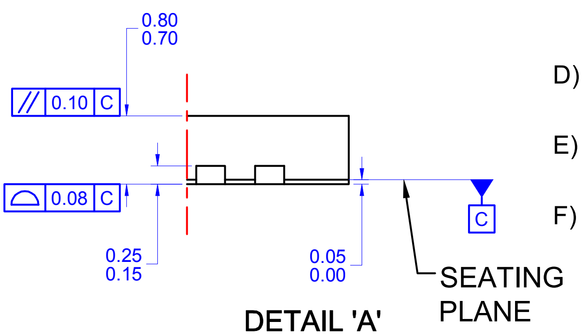
LAND PATTERN RECOMMENDATION



FRONT VIEW



BOTTOM VIEW



DETAIL 'A'

SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229 DATED 8/2012

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: MKT-PQFN12BREV1

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MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
MotionGrid®
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SuperSOT™-6
SuperSOT™-8
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TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
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Definition of Terms

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