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November 2013
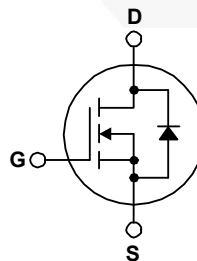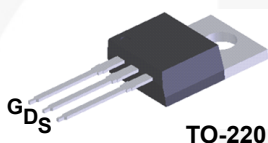
FQP13N50

N-Channel QFET® MOSFET

500 V, 12.5 A, 430 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 12.5 A, 500 V, $R_{DS(on)}$ = 430 mΩ (Max.) @ V_{GS} = 10 V, I_D = 6.25 A

- Low Gate Charge (Typ. 45 nC)

- Low Crss (Typ. 25 pF)

- 100% Avalanche Tested

TO-220

D

G

S

Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FQP13N50	Unit
V_{DSS}	Drain-Source Voltage			500	V
I_D	Drain Current	- Continuous (T_C = 25°C)		12.5	A
		- Continuous (T_C = 100°C)		7.9	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	50	A
V_{GSS}	Gate-Source Voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	810	mJ
I_{AR}	Avalanche Current		(Note 1)	12.5	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	17	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)			170	W
	- Derate above 25°C			1.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FQP13N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.74	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Max.	0.5	°C/W

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP13N50	FQP13N50	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.48	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 6.25 A	--	0.33	0.43	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 6.25 A	--	10	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1800	2300	pF
C_{oss}	Output Capacitance		--	245	320	pF
C_{rss}	Reverse Transfer Capacitance		--	25	35	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 13.4 A, R_G = 25 Ω	--	40	90	ns
t_r	Turn-On Rise Time		--	140	290	ns
$t_{d(off)}$	Turn-Off Delay Time		--	100	210	ns
t_f	Turn-Off Fall Time	(Note 4)	--	85	180	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 13.4 A, V_{GS} = 10 V	--	45	60	nC
Q_{gs}	Gate-Source Charge		--	11	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	22	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	12.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	50	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 12.5 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 13.4 A, dI_F / dt = 100 A/µs	--	290	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.6	--	µC

Notes:
1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 9.3 mH, I_{AS} = 12.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 13.4 A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature.
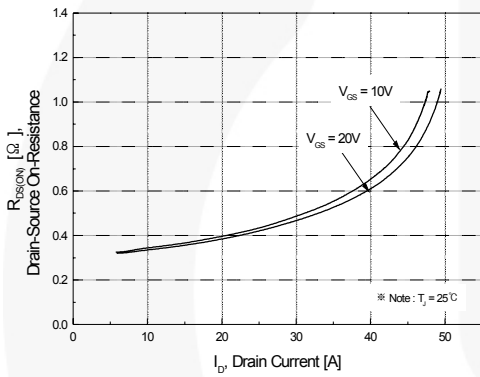
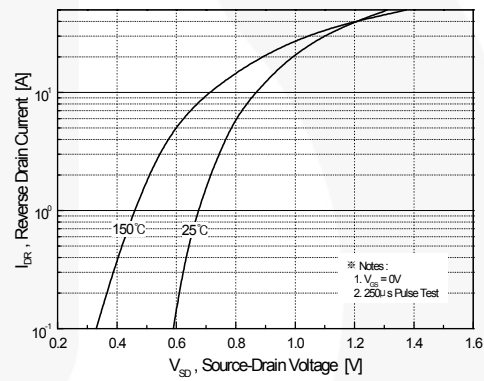FQP13N50 — N-Channel QFET® MOSFET

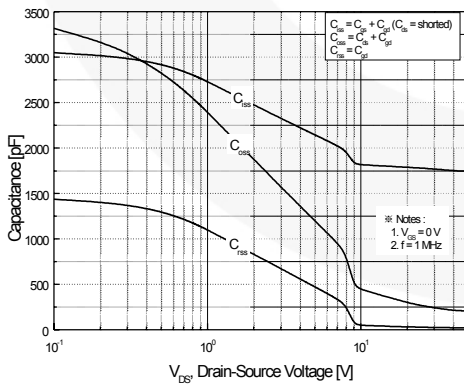## Typical Characteristics
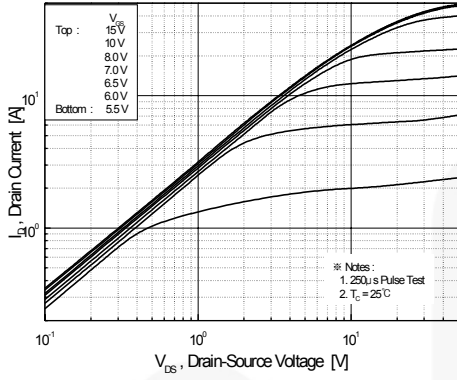
Figure 1. On-Region Characteristics
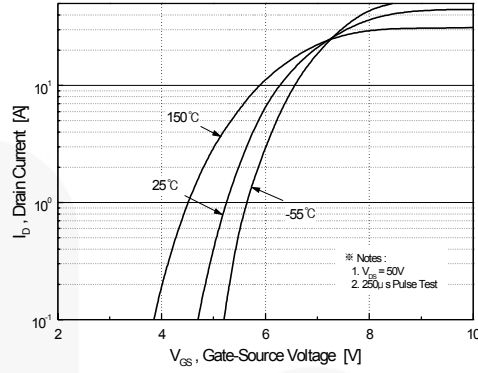
Figure 2. Transfer Characteristics
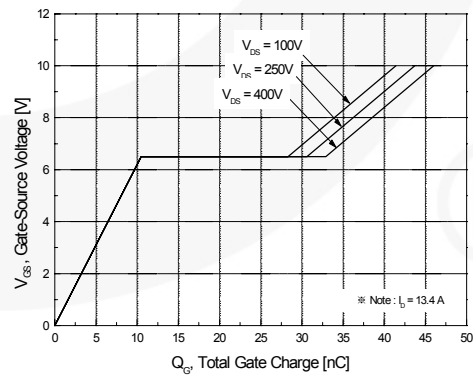

Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage
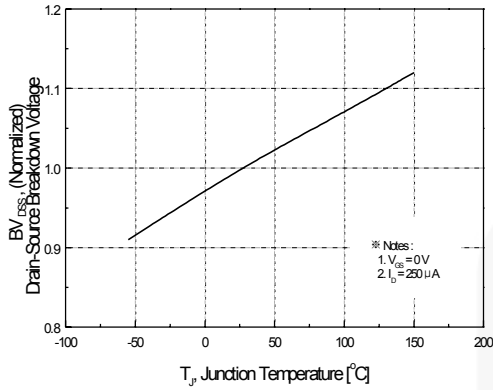Variation vs. Source Current
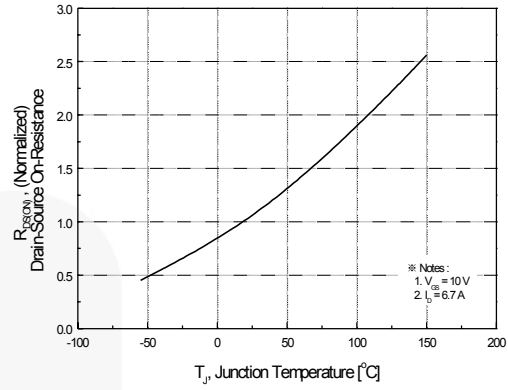and Temperature

Figure 5. Capacitance Characteristics

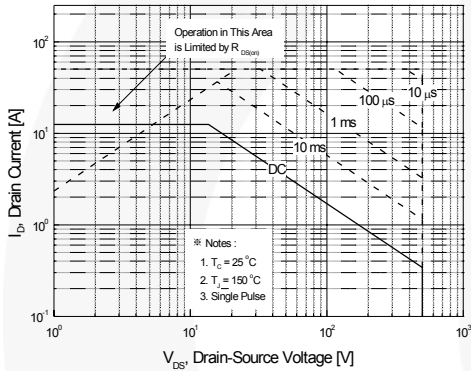Figure 6. Gate Charge Characteristics

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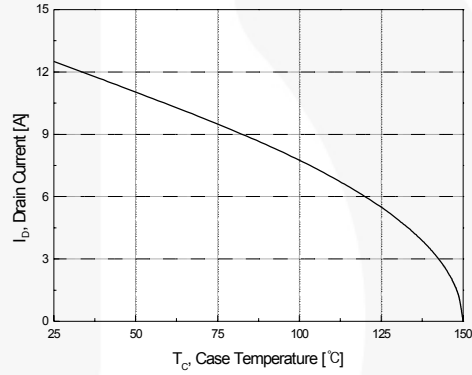
Typical Characteristics (Continued)

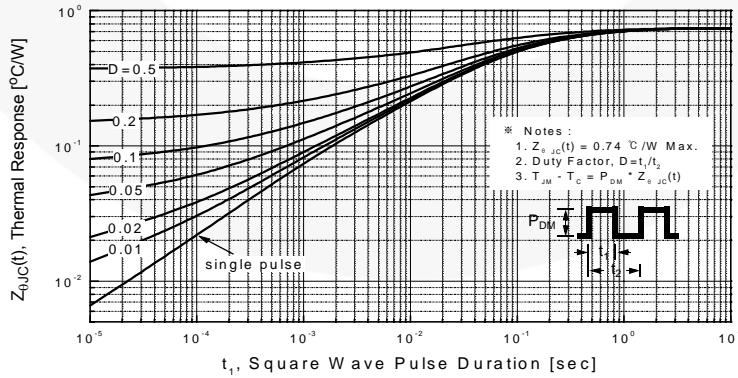**Figure 7. Breakdown Voltage Variation vs. Temperature**

Figure 8. On-Resistance Variation vs. Temperature

Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

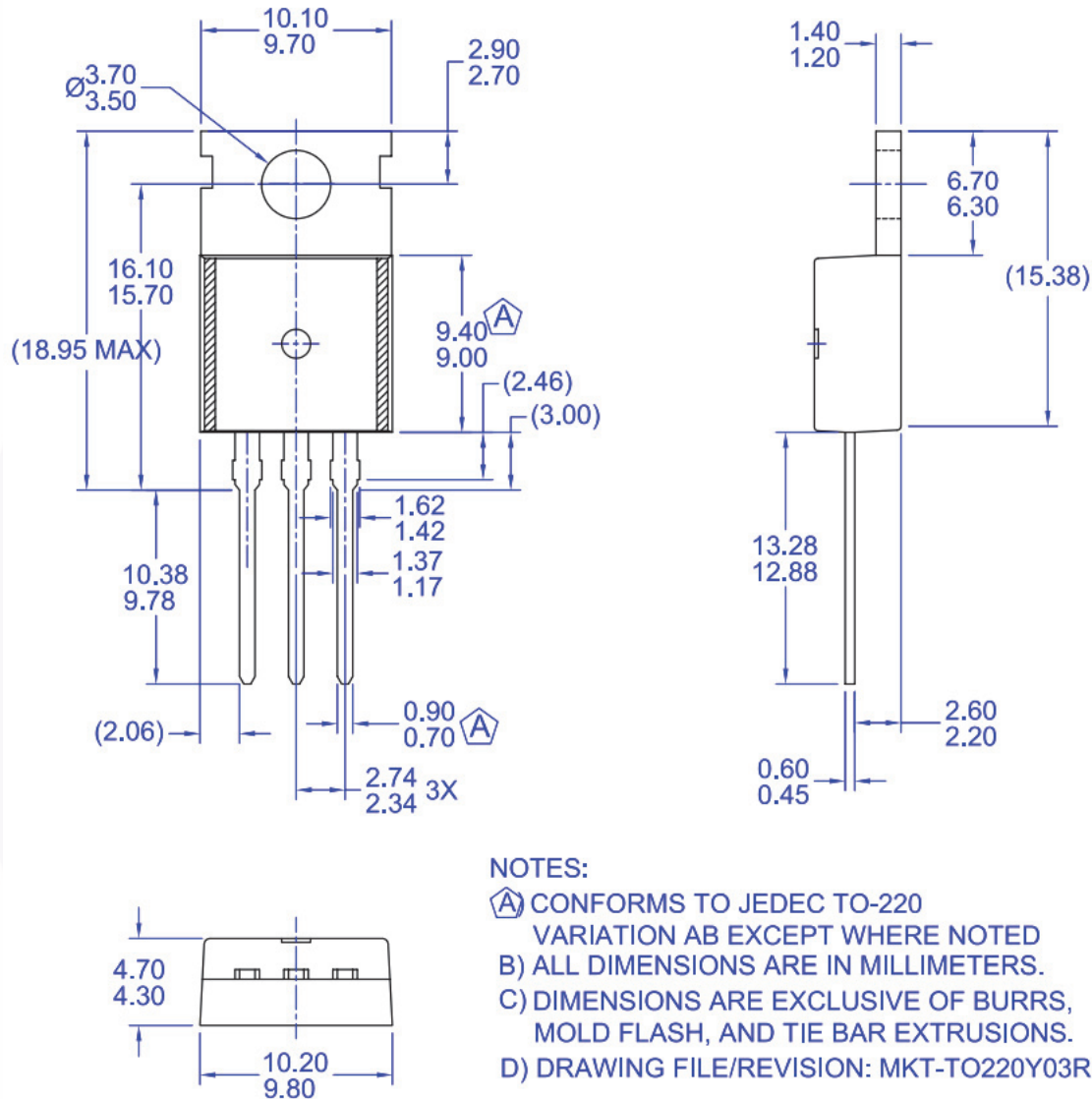**Figure 13. Resistive Switching Test Circuit & Waveforms**

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \quad \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FQP13N50 Rev. C1

5

DUT

V_{DS}

+

−

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

6

Mechanical Dimensions

Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

NOTES:
A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

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Rev. I66

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