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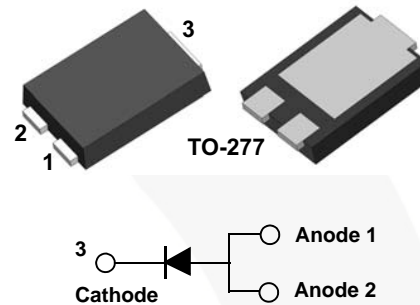
July 2015

FSV15120V

15 A, 120 V Ultra-Low VF Schottky Rectifier

Features

- Ultra-Low Forward Voltage Drop
- Low Thermal Resistance
- Very Low Profile: Typical Height of 1.1 mm
- Trench Schottky Technology
- RoHS Compliant
- Green Molding Compound as per IEC61249 Standard
- Lead Free in Compliance with EU RoHS 2011/65/EU Directive
- Qualified per AEC-Q101 Rev. C Standard



Ordering Information

Part Number	Top Mark	Package	Packing Method
FSV15120V	FSV15120V	TO-277 3L	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{RRM}	Peak Repetitive Reverse Voltage	120	V
V_{RWM}	Working Peak Reverse Voltage	120	V
V_{RMS}	RMS Reverse Voltage	85	V
V_R	DC Blocking Voltage	120	V
$I_{F(AV)}$	Average Rectified Peak Forward Surge Current	15	A
I_{FSM}	Non-Repetitive Peak Forward Surge Current	250	A
T_J	Operating Junction Temperature Range	-55 to +150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to +150	$^\circ\text{C}$

FSV15120V — 15 A, 120 V Ultra-Low VF Schottky Rectifier

Thermal Characteristics⁽¹⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Minimum Land Pattern	Maximum Land Pattern	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	100	40	$^\circ\text{C}/\text{W}$
Ψ_{JL}	Junction-to-Lead Thermal Characteristics, Thermocouple Soldered to Anode	15	12	$^\circ\text{C}/\text{W}$
	Junction-to-Lead Thermal Characteristics, Thermocouple Soldered to Cathode	6	5	

Note:

- The thermal resistances ($R_{\theta JA}$ & Ψ_{JL}) are characterized with device mounted on the following FR4 printed circuit boards, as shown in Figure 1 and Figure 2. PCB size: 76.2 x 114.3 mm. Minimum land pattern size: 4.9 x 4.8 mm (big pattern, x1), 1.4 x 1.52 mm (small pattern, x2). Maximum land pattern size: 30 x 30 mm (pattern, x2). Force line trace size = 55 mils, sense line trace size = 4 mils.



Figure 1. Minimum Land Pattern of 2 oz Copper

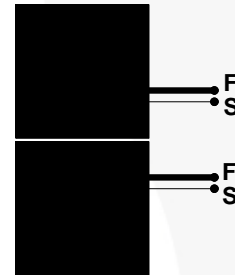


Figure 2. Maximum Land Pattern of 2 oz Copper

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_R	Breakdown Voltage	$I_R = 0.5 \text{ mA}$	120			V
V_F	Forward Voltage Drop	$I_F = 15 \text{ A}$		0.741	0.790	V
I_R	Reverse Current	$V_R = 120 \text{ V}$		7.7	35	μA

Typical Performance Characteristics

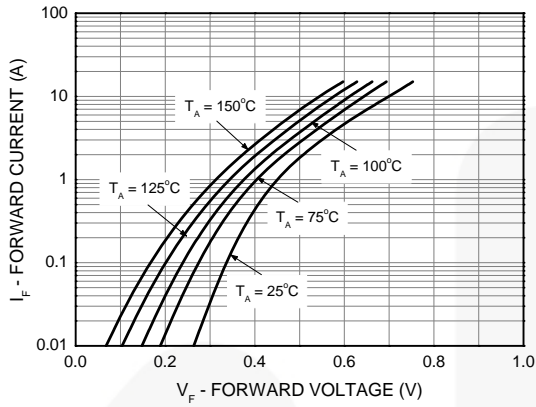


Figure 3. Typical Forward Characteristics

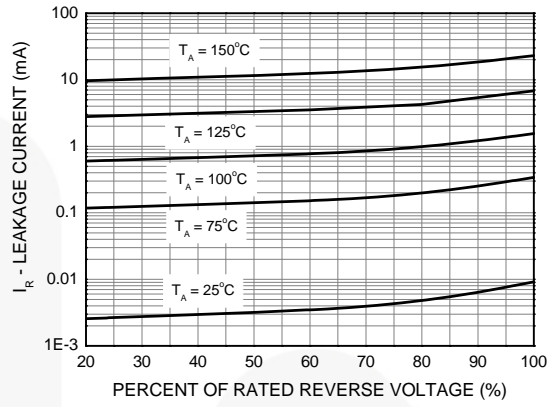


Figure 4. Typical Reverse Characteristics

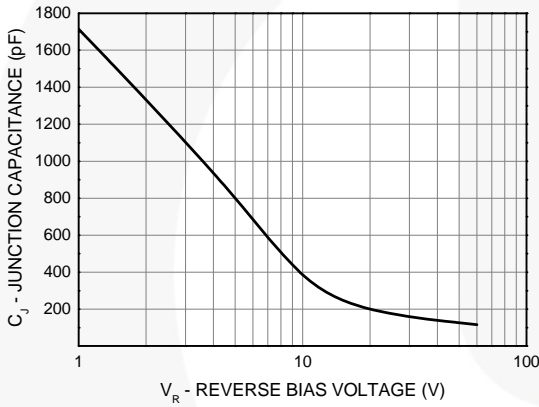


Figure 5. Typical Junction Capacitance

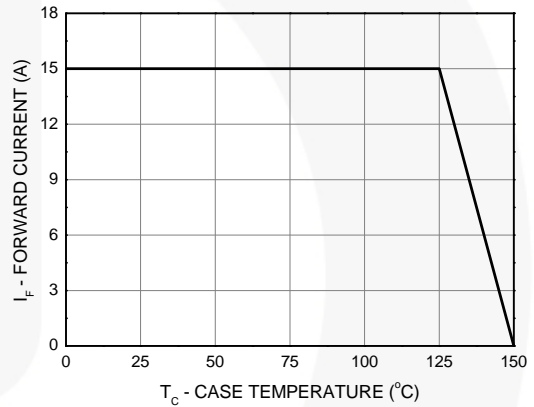


Figure 6. Forward Current Derating Curve



TOP VIEW



LAND PATTERN RECOMMENDATION

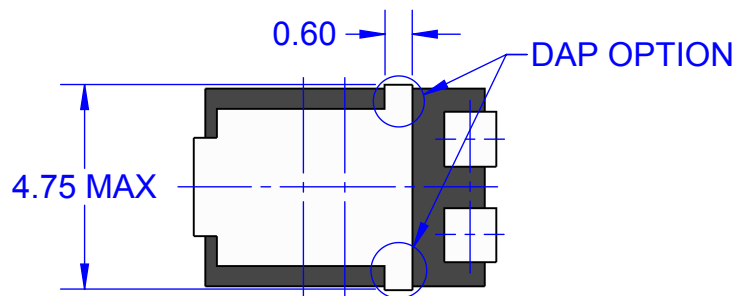


FRONT VIEW



BOTTOM VIEW

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- A. PACKAGE REFERENCE: JEDEC TO-277
 - B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - C. ALL DIMENSIONS ARE IN MILLIMETERS.
 - D. DOES NOT COMPLY TO JEDEC STANDARD VALUE.
 - E. DRAWING FILENAME: MKT-TO277A03rev5








BOTTOM VIEW - DAP OPTION





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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