October 1996



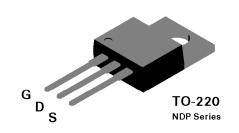
NDP5060L / NDB5060L N-Channel Logic Level Enhancement Mode Field Effect Transistor

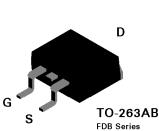
General Description

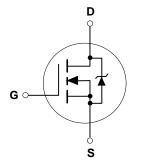
These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







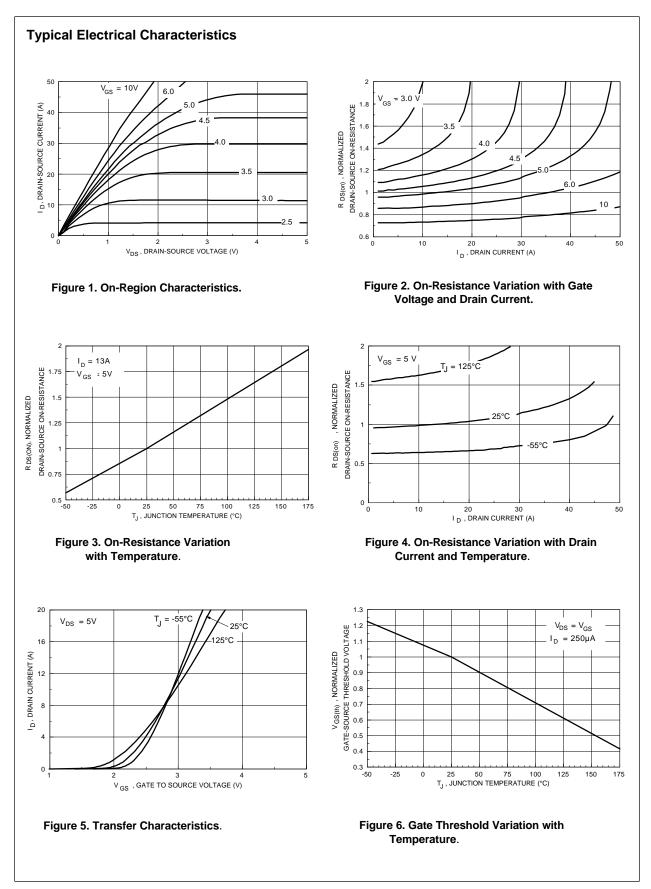
Absolute Maximum Ratings T_c = 25°C unless otherwise noted

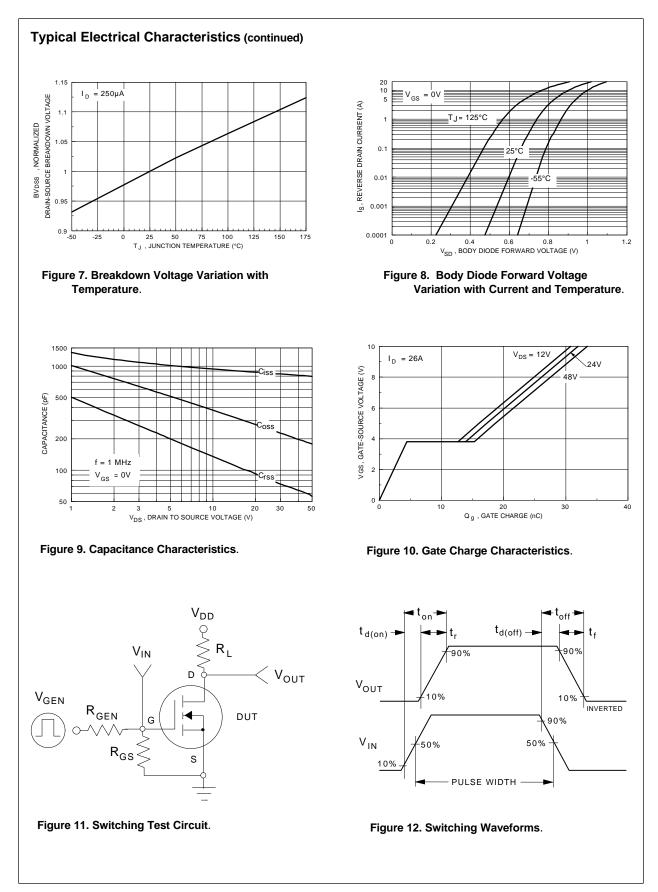
Symbol	Parameter	NDP5060L	NDB5060L	Units	
V _{DSS}	Drain-Source Voltage	60		V	
V_{DGR}	Drain-Gate Voltage ($R_{GS} \le 1 M\Omega$)	60		V	
V_{GSS}	Gate-Source Voltage - Continuous	±16		V	
	- Nonrepetitive ($t_p < 50 \ \mu s$)	±25			
I _D	Drain Current - Continuous 26		26	А	
	- Pulsed	78			
P _D	Total Power Dissipation @ $T_c = 25^{\circ}C$	6	68		
	Derate above 25°C	0.	W/°C		
TJ,TSTG	Operating and Storage Temperature Range	-65 t	o 175	°C	

Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)						
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 30 V, I _D = 26 A				100	mJ
I _{AR}	Maximum Drain-Source Avalanche Curre	ent				26	А
OFF CH/	ARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$		60			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{\rm DS} = 60 \text{ V}, V_{\rm GS} = 0 \text{ V}$				250	μA
			T _J = 125°C			1	mA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$	·			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$				-100	nA
ON CHA	RACTERISTICS (Note 1)						
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		1	1.4	2	V
			T _J = 125°C	0.65	1	1.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 5 \text{ V}, I_{D} = 13 \text{ A}$	·		0.042	0.05	Ω
			T _J = 125°C		0.07	0.08	
		$V_{GS} = 10 \text{ V}, I_{D} = 13 \text{ A}$	·		0.031	0.035	ľ
I _{D(on)}	On-State Drain Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$		26			А
9 _{FS}	Forward Transconductance	$V_{\rm DS} = 10 \text{ V}, \text{ I}_{\rm D} = 13 \text{ A}$			16		S
DYNAMI	C CHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			840		pF
C _{oss}	Output Capacitance				230		pF
C _{rss}	Reverse Transfer Capacitance				75		pF
SWITCHI	NG CHARACTERISTICS (Note 1)						
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 30 \text{ V}, \ I_{D} = 26 \text{ A}, \\V_{GS} = 5 \text{ V}, \ R_{GEN} = 30 \Omega \\R_{GS} = 30 \Omega$			13	20	nS
t,	Turn - On Rise Time				200	400	nS
t _{D(off)}	Turn - Off Delay Time				45	80	nS
t _f	Turn - Off Fall Time				102	200	nS
Q _g	Total Gate Charge	$V_{DS} = 24 V,$ $I_{D} = 26 A, V_{GS} = 5 V$			17	24	nC
Q _{gs}	Gate-Source Charge				4		nC
Q _{gd}	Gate-Drain Charge				10		nC

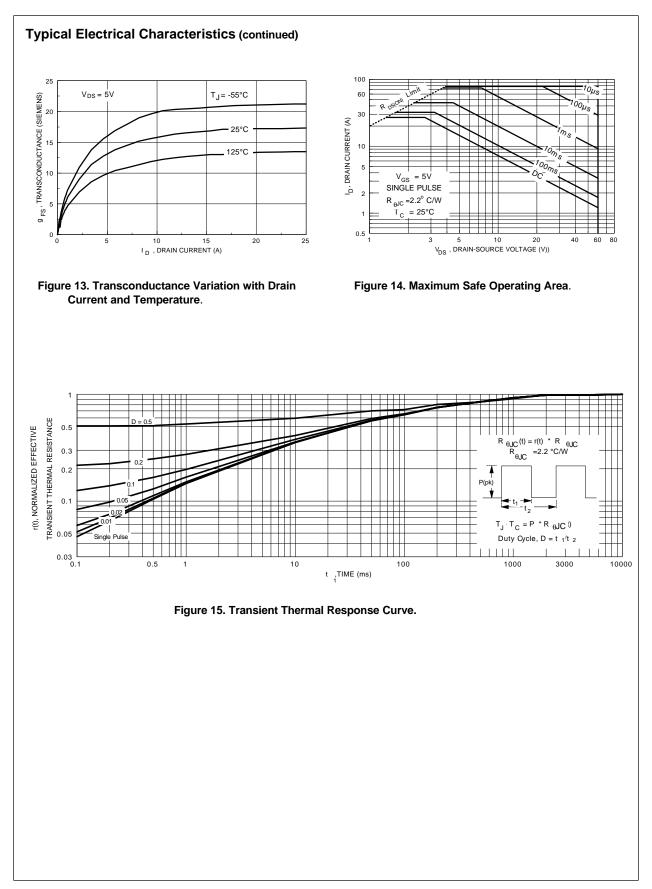
Electrical Characteristics (T _c = 25°C unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS		•			
I _s	Maximum Continuos Drain-Source Diode Forward Current				26	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				78	А
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{S} = 13 \text{ A} \text{ (Note 1)}$		0.9	1.3	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 V, I_F = 26 A,$ $dI_F/dt = 100 A/\mu s$		54	120	ns
l _m	Reverse Recovery Current			2.1	8	Α
THERMA	L CHARACTERISTICS	· ·	÷		•	
R _{θJC}	Thermal Resistance, Junction-to-Case				2.2	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

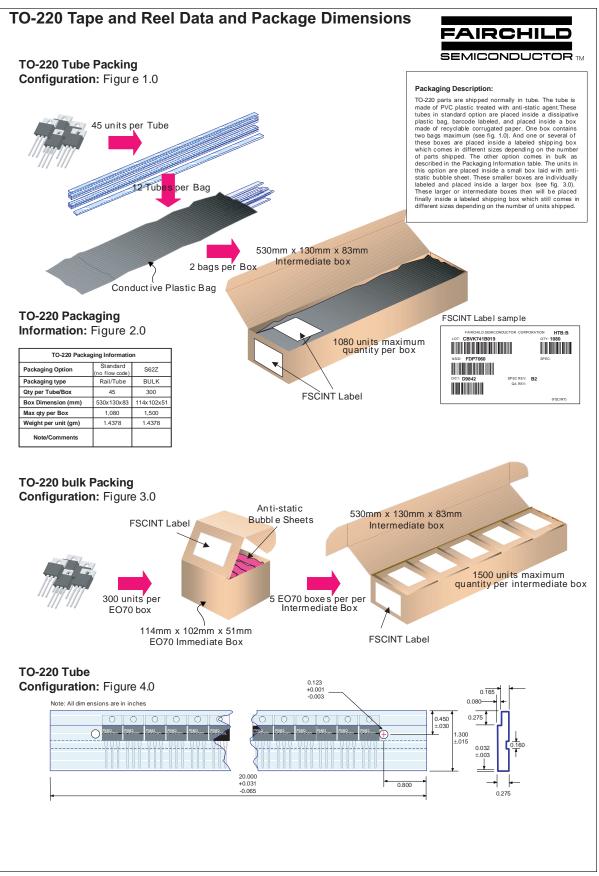
Note: 1. Pulse Test: Pulse Width \leq 300 µs, Duty Cycle \leq 2.0%.



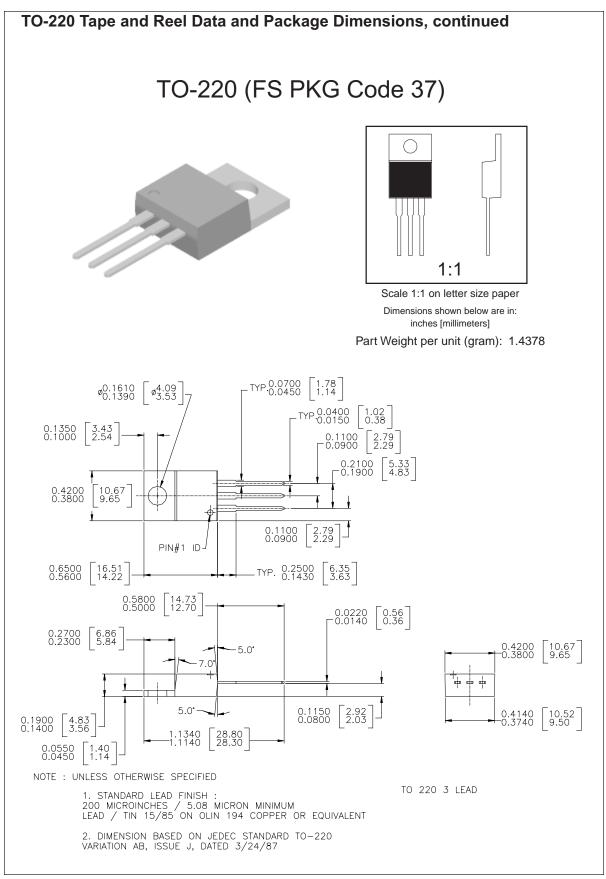


NDP5060L Rev.A

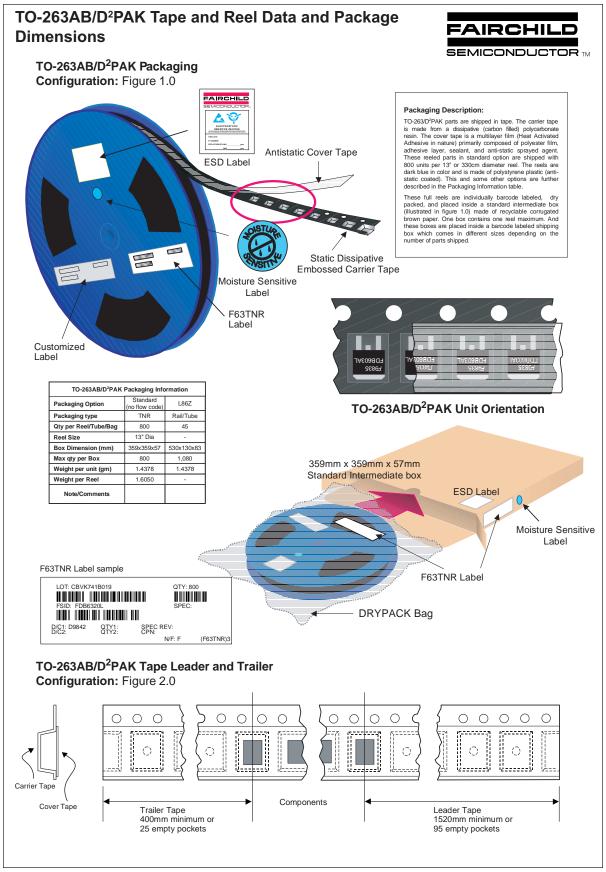




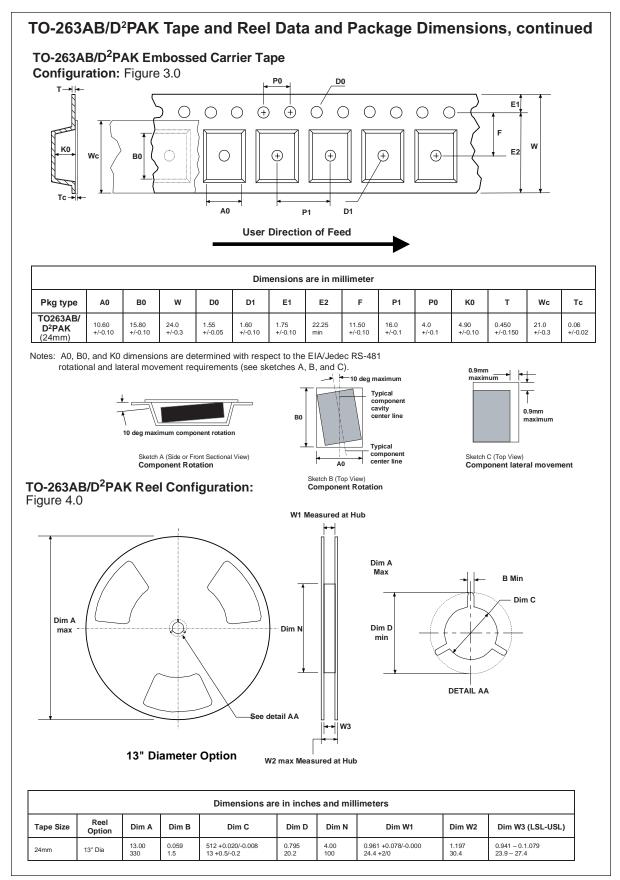
August 1999, Rev. B

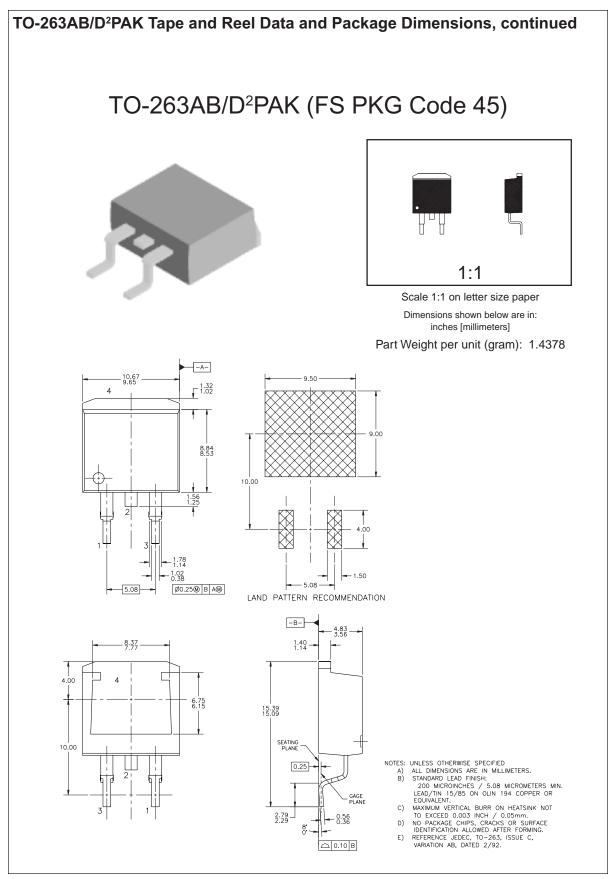


September 1998, Rev. A



September 1999, Rev. B





August 1998, Rev. A

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