September 1996

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SEMICONDUCTOR TM

NDT014

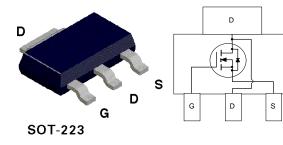
N-Channel Enhancement Mode Field Effect Transistor

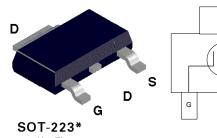
General Description

Power SOT N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.7A, 60V. $R_{DS(ON)} = 0.2\Omega @ V_{GS} = 10V.$
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.





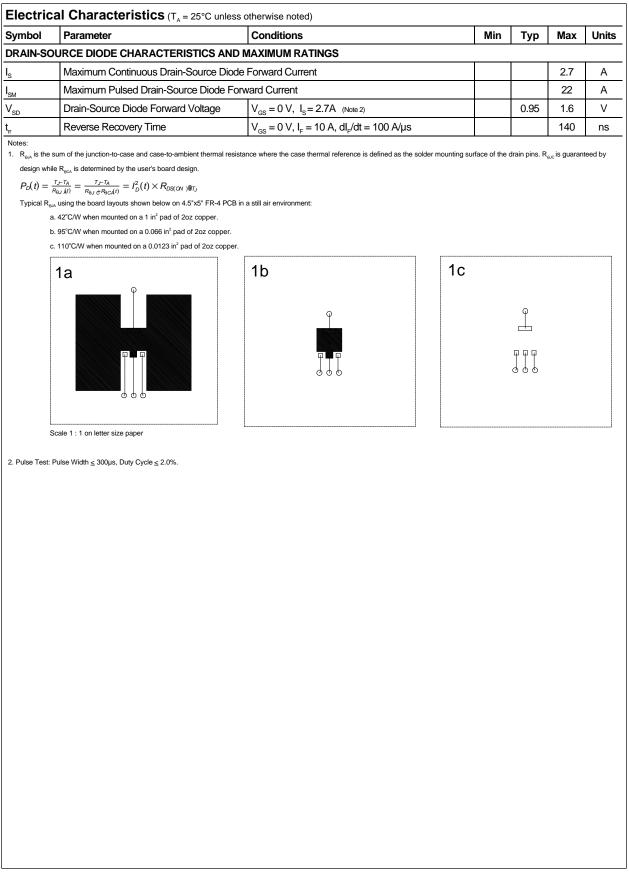
(J23Z)

Absolute Maximum Ratings $T_A = 25^{\circ}C$ unless otherwise noted

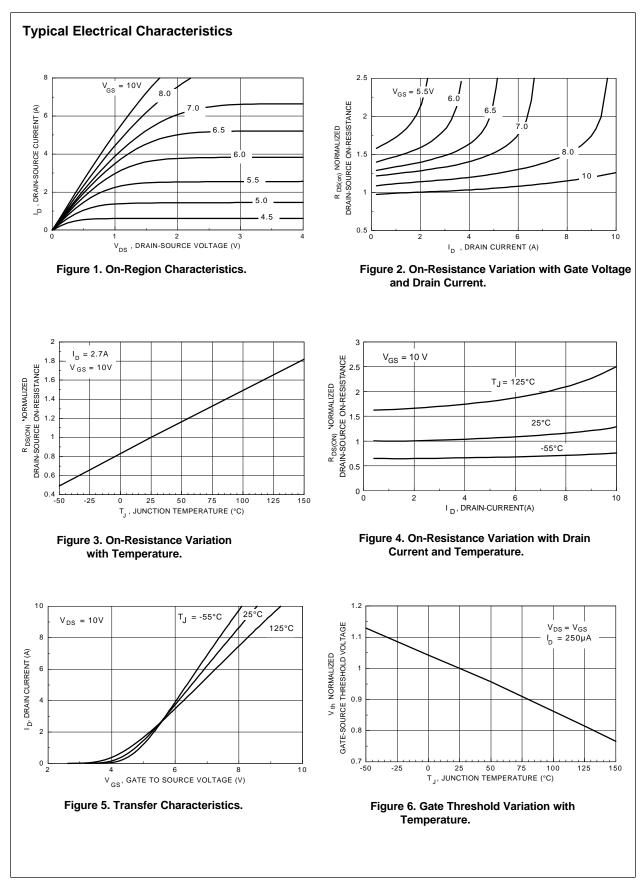
Symbol	Parameter		NDT014	Units
V _{DSS}	Drain-Source Voltage		60	
V _{GSS}	Gate-Source Voltage		±20	V
D	Drain Current - Continuous	(Note 1a)	±2.7	A
	- Pulsed		±10	
P _D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
Г _Ј ,Т _{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMA	L CHARACTERISTICS			
۶ _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
۲ _{өлс}	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W
	tion J23Z for cropped center drain lead.			

Order option J23Z for cropped center drain lead.

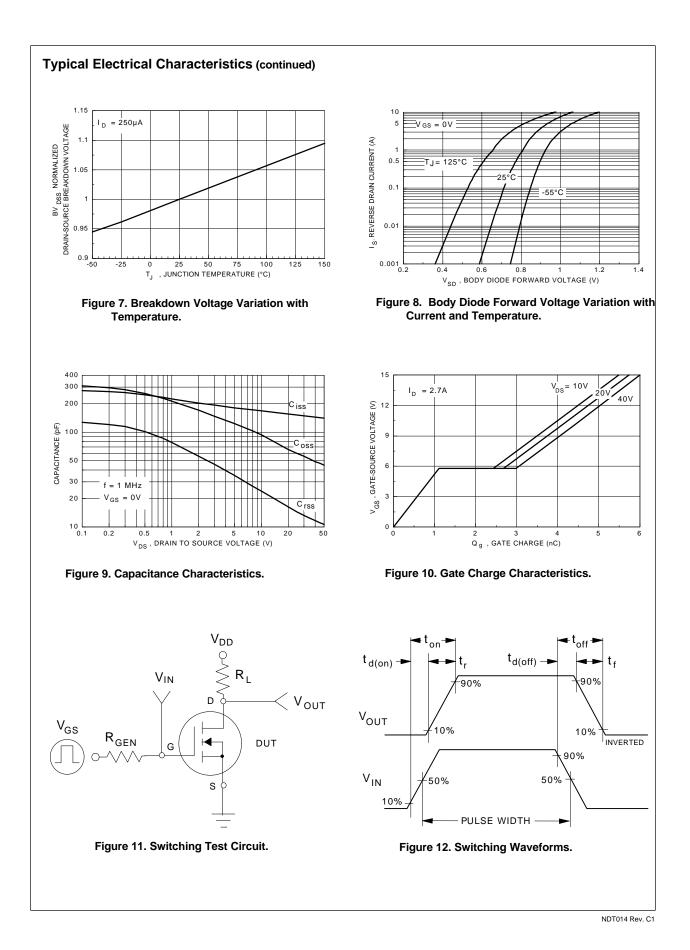
Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHA	RACTERISTICS					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 V, I_{D} = 250 \mu A$	60			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			25	μA
		$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, \text{T}_{J} = 125^{\circ}\text{C}$			250	μA
	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			100	nA
	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHAF	ACTERISTICS (Note 2)		-			
V _{GS(th)}	Gate Threshold Voltage	$V_{\rm DS} = V_{\rm GS}, \ I_{\rm D} = 250 \ \mu {\rm A}$	2	3	4	V
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 1.6 \text{ A}$		0.18	0.2	Ω
9 _{FS}	Forward Transconductance	$V_{\rm DS} = 25 \text{ V}, \text{ I}_{\rm D} = 1.6 \text{ A}$		2		S
DYNAMIC	CHARACTERISTICS					
C _{iss}	Input Capacitance	$V_{DS} = 25 V, V_{GS} = 0 V,$		155		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		60		pF
C _{rss}	Reverse Transfer Capacitance			15		pF
SWITCHI	NG CHARACTERISTICS (Note 2)					
t _{D(on)}	Turn - On Delay Time	$V_{DD} = 30 \text{ V}, \ \text{I}_{D} = 10 \text{ A},$		10	20	ns
t,	Turn - On Rise Time	V_{GEN} = 10 V, R_{GEN} = 24 Ω		64	100	ns
t _{D(off)}	Turn - Off Delay Time			10	20	ns
t,	Turn - Off Fall Time			10	20	ns
Q _g	Total Gate Charge	$V_{\rm DS} = 48 \ V,$		5	11	nC
Q_{gs}	Gate-Source Charge	$I_{\rm D} = 10 \text{ A}, V_{\rm GS} = 10 \text{ V}$		1.2	3.1	nC
Q _{gd}	Gate-Drain Charge			2	5.8	nC

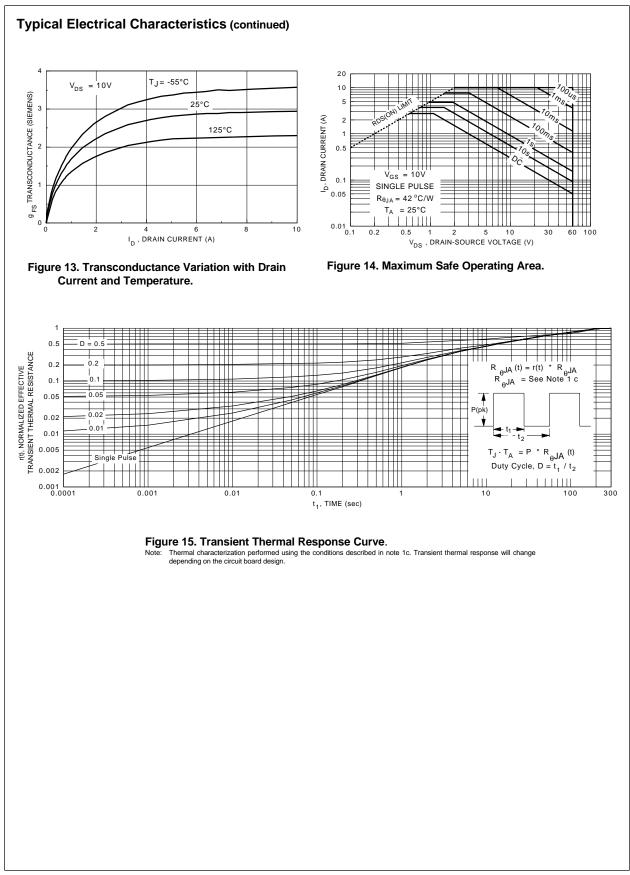


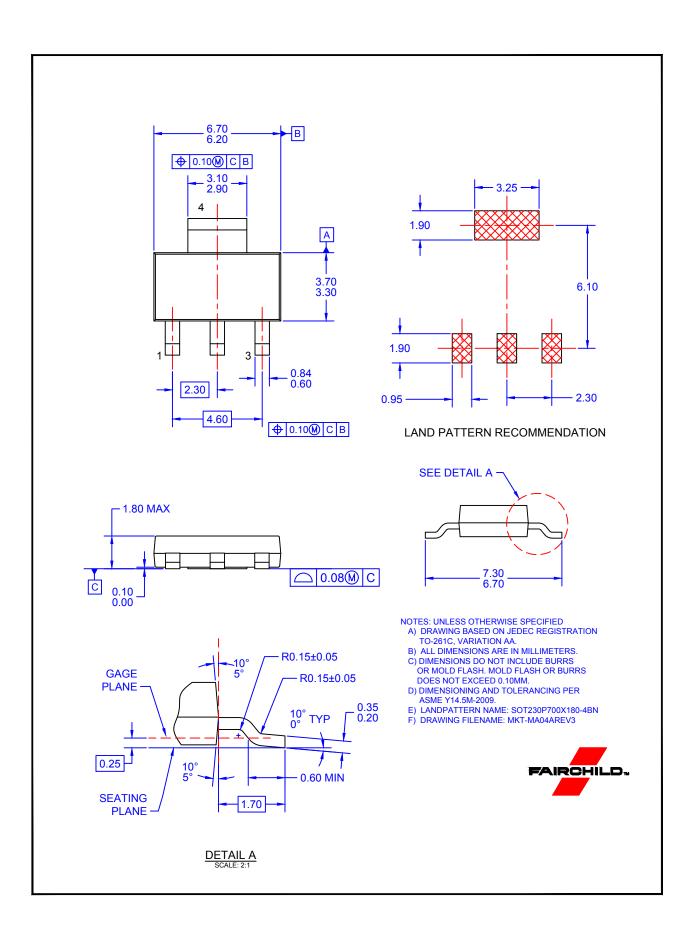
NDT014 Rev. C1



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