

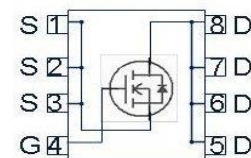
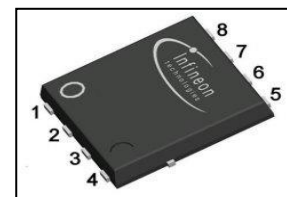
## OptiMOS™ Power-Transistor

### Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product Summary

$V_{DS}$	60	V
$R_{DS(on),max}$	6.6	m $\Omega$
$I_D$	64	A
$Q_{OSS}$	19	nC
$Q_G(0V..10V)$	17	nC


**PG-TDSON-8**


Type	Package	Marking
BSC066N06NS	PG-TDSON-8	066N06NS

**Maximum ratings**, at  $T_J=25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ }^\circ\text{C}$	64	A
		$V_{GS}=10\text{ V}, T_C=100\text{ }^\circ\text{C}$	41	
		$V_{GS}=10\text{ V}, T_C=25\text{ }^\circ\text{C}, R_{thJA}=50\text{K/W}^2)$	15	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ }^\circ\text{C}$	256	
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	$I_D=40\text{ A}, R_{GS}=25\text{ }\Omega$	21	mJ
Gate source voltage	$V_{GS}$		$\pm 20$	V

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See figure 3 for more detailed information

<sup>4)</sup> See figure 13 for more detailed information

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	46	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=50\text{ K/W}^2)$	2.5	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

#### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$	bottom	-	-	2.7	K/W
		top	-	-	20	
Device on PCB	$R_{\text{thJA}}$	6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	-	50	

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}$ , $I_{\text{D}}=1\text{ mA}$	60	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}$ , $I_{\text{D}}=20\text{ }\mu\text{A}$	2.1	2.8	3.3	
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=60\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{\text{DS}}=60\text{ V}$ , $V_{\text{GS}}=0\text{ V}$ , $T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}$ , $V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{ V}$ , $I_{\text{D}}=50\text{ A}$	-	5.5	6.6	m $\Omega$
		$V_{\text{GS}}=6\text{ V}$ , $I_{\text{D}}=12.5\text{ A}$	-	8.2	9.9	
Gate resistance	$R_{\text{G}}$		-	1.2	1.8	$\Omega$
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$ , $I_{\text{D}}=50\text{ A}$	32	65	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$	-	1200	1500	pF
Output capacitance	$C_{oss}$		-	300	375	
Reverse transfer capacitance	$C_{rss}$		-	19	38	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A}, R_{G,ext}=1.6\ \Omega$	-	7	-	ns
Rise time	$t_r$		-	3	-	
Turn-off delay time	$t_{d(off)}$		-	12	-	
Fall time	$t_f$		-	3	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	6.3	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.4	-	
Gate to drain charge	$Q_{gd}$		-	3.6	5.1	
Switching charge	$Q_{sw}$		-	6.5	-	
Gate charge total	$Q_g$		-	17	21	
Gate plateau voltage	$V_{plateau}$		-	5.1	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$	-	15	-	nC
Output charge	$Q_{oss}$	$V_{DD}=30\text{ V}, V_{GS}=0\text{ V}$	-	19	-	

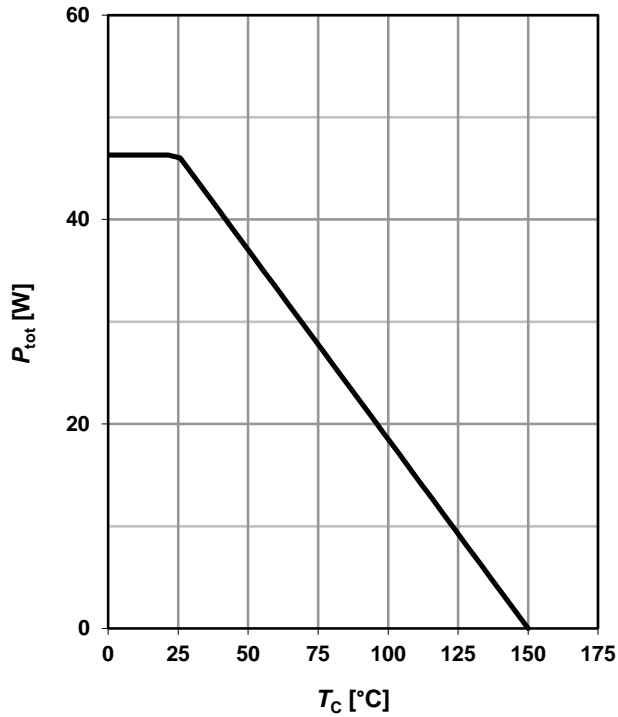
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	256	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=40\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.95	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=30\text{ V}, I_F=40\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$	-	23	37	ns
Reverse recovery charge	$Q_{rr}$		-	52	-	

<sup>5)</sup> See figure 16 for gate charge parameter definition

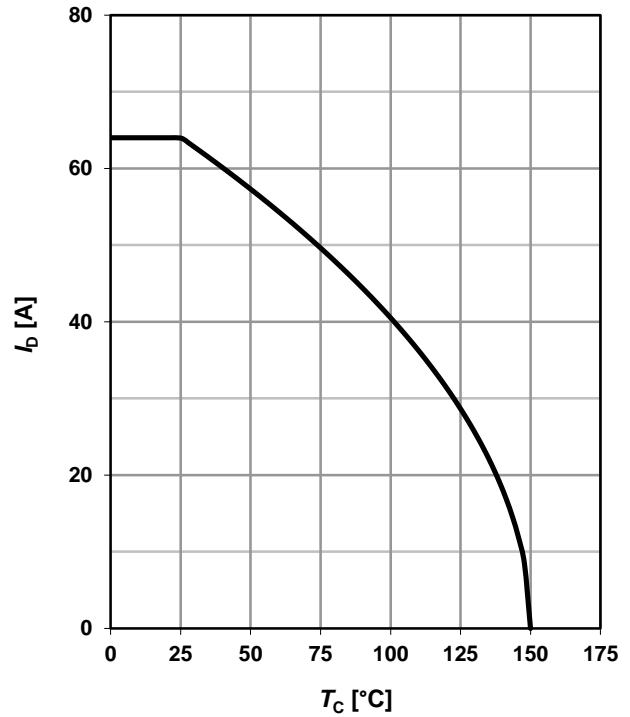
**1 Power dissipation**

$P_{tot}=f(T_C)$



**2 Drain current**

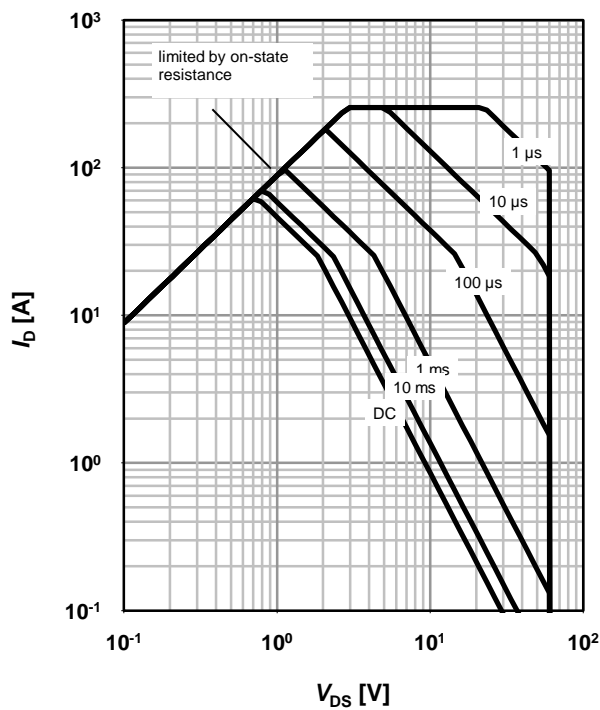
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



**3 Safe operating area**

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

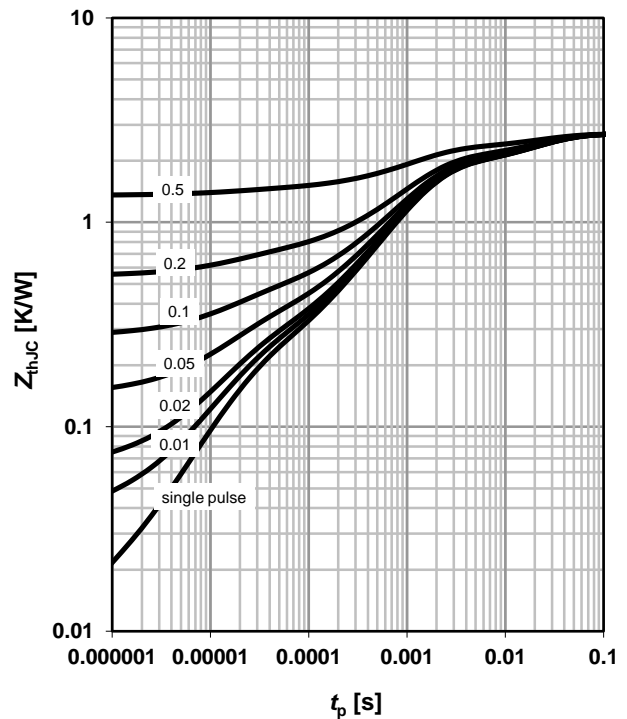
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJC}=f(t_p)$

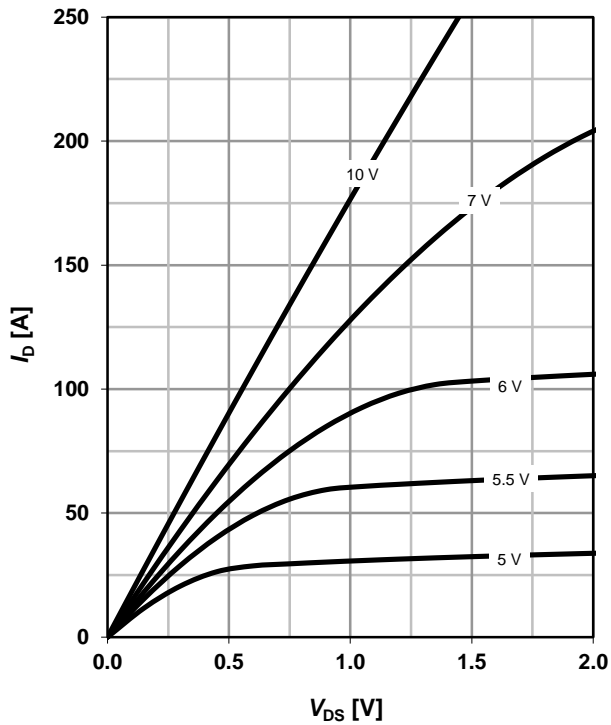
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

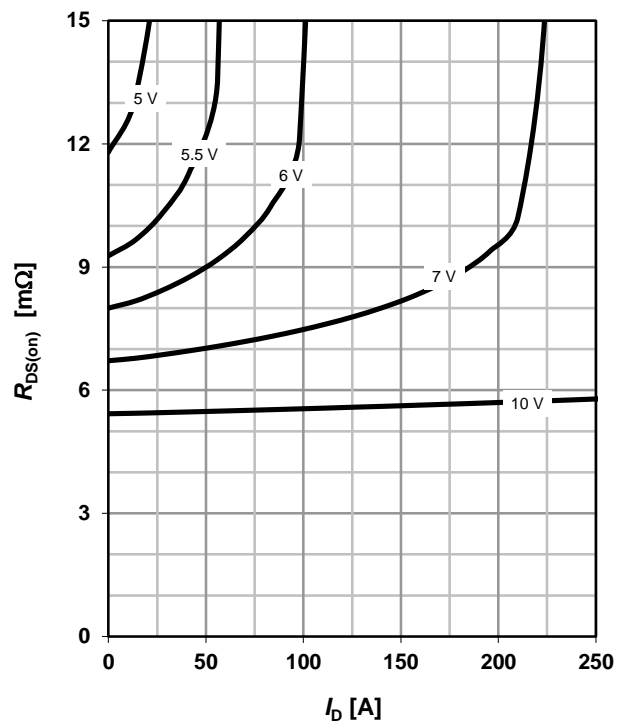
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

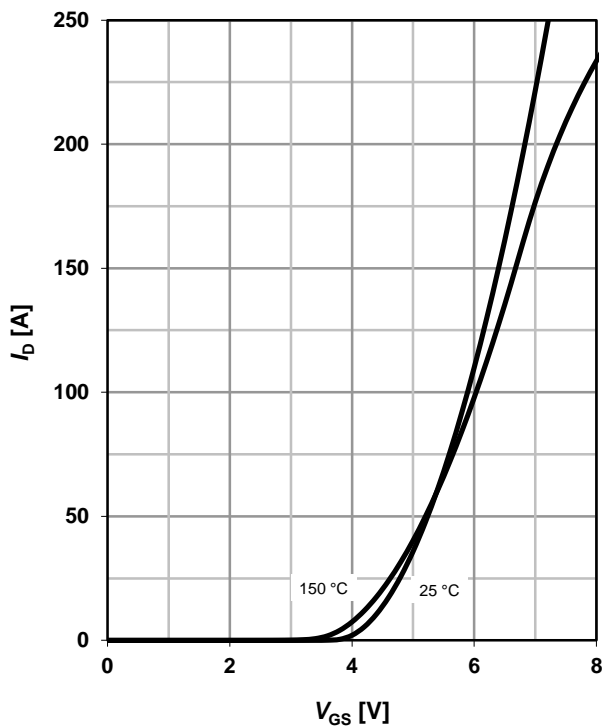
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

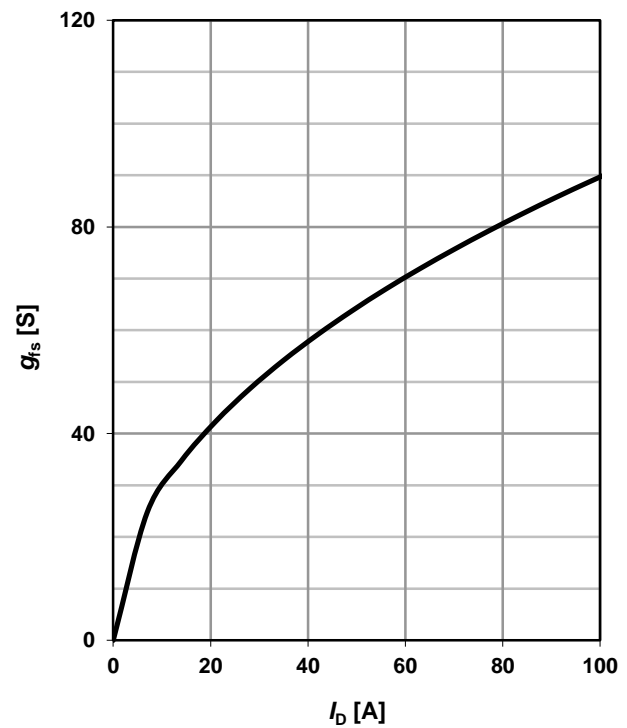
parameter:  $T_j$



**8 Typ. forward transconductance**

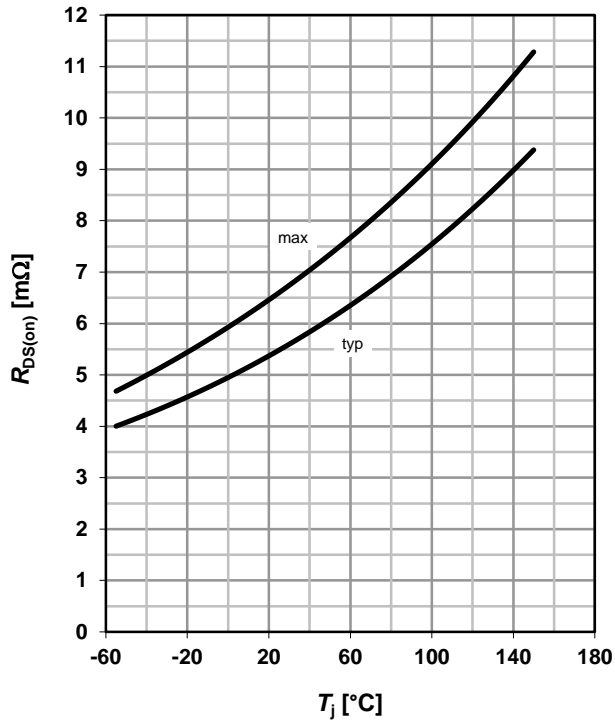
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

parameter:  $V_{GS}$



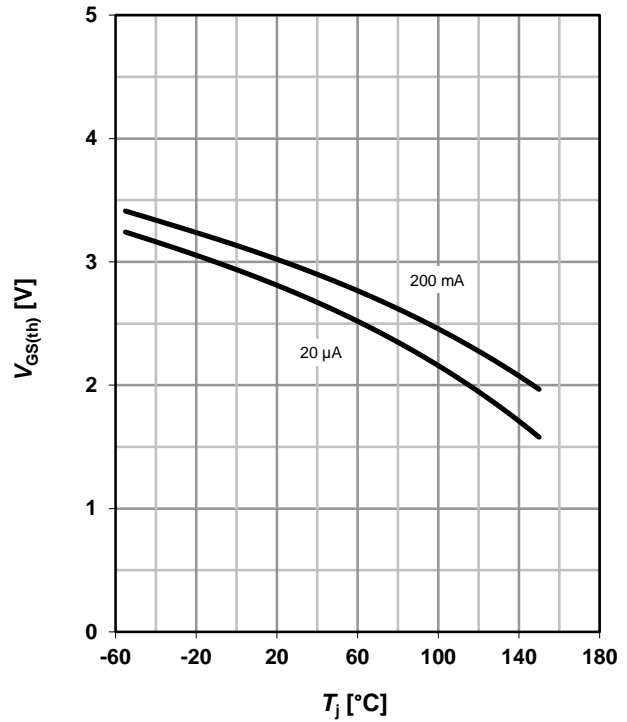
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=50\text{ A}; V_{GS}=10\text{ V}$



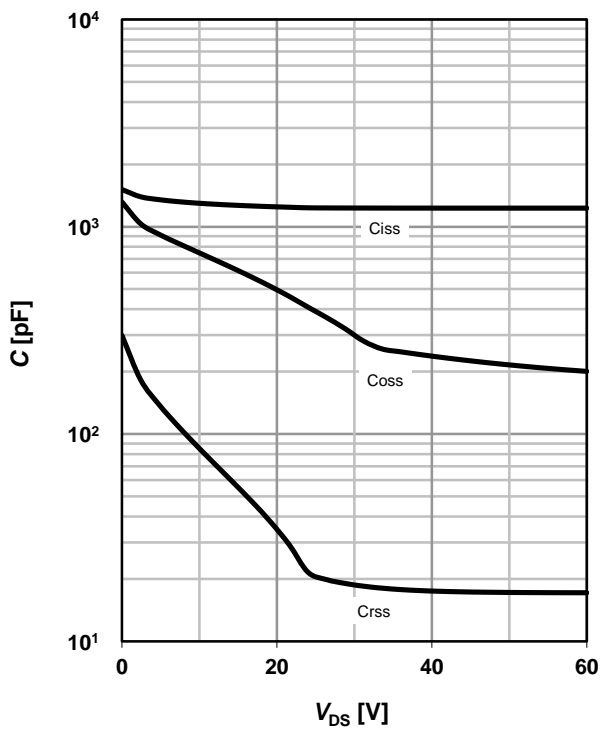
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$



**11 Typ. capacitances**

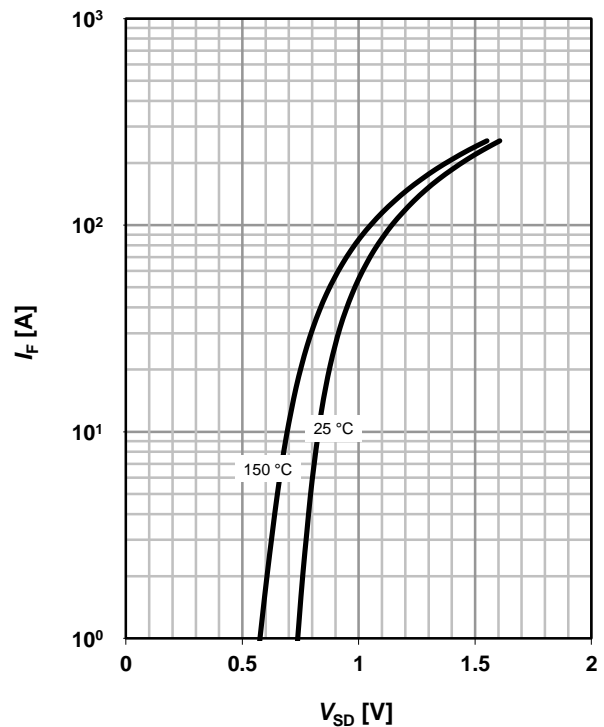
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

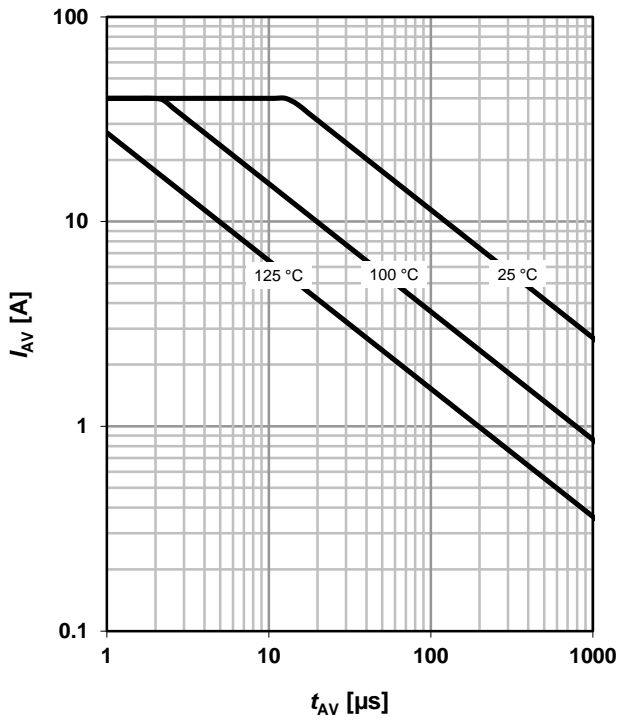
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

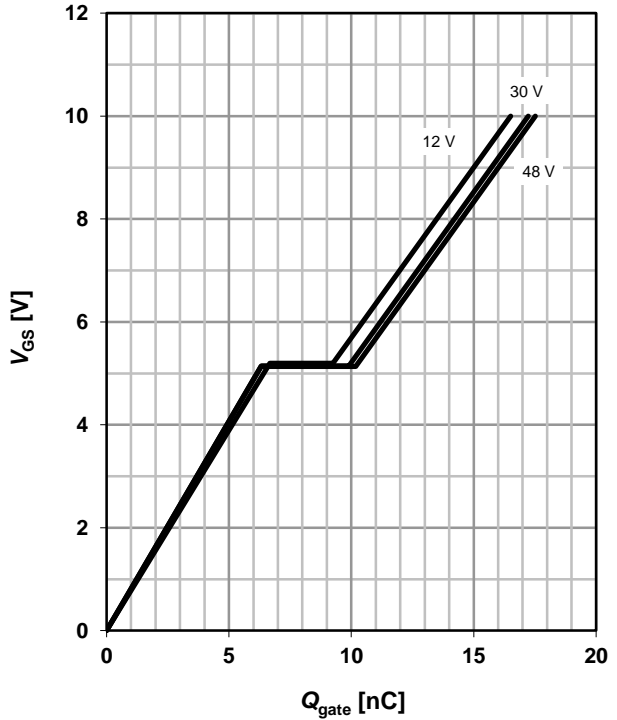
parameter:  $T_{j(\text{start})}$



**14 Typ. gate charge**

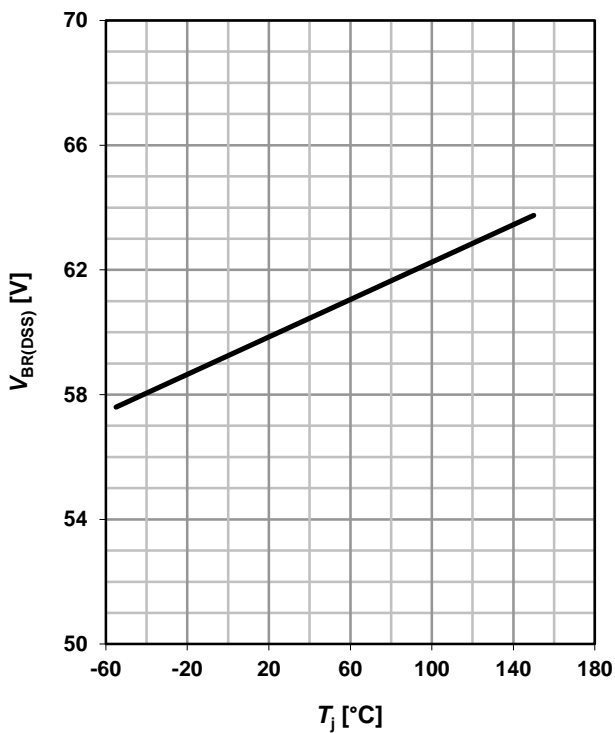
$V_{GS}=f(Q_{\text{gate}}); I_D=50 \text{ A pulsed}$

parameter:  $V_{DD}$

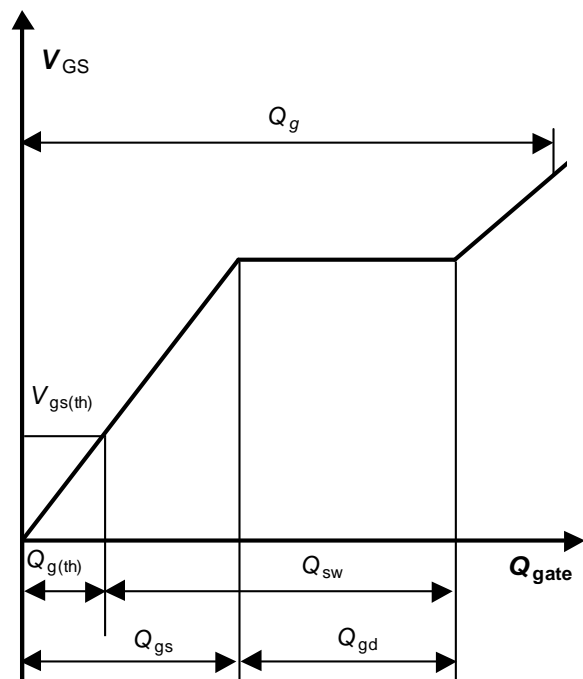


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



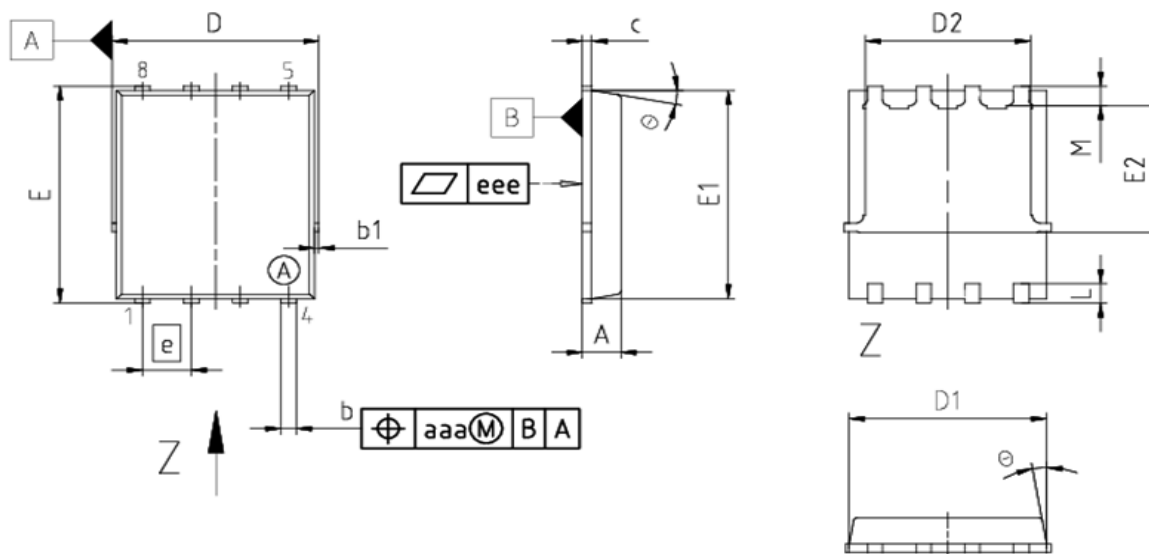
**16 Gate charge waveforms**



Package Outline

PG-TDSON-8

PG-TDSON-8: Outline



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
theta	8.5°	12°
aaa	0.25	
eee	0.08	

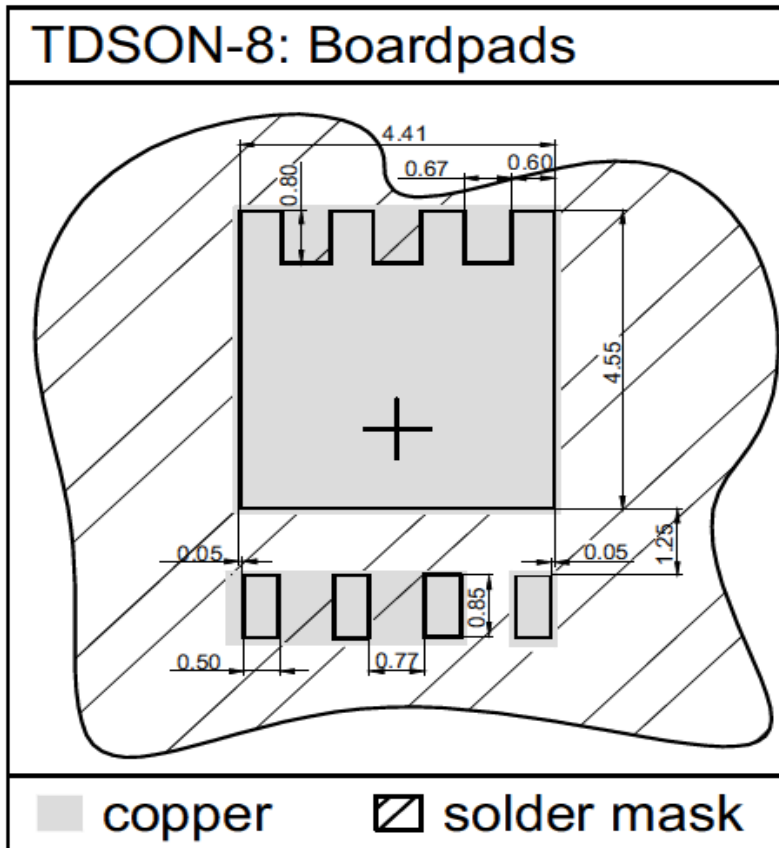
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<b>EUROPEAN PROJECTION</b> 
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<b>REVISION</b> 04



Package Footprint

PG-TDSON-8

PG-TDSON-8: Footprint



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