

# TVS Diode

Transient Voltage Suppressor Diode

## ESD5V3U4U-HDMI

Uni-directional Ultra-low Capacitance ESD / Transient Protection Array

ESD5V3U4U-HDMI

## Data Sheet

Revision 1.1, 2012-07-03  
Final

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**Revision History Revision 1.0, 2012-06-30**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.1, 2012-07-03</b>	
7	Figure 2-1

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Last Trademarks Update 2010-10-26

# 1 Uni-directional Ultra-low Capacitance ESD / Transient Protection Array

## 1.1 Features

- ESD / Transient protection of high speed data lines exceeding:
  - IEC61000-4-2 (ESD):  $\pm 20$  kV (air / contact)
  - IEC61000-4-4 (EFT): 2.5 kV / 50 A (5/50 ns)
  - IEC61000-4-5 (surge): 3 A (8/20  $\mu$ s)
- Maximum working voltage:  $V_R = 5.3$  V
- Very low reverse current:  $I_R < 1$  nA typ.
- Extremely low capacitance: 0.4 pF typ. (I/O to GND)
- Four-lines protection array with pad pitch = 0.5 mm
- Flow-through design for optimal PCB layout of differential lines
- Pb-free package (RoHS compliant) and halogen free package



## 1.2 Application Examples

- Protection of high speed digital interfaces like:
- HDMI 1.3, HDMI 1.4a, MHL, DisplayPort, S-ATA, DVI, MIPI, MDDI
- USB2.0, 10/100/1000 Ethernet, FireWire

# 2 Product Description

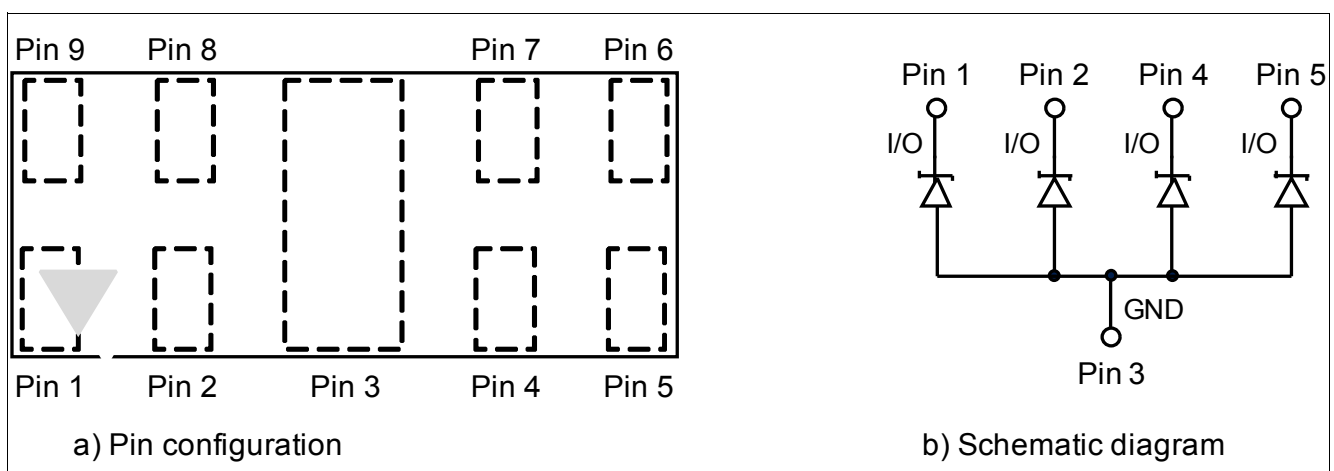


Figure 2-1 Pin Configuration and Schematic Diagram

Table 2-1 Ordering information

Type	Package	Configuration	Marking code
ESD5V3U4U-HDMI	PG-TSLP-9-1	4 lines, uni-directional	Z1

### 3 Characteristics

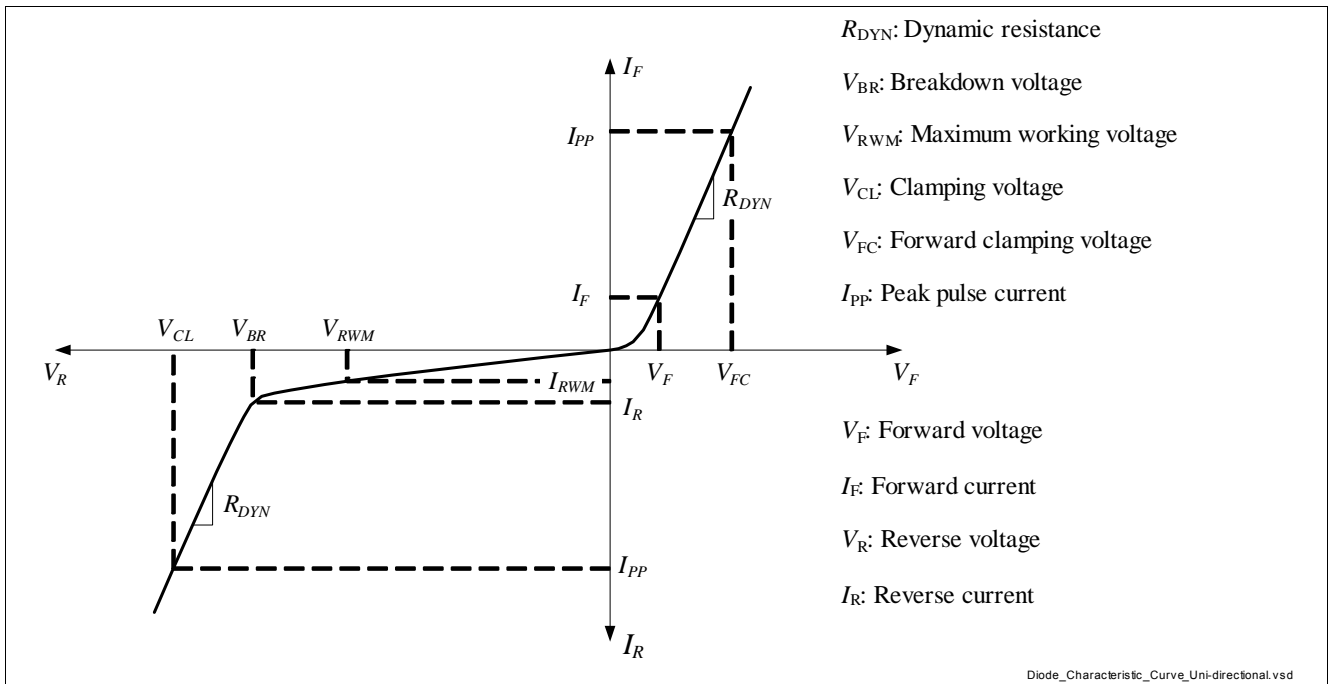
**Table 3-1 Maximum Rating at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge <sup>1)</sup>	$V_{ESD}$	–	–	20	kV
Peak pulse current ( $t_p = 8/20\text{ }\mu\text{s}$ ) <sup>2)</sup>	$I_{PP}$	–	–	3	A
Operating temperature range	$T_{OP}$	-40	–	125	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-65	–	150	$^\circ\text{C}$

1)  $V_{ESD}$  according to IEC61000-4-2

2)  $I_{PP}$  according to IEC61000-4-5

#### 3.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified



**Figure 3-1 Definitions of Electrical Characteristics**

**Table 3-2 DC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	–	–	5.3	V	
Breakdown voltage	$V_{BR}$	6	–	–	V	$I_{BR} = 1\text{ mA}$ (I/O to GND)
Reverse current	$I_R$	–	<1	50	nA	$V_R = 5.3\text{ V}$ (I/O to GND)

**Table 3-3 RF Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance <sup>1)</sup>	$C_L$	–	0.4	0.6	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ (I/O to GND)
Line capacitance <sup>1)</sup>	$C_L$	–	0.2	0.3	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ (I/O to I/O)

1) Total capacitance line to ground

**Table 3-4 ESD Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>1)</sup>	$V_{CL}$	–	19	–	V	$I_{PP} = 16\text{ A}$ (I/O to GND)
		–	28	–	V	$I_{PP} = 30\text{ A}$ (I/O to GND)
Forward clamping voltage <sup>1)</sup>	$V_{FC}$	–	10	–	V	$I_{PP} = 16\text{ A}$ (GND to I/O)
		–	17	–	V	$I_{PP} = 30\text{ A}$ (GND to I/O)
Dynamic resistance <sup>1)</sup>	$R_{DYN}$	–	0.6	–	$\Omega$	I/O to GND
		–	0.5	–		GND to I/O

1) Please refer to Application Note AN210 [1]. TLP parameter:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ , averaging window:  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ , extraction of dynamic resistance using least squares fit of TLP characteristic between  $I_{PP1} = 10\text{ A}$  and  $I_{PP2} = 40\text{ A}$ .

3.2 Typical Characteristics at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

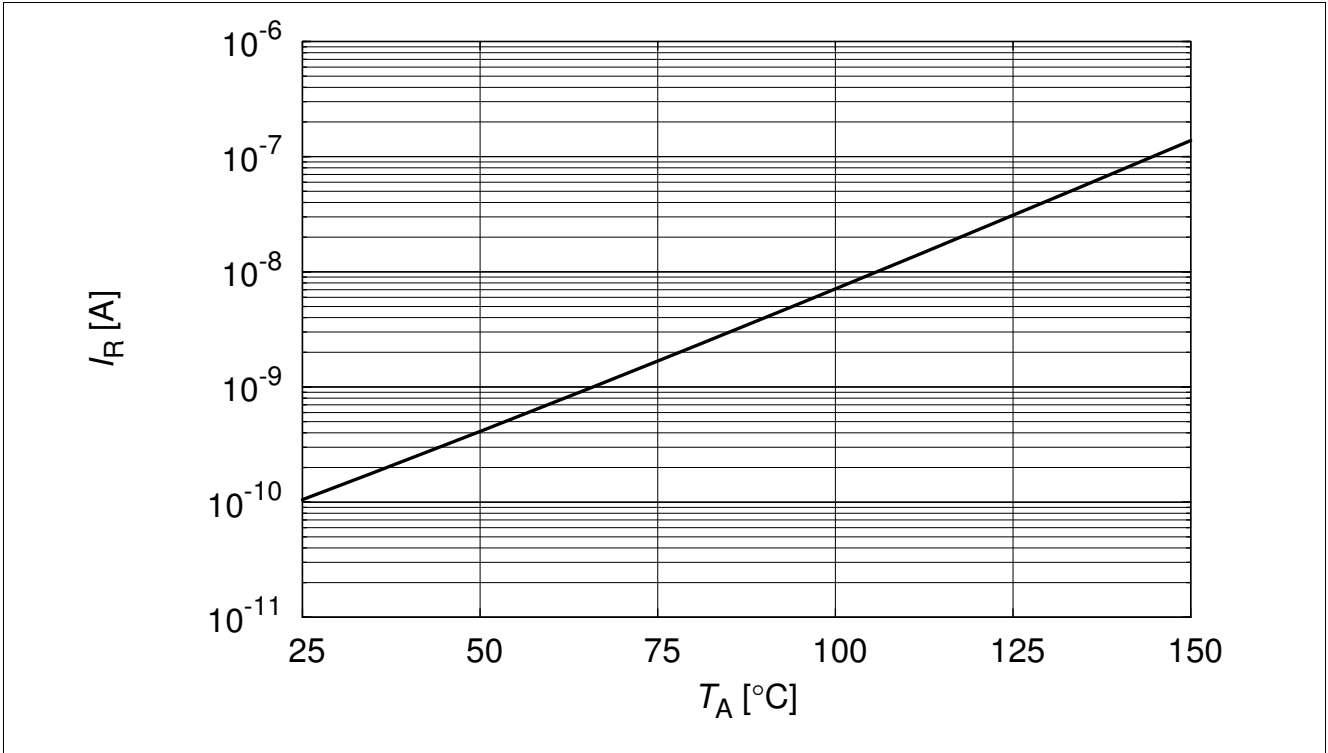


Figure 3-2 Reverse current:  $I_R = f(T_A)$ ,  $V_R = 5.3 \text{ V}$ , (I/O to GND)

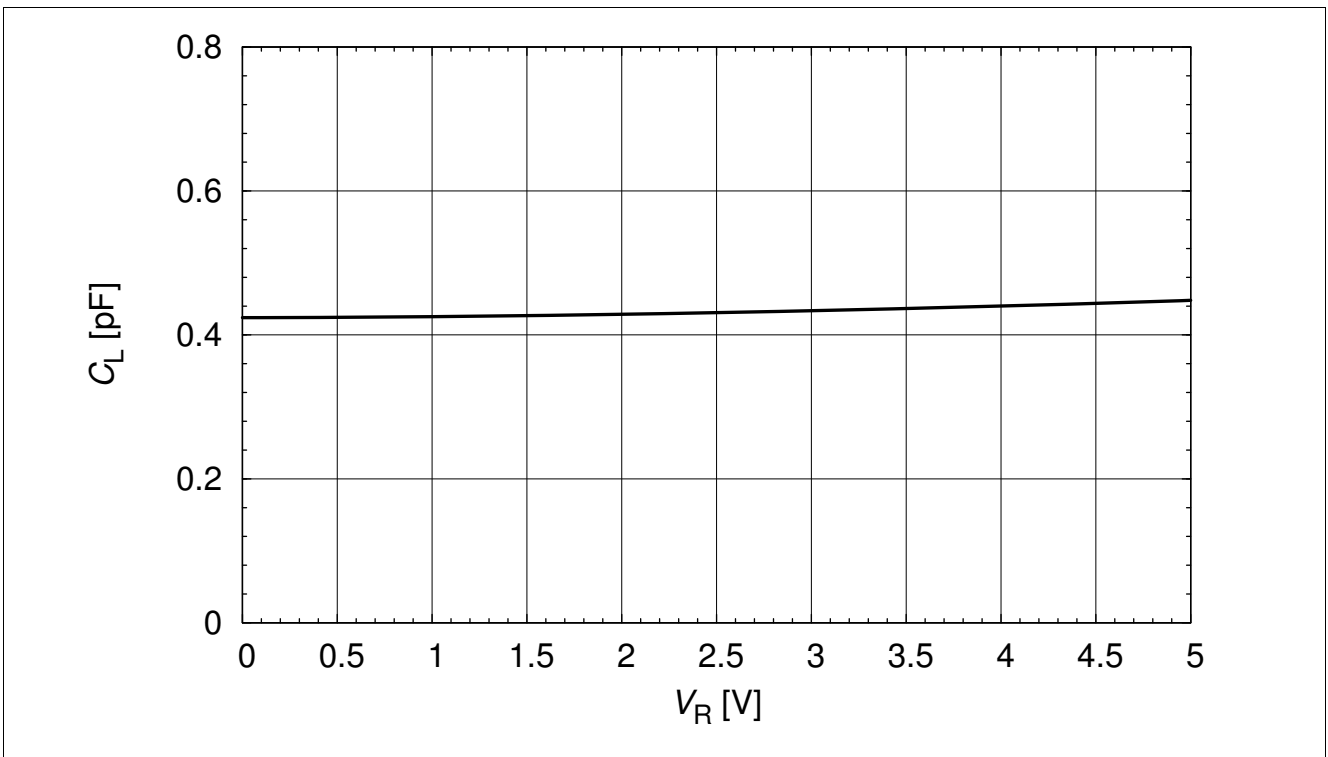


Figure 3-3 Diode capacitance:  $C_L = f(V_R)$ , (I/O to GND)

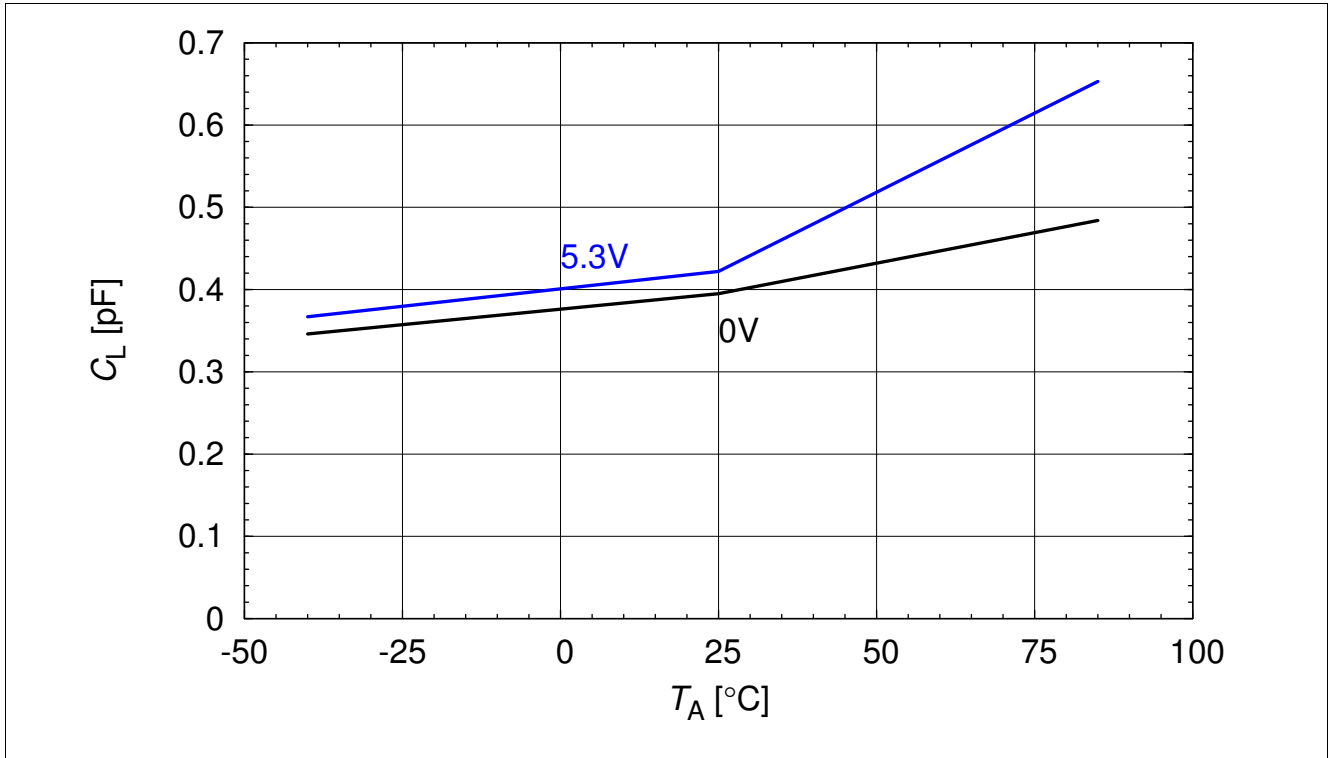


Figure 3-4 Line capacitance:  $C_L = f(T_A)$

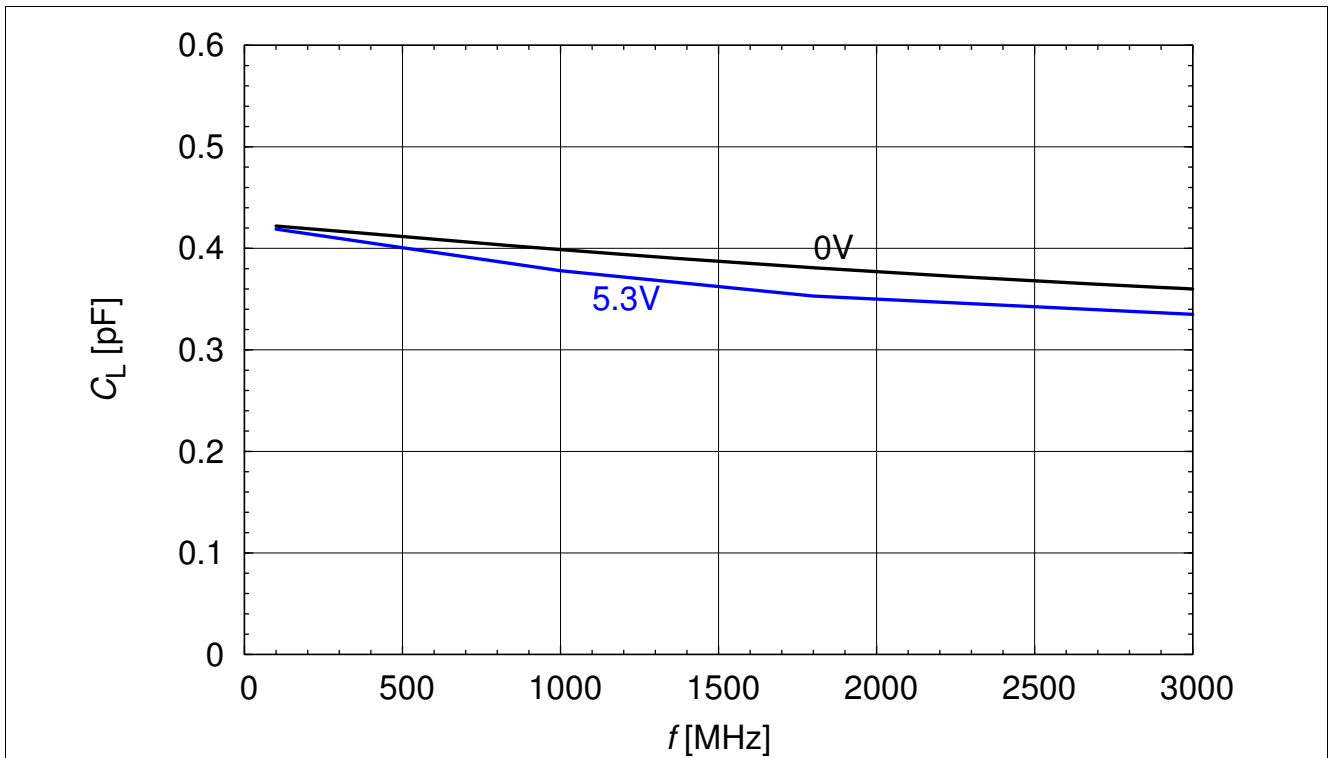


Figure 3-5 Line capacitance:  $C_L = f(f)$ , (I/O to GND)



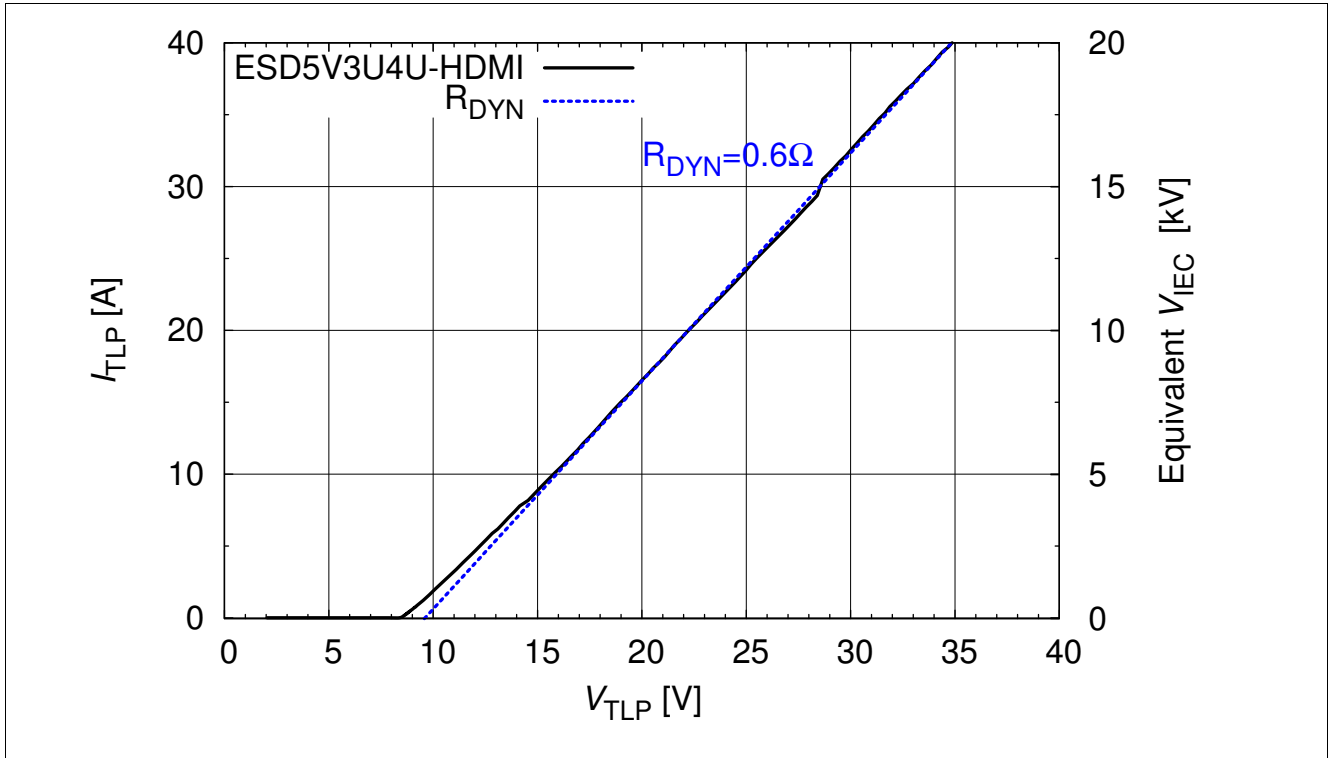


Figure 3-6 Forward clamping voltage:  $I_{TLP} = f(V_{TLP})$ , (GND to I/O) [1]

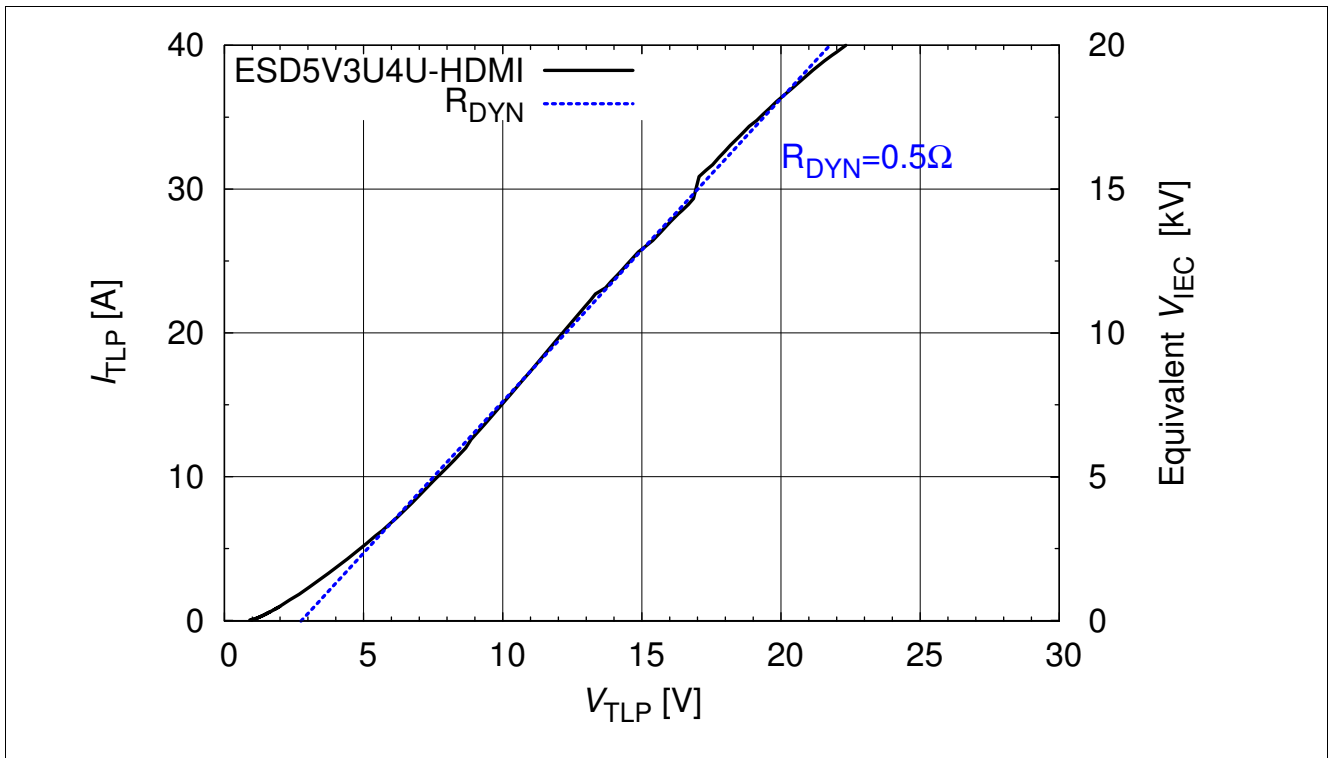


Figure 3-7 Reverse clamping voltage:  $I_{TLP} = f(V_{TLP})$ , (I/O to GND) [1]

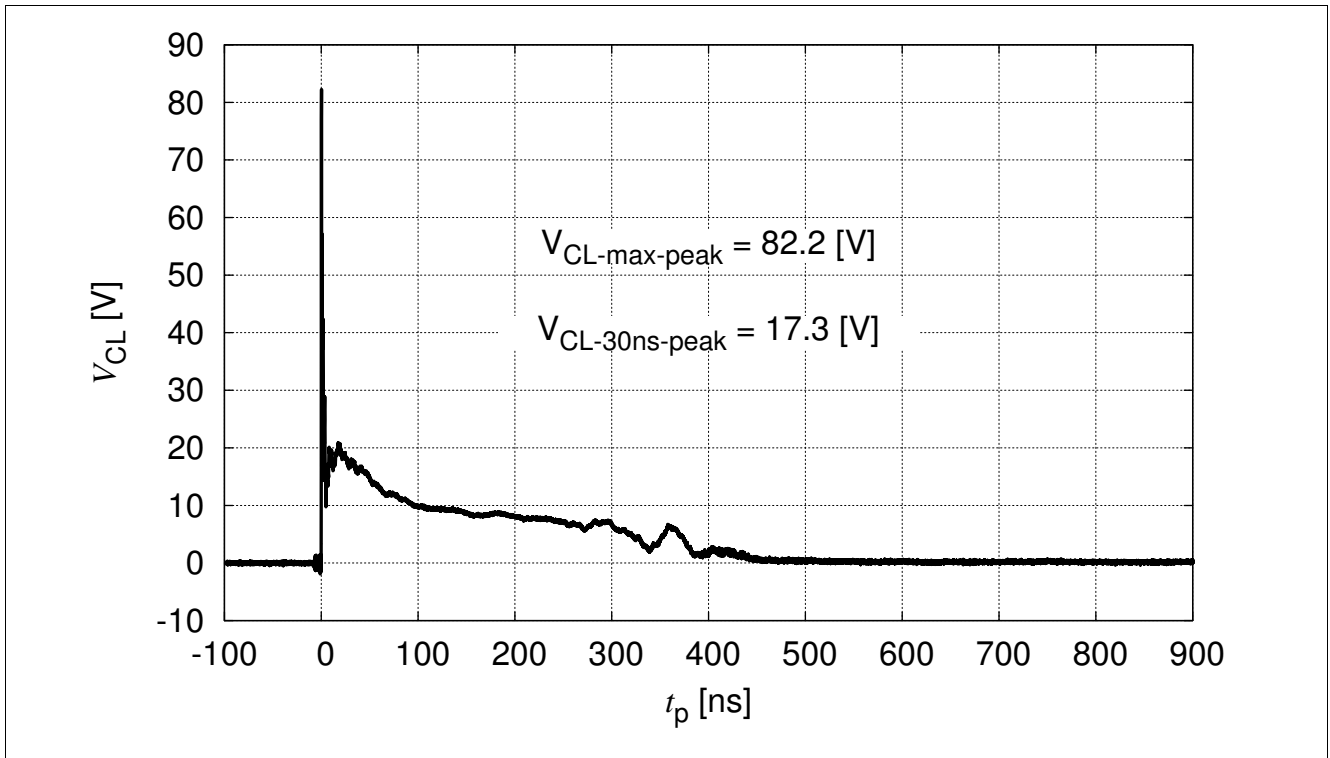


Figure 3-8 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV positive pulse, (I/O to GND)

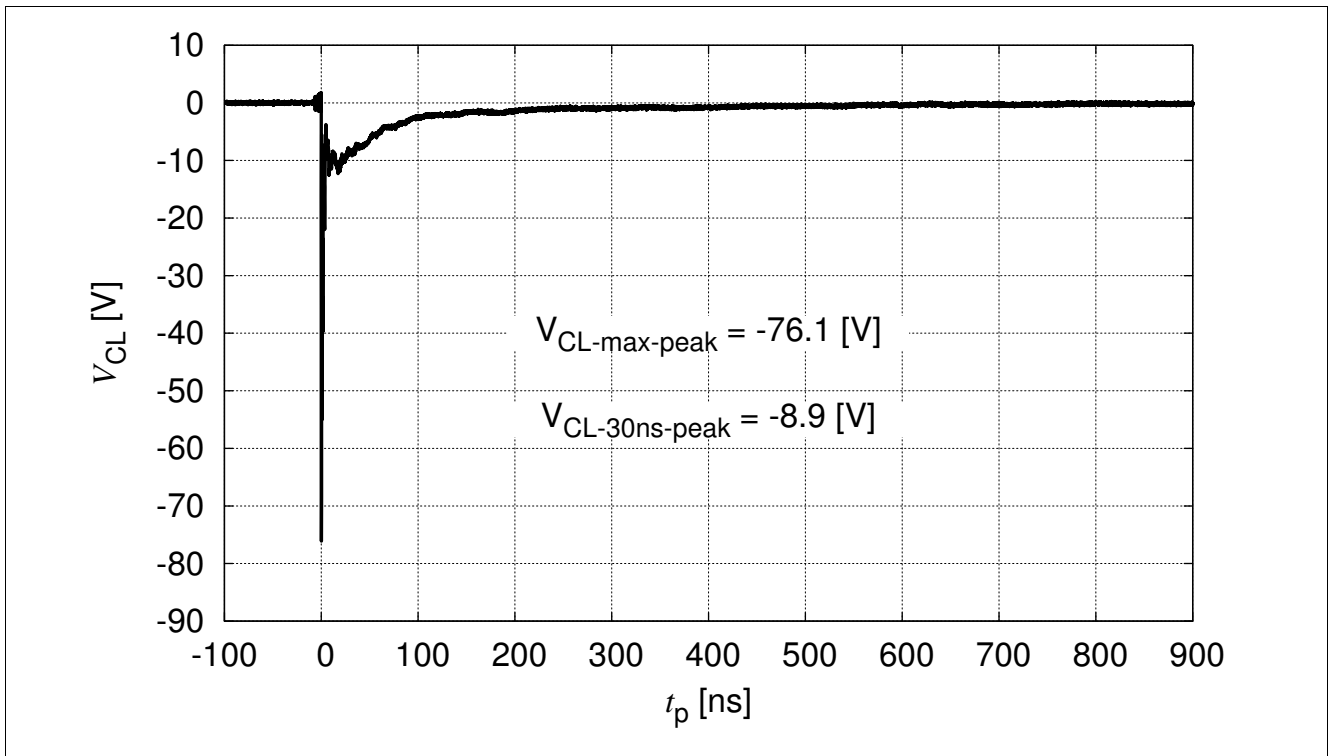


Figure 3-9 IEC61000-4-2  $V_{CL} = f(t)$ , 8 kV negative pulse, (I/O to GND)

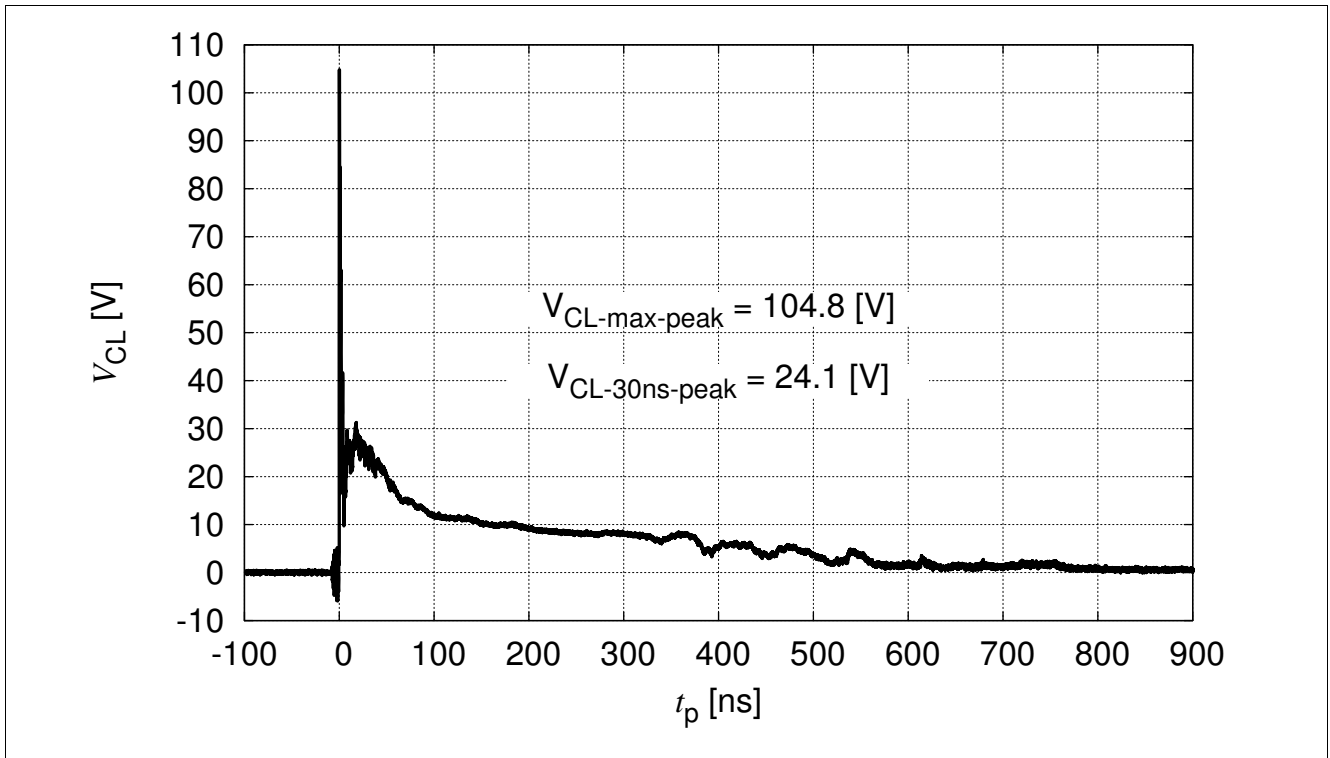


Figure 3-10 IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV positive pulse, (I/O to GND)

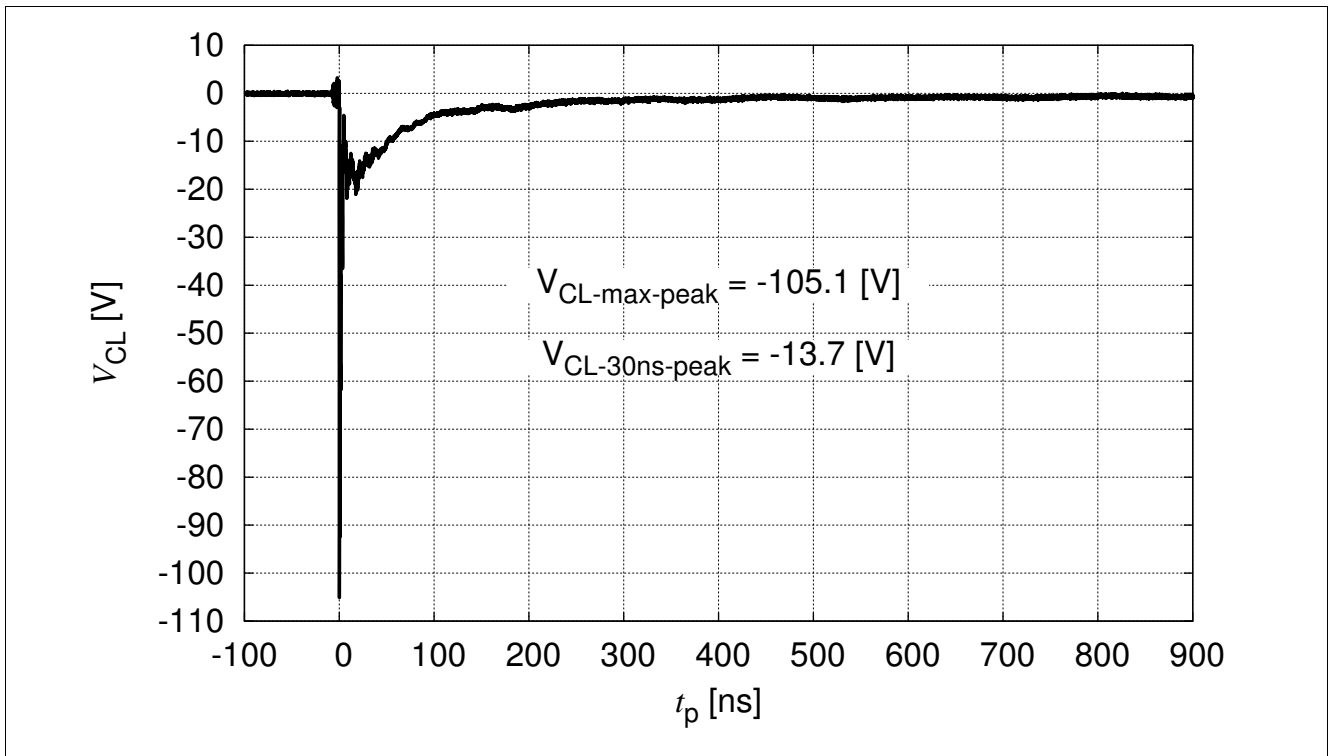
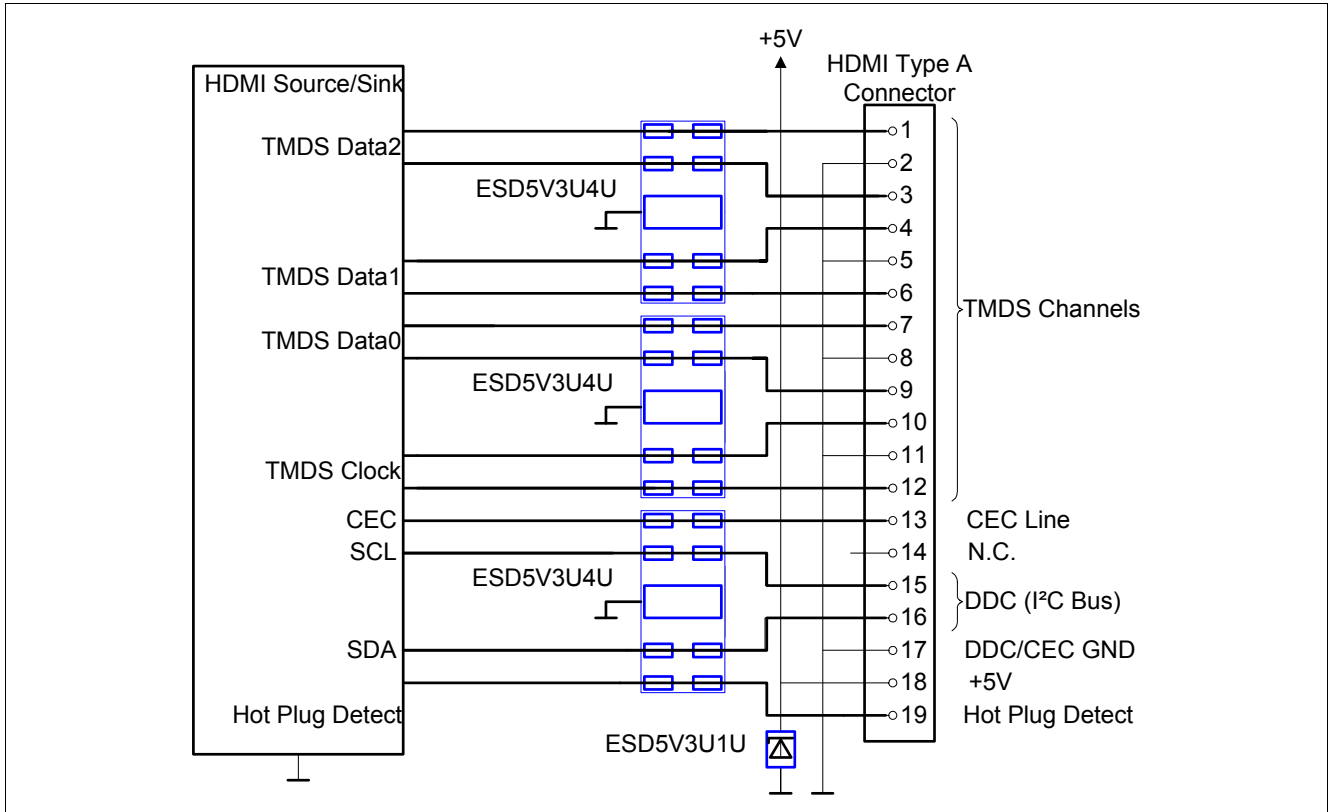


Figure 3-11 IEC61000-4-2  $V_{CL} = f(t)$ , 15 kV negative pulse, (I/O to GND)

## 4 Application Information



**Figure 4-1 4 lines, uni-directional ESD5V3U4U-HDMI**

For protection on the 5 V supply rail please refer to ESD5V3U1U- TVS diode data sheet.

## 5 Ordering Information Scheme (Examples)

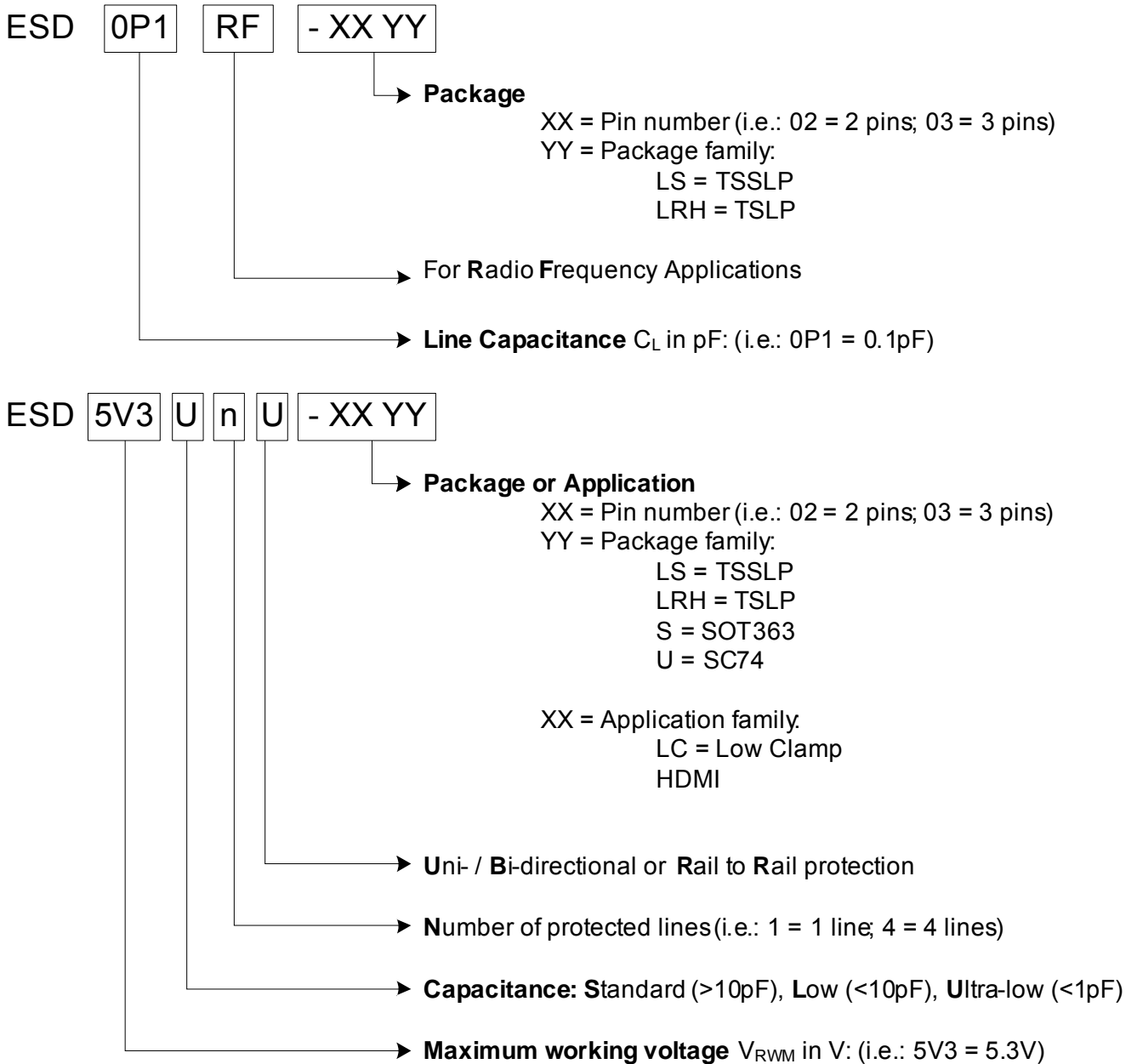


Figure 5-1 Ordering information scheme



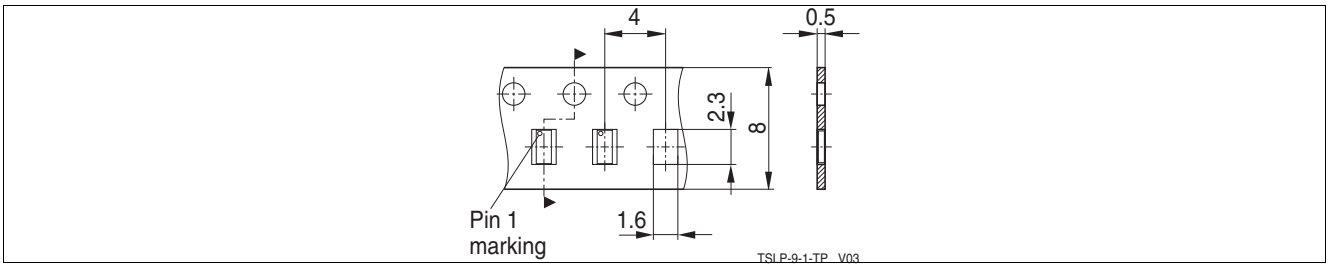


Figure 6-3 PG-TSLP-9-1: Packing

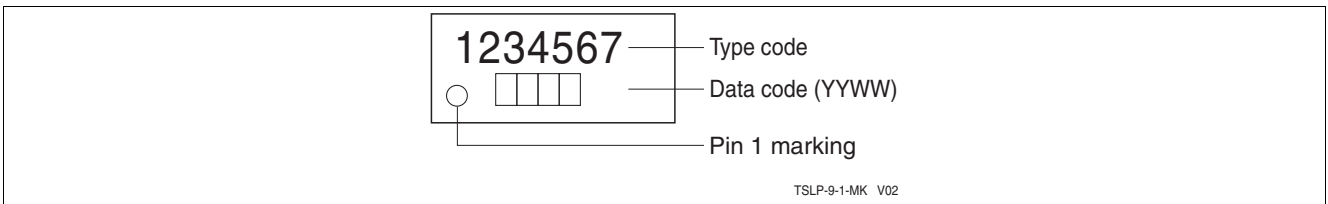


Figure 6-4 PG-TSLP-9-1: Marking (example)

**References**

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology



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