

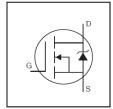
## **AUTOMOTIVE GRADE**



HEXFET® Power MOSFET

## **Features**

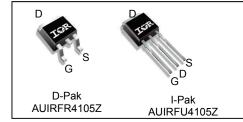
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- · Repetitive Avalanche Allowed up to Timax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



V <sub>DSS</sub>		55V
R <sub>DS(on)</sub> max.		24.5mΩ
I <sub>D</sub>		30A

## Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Boss nort number	Standard Pack		Orderable Part Number	
Base part number	Package Type	Form	Quantity	Orderable Part Number
AUIRFU4105Z	I-Pak	Tube	75	AUIRFU4105Z
ALUDED44057 D. Dok		Tube	75	AUIRFR4105Z
AUIRFR4105Z	D-Pak	Tape and Reel Left	3000	AUIRFR4105ZTRL

## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless

•	•	. ,	
Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	30	
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	21	Α
I <sub>DM</sub>	Pulsed Drain Current ①	120	=
P <sub>D</sub> @T <sub>C</sub> = 25°C	Maximum Power Dissipation	48	W
	Linear Derating Factor	0.32	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	29	
E <sub>AS</sub> (Tested)	Single Pulse Avalanche Energy Tested Value ®	46	- mJ
I <sub>AR</sub>	Avalanche Current ①	See Fig.15,16, 12a, 12b	Α
E <sub>AR</sub>	Repetitive Avalanche Energy ©		mJ
$T_J$	Operating Junction and	-55 to + 175	
T <sub>STG</sub>	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

## Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ®		3.12	
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mount) ∅		50	°C/W
$R_{\theta JA}$	Junction-to-Ambient		110	

HEXFET® is a registered trademark of Infineon.

<sup>\*</sup>Qualification standards can be found at www.infineon.com



# Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.053		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance		19	24.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 18A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$
gfs	Forward Trans conductance	16			S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 18A ③
	Drain to Source Leakage Current			20	μA	$V_{DS} = 55V$ , $V_{GS} = 0V$
IDSS	Drain-to-Source Leakage Current			250	μΑ	$V_{DS} = 55V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
	Gate-to-Source Forward Leakage			200	- Λ	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Reverse Leakage			-200	nA	$V_{GS} = -20V$

# Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

<del>-</del>		_	-		
Total Gate Charge		18	27		I <sub>D</sub> = 18A
Gate-to-Source Charge		5.3		nC	$V_{DS} = 44V$
Gate-to-Drain Charge		7.0			V <sub>GS</sub> = 10V3
Turn-On Delay Time	—	10			$V_{DD} = 28V$
Rise Time		40		no	I <sub>D</sub> = 18A
Turn-Off Delay Time		26		115	$R_G = 24.5\Omega$
Fall Time		24			V <sub>GS</sub> = 10V3
Internal Drain Inductance		4.5			Between lead, 6mm (0.25in.)
Internal Source Inductance		7.5			from package and center of die contact
Input Capacitance		740			$V_{GS} = 0V$
Output Capacitance		140			$V_{DS} = 25V$
Reverse Transfer Capacitance		74		nΕ	f = 1.0MHz
Output Capacitance		450		рΓ	$V_{GS} = 0V$ , $V_{DS} = 1.0V$ $f = 1.0MHz$
Output Capacitance		110			$V_{GS} = 0V$ , $V_{DS} = 44V$ $f = 1.0MHz$
Effective Output Capacitance		180			$V_{GS}$ = 0V, $V_{DS}$ = 0V to 44V $\oplus$
	Gate-to-Source Charge Gate-to-Drain Charge Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time Internal Drain Inductance Internal Source Inductance Input Capacitance Output Capacitance Reverse Transfer Capacitance Output Capacitance Output Capacitance Output Capacitance Output Capacitance	Gate-to-Source Charge ————————————————————————————————————	Gate-to-Source Charge         — 5.3           Gate-to-Drain Charge         — 7.0           Turn-On Delay Time         — 10           Rise Time         — 40           Turn-Off Delay Time         — 26           Fall Time         — 24           Internal Drain Inductance         — 7.5           Input Capacitance         — 740           Output Capacitance         — 140           Reverse Transfer Capacitance         — 74           Output Capacitance         — 450           Output Capacitance         — 450           Output Capacitance         — 110	Gate-to-Source Charge         — 5.3         —           Gate-to-Drain Charge         — 7.0         —           Turn-On Delay Time         — 10         —           Rise Time         — 40         —           Turn-Off Delay Time         — 26         —           Fall Time         — 24         —           Internal Drain Inductance         — 4.5         —           Internal Source Inductance         — 7.5         —           Input Capacitance         — 740         —           Output Capacitance         — 140         —           Reverse Transfer Capacitance         — 74         —           Output Capacitance         — 450         —           Output Capacitance         — 110         —	Gate-to-Source Charge         —         5.3         —         nC           Gate-to-Drain Charge         —         7.0         —           Turn-On Delay Time         —         10         —           Rise Time         —         40         —           Turn-Off Delay Time         —         26         —           Fall Time         —         24         —           Internal Drain Inductance         —         4.5         —           Input Capacitance Inductance         —         7.5         —           Input Capacitance         —         740         —           Output Capacitance         —         74         —           Output Capacitance         —         74         —           Output Capacitance         —         450         —           Output Capacitance         —         110         —

## **Diode Characteristics**

21040 011414001101100						
	Parameter	Min.	Тур.	Max.	Units	Conditions
L	Continuous Source Current			30		MOSFET symbol
IS	(Body Diode)			30	_	showing the
	Pulsed Source Current			120	A	integral reverse
I <sub>SM</sub>	(Body Diode) ①			120		p-n junction diode.
$V_{SD}$	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 18A, V_{GS} = 0V$ ③
t <sub>rr</sub>	Reverse Recovery Time		19	29	ns	$T_J = 25^{\circ}C$ , $I_F = 18A$ , $V_{DD} = 28V$
Q <sub>rr</sub>	Reverse Recovery Charge		14	21	nC	di/dt = 100A/µs③
t <sub>on</sub>	Forward Turn-On Time	Intrinsi	turn-or	n time is	negligil	ble (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )

## Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

- $\oplus$  C<sub>oss</sub> eff. is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>
- © Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting  $T_J = 25^{\circ}C$ , L = 0.18mH, R<sub>G</sub> = 25 $\Omega$ , I<sub>AS</sub> = 18A, V<sub>GS</sub> =10V.
- When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

 $\otimes$  R<sub>0</sub> is measured at T<sub>J</sub> approximately 90°C.



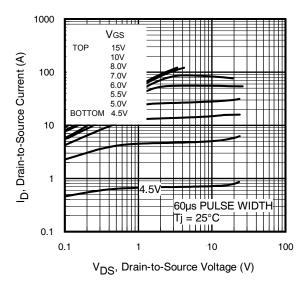


Fig. 1 Typical Output Characteristics

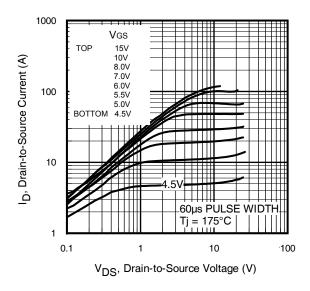


Fig. 2 Typical Output Characteristics

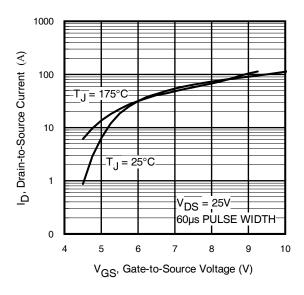
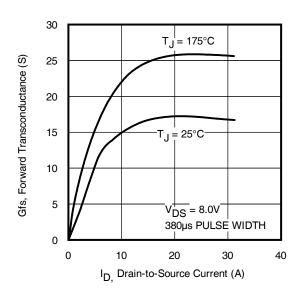
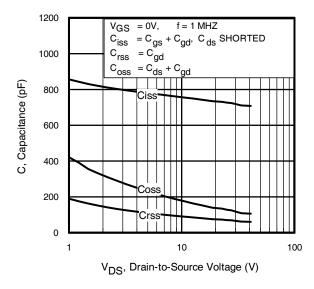


Fig. 3 Typical Transfer Characteristics

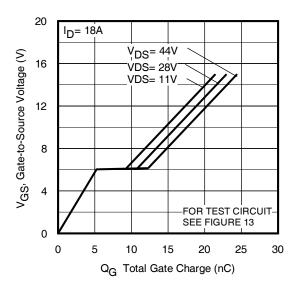


**Fig. 4** Typical Forward Trans conductance Vs. Drain Current





**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

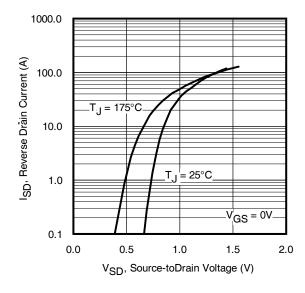


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

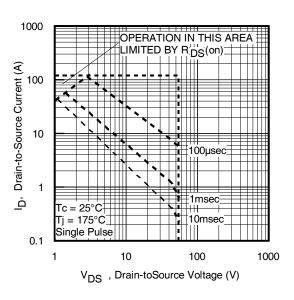
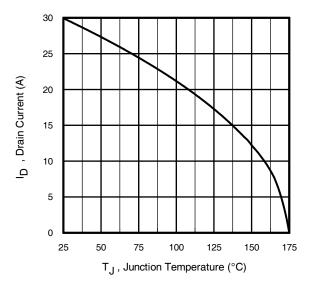
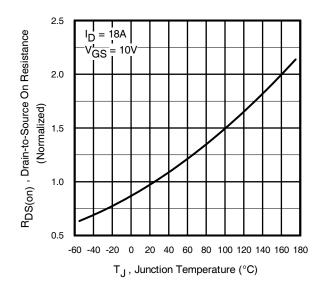


Fig 8. Maximum Safe Operating Area







**Fig 9.** Maximum Drain Current Vs. Case Temperature

**Fig 10.** Normalized On-Resistance Vs. Temperature

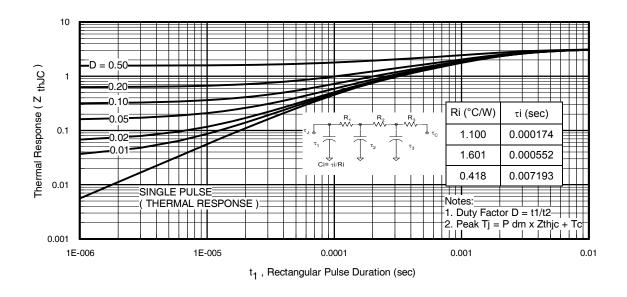


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



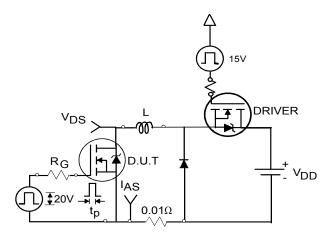


Fig 12a. Unclamped Inductive Test Circuit

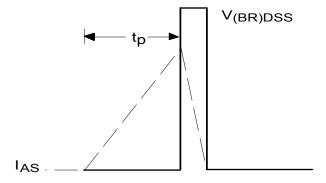


Fig 12b. Unclamped Inductive Waveforms

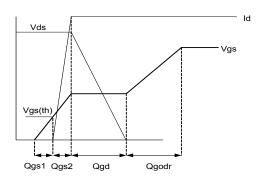


Fig 13a. Gate Charge Waveform

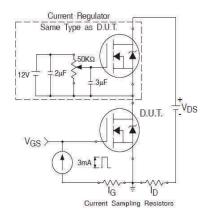
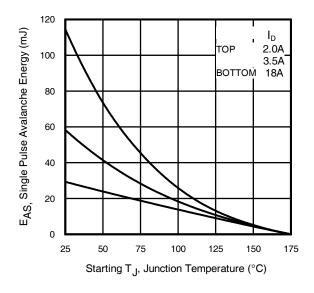


Fig 13b. Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

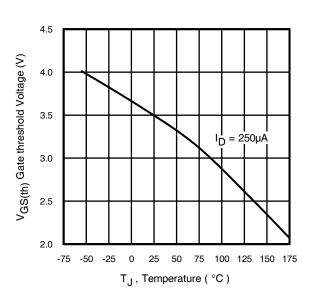


Fig 14. Threshold Voltage Vs. Temperature

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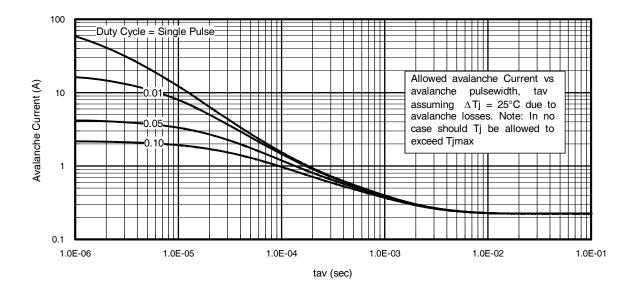
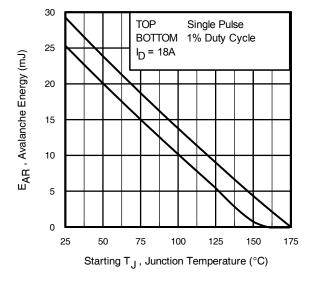


Fig 15. Typical Avalanche Current Vs. Pulse width



**Fig 16.** Maximum Avalanche Energy Vs. Temperature

## Notes on Repetitive Avalanche Curves , Figures 15, 16:

# (For further info, see AN-1005 at www.infineon.com)

- Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T<sub>imax</sub>. This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
- 4. PD (ave) = Average power dissipation per single avalanche pulse.
- 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. lav = Allowable avalanche current.
- 7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).

tav = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

ZthJC(D, tav) = Transient thermal resistance, see Figures 13)

$$\begin{split} P_{D \; (ave)} &= 1/2 \; (\; 1.3 \cdot BV \cdot I_{av}) = \Delta T / \; Z_{thJC} \\ I_{av} &= 2\Delta T / \; [1.3 \cdot BV \cdot Z_{th}] \\ E_{AS \; (AR)} &= P_{D \; (ave)} \cdot t_{av} \end{split}$$

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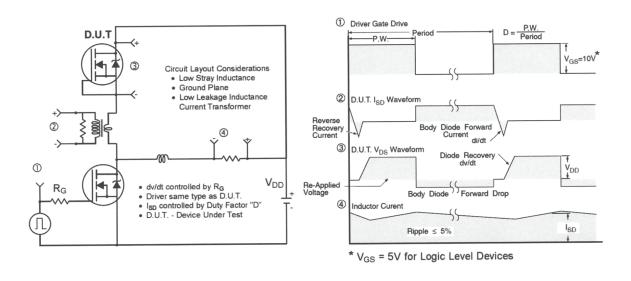


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

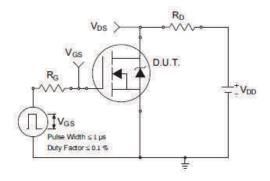


Fig 18a. Switching Time Test Circuit

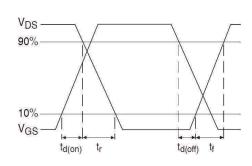
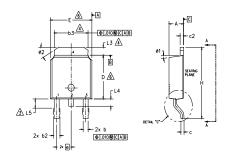


Fig 18b. Switching Time Waveforms

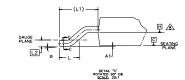
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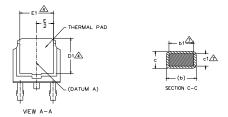


# D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))









#### NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 1 LEAD DIMENSION UNCONTROLLED IN L5.
- A- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- Limited Dimension D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- A- DIMENSION 61 & c1 APPLIED TO BASE METAL ONLY.
- ♠ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S			N		
M B O	MILLIM	ETERS	INC	HES	O T
O L	MIN.	MAX.	MIN.	MAX.	E S
Α	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
ь1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
С	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
Ε	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
е	2.29	BSC	.090	BSC	
Н	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74	BSC	.108 REF.		
L2	0.51	BSC	.020	BSC	
L3	0.89	1.27	.035	.050	4
L4	-	1.02	_	.040	
L5	1.14	1.52	.045	.060	3
ø	0.	10°	0,	10°	
ø1	0.	15*	0,	15*	
ø2	25*	35*	25*	35*	

## LEAD ASSIGNMENTS

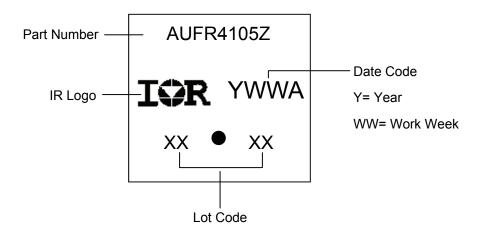
# **HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE 4.- DRAIN
- 4. DIVAII

#### IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER 4.- COLLECTOR

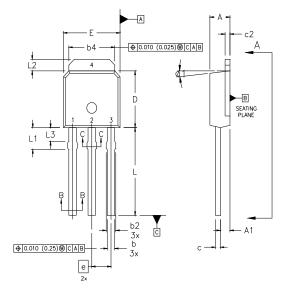
# D-Pak (TO-252AA) Part Marking Information

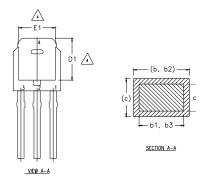


Note: For the most current drawing please refer to IR website at http://www.irf.com/package/



# I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches)





#### NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- JIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION 64, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION 61, 63 APPLY TO BASE METAL ONLY.
  OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- B CONTROLLING DIMENSION : INCHES.

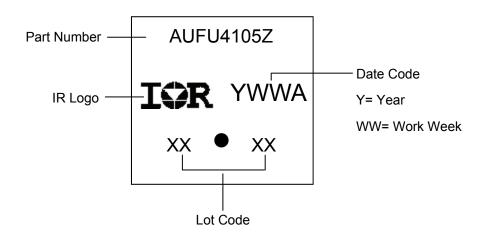
#### LEAD ASSIGNMENTS

ŀ	НE	X	F	Ε.	I
_					

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

SYMBOL	MILLIM	ETERS	INC	HES	
	MIN.	MAX.	MIN.	MAX.	NOTES
А	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
ь1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
С	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.	29	0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1,14	1.52	0.045	0.060	5
ø1	0*	15*	0*	15*	

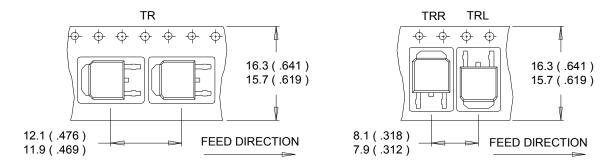
I-Pak (TO-251AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <a href="http://www.irf.com/package/">http://www.irf.com/package/</a>

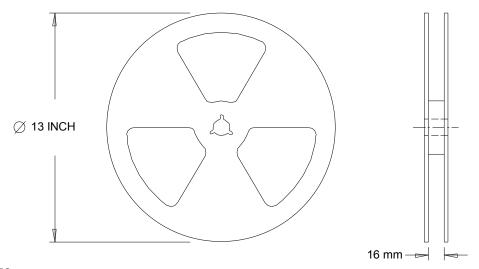


# D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))



#### NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



# NOTES:

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <a href="http://www.irf.com/package/">http://www.irf.com/package/</a>



#### **Qualification Information**

<u> </u>	don miorination					
Qualification Level		Automotive (per AEC-Q101)				
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.				
Moisture Sensitivity Level		D-Pak	MCI 4			
		I-Pak	MSL1			
	Machine Medal	Class M2 (+/-200V) <sup>†</sup>				
	Machine Model	AEC-Q101-002				
FOD	Liverson Dady Madal	Class H1A (+/-500V) <sup>†</sup>				
ESD	Human Body Model	AEC-Q101-001				
	Observed Davis Madal	Class C5 (+/-1125V) <sup>†</sup>				
Charged Device Model		AEC-Q101-005				
RoHS Compliant			Yes			
		1				

<sup>†</sup> Highest passing voltage.

# **Revision History**

Date	Comments
12/1/2015	Updated datasheet with corporate template
	Corrected ordering table on page 1.

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