±60V Fault Protected, 3.3V to 5V, ±20V Common-Mode Range, RS-485/RS-422 Transceivers with Cable Invert and ±15kV ESD

ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E, ISL32458E, ISL32459E

The ISL32450E through ISL32459E are 3.3V to 5V powered, fault protected, extended common-mode range differential transceivers for balanced communication. The RS-485 bus pins (driver outputs and receiver inputs) are protected against overvoltages up to ±60V, and against ±15kV ESD strikes. These transceivers operate in environments with common-mode voltages up to ±20V (exceeds the RS-485 requirement), making this RS-485 family one of the more robust on the market.

Transmitters are RS-485 compliant with $V_{CC} \geq 4.5V$ and deliver a 1.1V differential output voltage into the RS-485 specified 54Ω load even with $V_{CC} = 3V$. Receiver (Rx) inputs feature a "Full Fail-Safe" design, which ensures a logic-high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven (idle) bus. Rx full fail-safe operation is maintained even when the Rx input polarity is switched (cable invert function on ISL32457E and ISL32459E).

The ISL32457E and ISL32459E include a cable invert function that reverses the polarity of the Rx and Tx bus pins in case the cable is misconnected during installation.

See Table 1 on page 2 for key features and configurations by device number.

Related Literature

- ISL32470E, ISL32472E, ISL32475E, ISL32478E datasheet "Fault Protected, Extended Common Mode Range, RS-485/RS-422 Transceivers with ±16.5kV ESD"

Features

- Fault protected RS-485 bus pins . . . . . up to ±60V
- Extended common-mode range . . . . . ±20V larger than required for RS-485
- ±15kV HBM ESD protection on RS-485 bus pins
- Wide supply range . . . . . 3V to 5.5V
- Cable invert pin (ISL32457E and ISL32459E only) corrects for reversed cable connections while maintaining Rx full fail-safe functionality
- 1/4 unit load for up to 128 devices on the bus
- High transient overvoltage tolerance. . . . . ±80V
- Full fail-safe (open, short, terminated) RS-485 receivers
- Choice of RS-485 data rates . . . . . up to 20Mbps
- Low quiescent supply current 2.1mA

Applications

- Utility meters/automated meter reading systems
- Air conditioning systems
- Security camera networks
- Building lighting and environmental control systems
- Industrial/process control networks

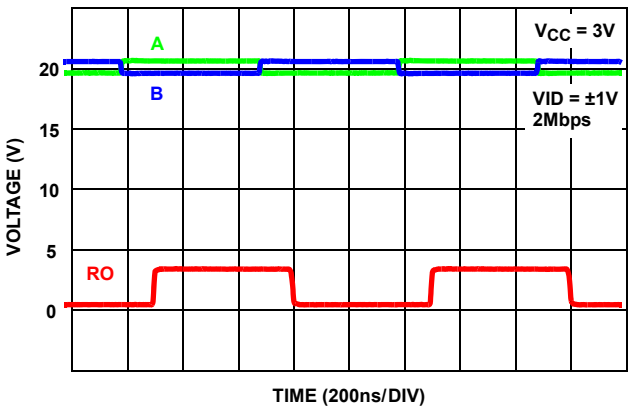


FIGURE 1. EXCEPTIONAL ISL32453E RX OPERATES AT >1Mbps EVEN WITH ±20V COMMON-MODE VOLTAGE

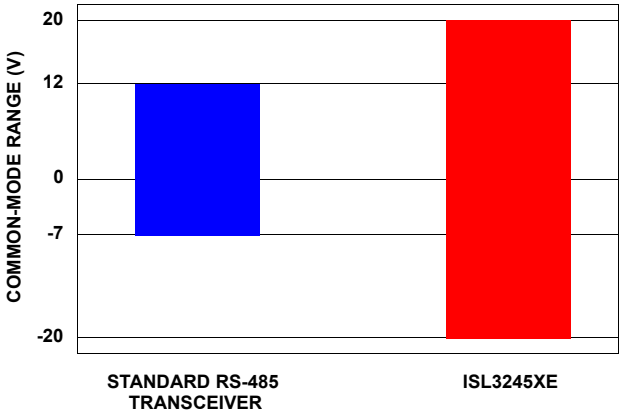


FIGURE 2. TRANSCEIVERS DELIVER SUPERIOR COMMON-MODE RANGE vs STANDARD RS-485 DEVICES

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED?	EN PINS?	HOT PLUG	CABLE INVERT (INV) PIN?	QUIESCENT I_{CC} (mA)	LOW POWER SHDN?	PIN COUNT
ISL32450E	Full	0.25	Yes	Yes	No	No	2.1	Yes	10, 14
ISL32452E	Half	0.25	Yes	Yes	No	No	2.1	Yes	8
ISL32453E	Full	1	Yes	Yes	No	No	2.1	Yes	10, 14
ISL32455E	Half	1	Yes	Yes	No	No	2.1	Yes	8
ISL32457E	Half	0.25	Yes	Tx Only	No	Yes	2.1	No	8
ISL32458E	Half	20	No	Yes	No	No	2.1	Yes	8
ISL32459E	Half	20	No	Tx Only	No	Yes	2.1	No	8

Ordering Information

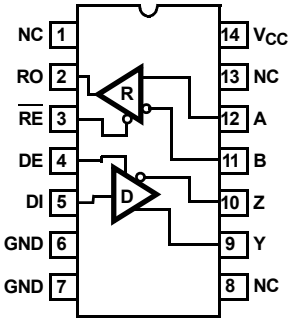
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL32450EIBZ	ISL32450 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL32450EIUZ	2450E	-40 to +85	10 Ld MSOP	M10.118
ISL32452EIBZ	32452 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32452EIUZ	2452E	-40 to +85	8 Ld MSOP	M8.118
ISL32453EIBZ	ISL32453 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL32453EIUZ	2453E	-40 to +85	10 Ld MSOP	M10.118
ISL32455EIBZ	32455 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32455EIUZ	2455E	-40 to +85	8 Ld MSOP	M8.118
ISL32457EIBZ	32457 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32457EIUZ	2457E	-40 to +85	8 Ld MSOP	M8.118
ISL32458EIBZ	32458 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32459EIBZ	32459 EIBZ	-40 to +85	8 Ld SOIC	M8.15

NOTES:

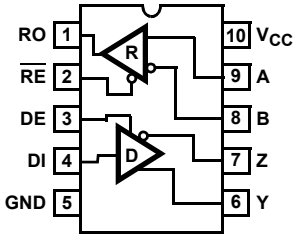
1. Add “-T” suffix for 2.5k unit or “-T7A” suffix for 250 unit Tape and Reel options. Please refer to Tech Brief TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information pages for ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E, ISL32458E, ISL32459E. For more information on MSL please see Tech Brief TB363.

Pin Configurations

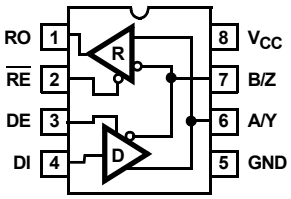
ISL32450E, ISL32453E
(14 LD SOIC)
TOP VIEW



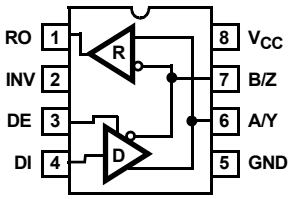
ISL32450E, ISL32453E
(10 LD MSOP)
TOP VIEW



ISL32452E, ISL32455E, ISL32458E
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



ISL32457E, ISL32459E
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



NOTE: Evaluate creepage and clearance requirements at your maximum fault voltage before using small pitch packages (e.g., MSOP).

Truth Tables

TRANSMITTING					
INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	INV (Note 4)	Y	Z
X	1	1	0	1	0
X	1	0	0	0	1
X	1	1	1	0	1
X	1	0	1	1	0
0	0	X	X	High-Z	High-Z
1	0	X	X	High-Z (Note 5)	High-Z (Note 5)

NOTES:

4. Parts without the INV pin follow the rows with INV = “0” and “X”.
5. Low Power Shutdown mode (see Notes 14 and 19).

RECEIVING					
INPUTS					OUTPUT
$\overline{RE}$ (Note 19)	DE (Half Duplex)	DE (Full Duplex)	A-B	INV (Note 4)	RO
0	0	X	≥ -0.01V	0	1
0	0	X	≤ -0.2V	0	0
0	0	X	≤ 0.01V	1	1
0	0	X	≥ 0.2V	1	0
0	0	X	Inputs Open or Shorted	X	1
1	0	0	X	X	High-Z (Note 5)
1	1	1	X	X	High-Z

Pin Descriptions

PIN NAME	ISL32450E, ISL32453E, (14 LD SOIC) PIN #	ISL32450E, ISL32453E, (10 LD MSOP) PIN #	ISL32452E, ISL32455E, ISL32458E (8 LD SOIC, 8 LD MSOP) PIN #	ISL32457E, ISL32459E (8 LD SOIC, 8 LD MSOP) PIN #	FUNCTION
RO	2	1	1	1	Receiver output. For parts without the cable invert function - or if INV is low - then: If A - B ≥ -10mV, RO is high; if A - B ≤ -200mV, RO is low. If INV is high, then: If B - A ≥ -10mV, RO is high; if B - A ≤ -200mV, RO is low. In all cases, RO = High if A and B are unconnected (floating), or shorted together, or connected to an undriven, terminated bus (i.e., Rx is always fail-safe open, shorted and idle, even if polarity is inverted).
$\overline{RE}$	3	2	2	N/A	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. Internally pulled low.
DE	4	3	3	3	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high and they are high impedance when DE is low. Internally pulled high.
DI	5	4	4	4	Driver input. For parts without the cable invert function - or if INV is low - a low on DI forces output Y low and output Z high, while a high on DI forces output Y high and output Z low. The output states, relative to DI, invert if INV is high.
GND	6, 7	5	5	5	Ground connection.
A/Y	N/A	N/A	6	6	±60V fault protected and ±16.5kV ESD protected RS-485/RS-422 I/O pin. For parts without the cable invert function - or if INV is low - A/Y is the noninverting receiver input and noninverting driver output. If INV is high, A/Y is the inverting receiver input and the inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
B/Z	N/A	N/A	7	7	±60V fault protected and ±16.5kV ESD protected RS-485/RS-422 I/O pin. For parts without the cable invert function - or if INV is low - B/Z is the inverting receiver input and inverting driver output. If INV is high, B/Z is the noninverting receiver input and the noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	12	9	N/A	N/A	±60V fault protected and ±15kV ESD protected RS-485/RS-422 noninverting receiver input.
B	11	8	N/A	N/A	±60V fault protected and ±15kV ESD protected RS-485/RS-422 inverting receiver input.
Y	9	6	N/A	N/A	±60V fault protected and ±15kV ESD protected RS-485/RS-422 noninverting driver output.
Z	10	7	N/A	N/A	±60V fault protected and ±15kV ESD protected RS-485/RS-422 inverting driver output.
V_{CC}	14	10	8	8	System power supply input (3V to 5.5V).
INV	N/A	N/A	N/A	2	Receiver and driver cable invert (polarity selection) input. When driven high this pin swaps the polarity of the driver output and receiver input pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.
NC	1, 8, 13	N/A	N/A	N/A	No internal connection.

Typical Operating Circuits

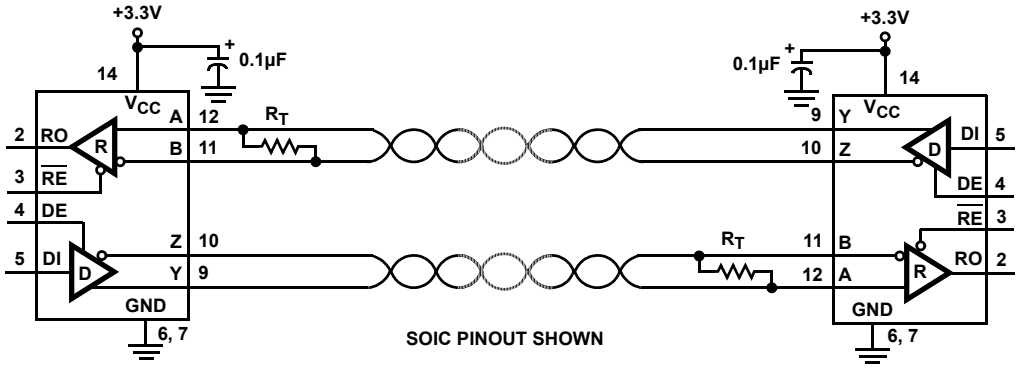


FIGURE 3. ISL32450E, ISL32453E FULL DUPLEX NETWORK

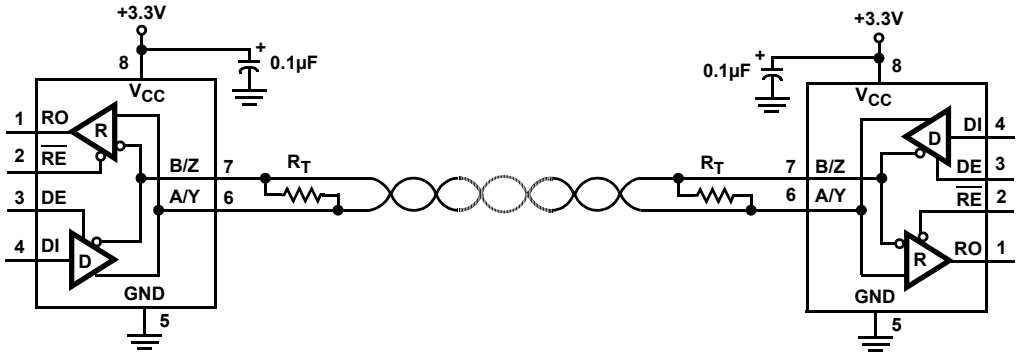


FIGURE 4. ISL32452E, ISL32455E, ISL32458E HALF DUPLEX NETWORK

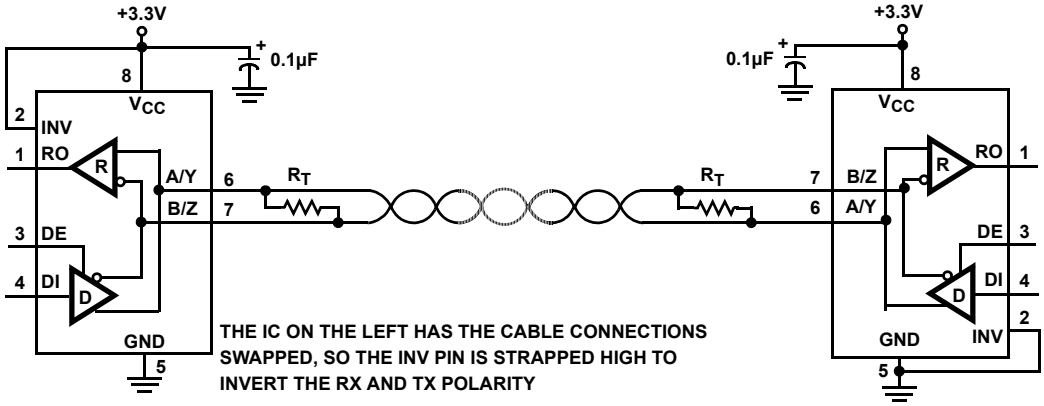


FIGURE 5. ISL32457E, ISL32459E HALF DUPLEX NETWORK USING CABLE INVERT FUNCTION

Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$, INV. . . . . -0.3V to V_{CC} + 0.3V
Input/Output Voltages
A/Y, B/Z, A, B, Y, Z . . . . . ±60V
A/Y, B/Z, A, B, Y, Z
(Transient Pulse Through 100Ω, Note 6) . . . . . ±80V
RO. . . . . -0.3V to (V_{CC} +0.3V)
Short-Circuit Duration
Y, Z . . . . . Indefinite
ESD Rating . . . . . see "Electrical Specifications"
Latch-Up (per JESD78, Level 2, Class A) . . . . . +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 7, 8)	108	47
8 Ld MSOP Package (Notes 7, 8)	140	40
10 Ld MSOP Package (Notes 7, 8)	135	50
14 Ld SOIC Package (Notes 7, 8)	88	39

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage (V_{CC}). . . . . 3.3V or 5V
Temperature Range . . . . . -40°C to +85°C
Bus Pin Common-Mode Voltage Range. . . . . -20V to +20V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Tested according to TIA/EIA-485-A, Section 4.2.6 (±80V for 15µs at a 1% duty cycle).
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V, unless otherwise specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 9). **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
DC CHARACTERISTICS							
Driver Differential V_{OUT} (No load)	V_{OD1}		Full	-	-	**V_{CC}**	V
Driver Differential V_{OUT} (Loaded, Figure 6A)	V_{OD2}	R_L = 100Ω (RS-422), V_{CC} ≥ 4.5V	Full	**2**	3	-	V
		R_L = 54Ω (RS-485), V_{CC} ≥ 4.5V	Full	**1.7**	2.3	**V_{CC}**	V
		R_L = 54Ω (RS-485), V_{CC} ≥ 3V	Full	**1.1**	1.3	**V_{CC}**	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 6A)	Full	-	-	**0.2**	V
Driver Differential V_{OUT} with Common-Mode Load (Figure 6B)	V_{OD3}	R_L = 60Ω, -20V ≤ V_{CM} ≤ 20V, V_{CC} ≥ 4.5V	Full	**1.5**	-	-	V
Driver Common-Mode V_{OUT} (Figure 6A)	V_{OC}	R_L = 54Ω or 100Ω	Full	**-1**	-	**3**	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 6A)	Full	-	-	**0.2**	V
Driver Short-Circuit Current	I_{OSD}	DE = V_{CC}, -20V ≤ V_O ≤ 20V (Note 11)	Full	**-250**	-	**250**	mA
	I_{OSD1}	At first fold-back, 24V ≤ V_O ≤ -24V	Full	**-83**	-	**83**	mA
	I_{OSD2}	At second fold-back, 35V ≤ V_O ≤ -35V	Full	**-13**	-	**13**	mA
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$, INV (See Figure 33)	Full	**2.35**	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$, INV	Full	-	-	**0.8**	V
Logic Input Current	I_{IN1}	DI	Full	**-1**	-	**1**	µA
		DE, $\overline{RE}$, INV	Full	**-15**	6	**15**	µA

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V, unless otherwise specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 9). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
Input/Output Current (A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 3.6V or 5.5V	V_{IN} = 12V	Full	-	-	**250**	µA
			V_{IN} = -7V	Full	**-200**	-	-	µA
			V_{IN} = ±20V	Full	**-800**	-	**850**	µA
			V_{IN} = ±60V, (Note 18)	Full	**-6**	-	**6**	mA
Input Current (A, B) (Full Duplex Versions Only)	I_{IN3}	V_{CC} = 0V or 3.6V or 5.5V	V_{IN} = 12V	Full	-	-	**125**	µA
			V_{IN} = -7V	Full	**-100**	-	-	µA
			V_{IN} = ±20V	Full	**-500**	-	**500**	µA
			V_{IN} = ±60V, (Note 18)	Full	**-3**	-	**3**	mA
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{OZD}	$\overline{RE}$ = 0V, DE = 0V, V_{CC} = 0V or 3.6V or 5.5V	V_{IN} = 12V	Full	-	-	**200**	µA
			V_{IN} = -7V	Full	**-100**	-	-	µA
			V_{IN} = ±20V	Full	**-500**	-	**500**	µA
			V_{IN} = ±60V, (Note 18)	Full	**-3**	-	**3**	mA
Receiver Differential Threshold Voltage	V_{TH}	-20V ≤ V_{CM} ≤ 20V, (For ISL32457E and ISL32459E only, A-B if INV = 0; B-A if INV = 1)	V_{CC} ≤ 3.6V	Full	**-200**	-120	**-10**	mV
			V_{CC} ≥ 4.5V	Full	**-250**	-180	**-10**	mV
Receiver Input Hysteresis	ΔV_{TH}	-20V ≤ V_{CM} ≤ 20V		+25	-	30	-	mV
Receiver Output High Voltage	V_{OH1}	V_{ID} = -10mV	I_O = -4mA, V_{CC} ≥ 3V	Full	**2.4**	-	-	V
	V_{OH2}		I_O = -8mA, V_{CC} ≥ 4.5V	Full	**2.4**	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{CC} ≥ 3V, V_{ID} = -200mV		Full	-	-	**0.4**	V
		I_O = 5mA, V_{CC} ≥ 4.5V, V_{ID} = -250mV		Full	-	-	**0.4**	V
Three-State (High Impedance) Receiver Output Current (Note 19)	I_{OZR}	0V ≤ V_O ≤ V_{CC}		Full	**-1**	0.01	**1**	µA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	-	-	**±115**	mA
SUPPLY CURRENT								
No-Load Supply Current (Note 10)	I_{CC}	DE = V_{CC}, $\overline{RE}$ = 0V or V_{CC}, DI = 0V or V_{CC}		Full	-	2.1	**4.5**	mA
Shutdown Supply Current (Note 19)	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	10	**35**	µA
ESD PERFORMANCE								
All Pins		Human Body Model (ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E; Tested per JESD22-A114E)		+25	-	±8	-	kV
		Human Body Model (ISL32458E, ISL32459E; Tested per JESD22-A114E)		+25	-	±3	-	kV
		Machine Model (Tested per JESD22-A115-A)		+25	-	±700	-	V
RS-485 Pins (A, B, Y, Z, A/Y, B/Z)		Human Body Model, From Bus Pins to GND	Full Duplex	+25	-	±15	-	kV
			Half Duplex	+25	-	±16.5	-	kV

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V, unless otherwise specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 9). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
DRIVER SWITCHING CHARACTERISTICS (250kbps VERSIONS; ISL32450E, ISL32452E, ISL32457E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	-	280	**1000**	ns
Driver Differential Output Skew	t_{SKEW}	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	-	4	**100**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	**250**	650	**1500**	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 9)	Full	**250**	-	**-**	kbps
Driver Enable to Output High	t_{ZH}	SW = GND (Figure 8), (Note 12)	Full	-	-	**1600**	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (Figure 8), (Note 12)	Full	-	-	**1600**	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (Figure 8)	Full	-	-	**300**	ns
Driver Disable from Output High	t_{HZ}	SW = GND (Figure 8)	Full	-	-	**300**	ns
Time to Shutdown	t_{SHDN}	(Notes 14, 19)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	SW = GND (Figure 8), (Notes 14, 15, 19)	Full	-	-	**3000**	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	SW = V_{CC} (Figure 8), (Notes 14, 15, 19)	Full	-	-	**3000**	ns
DRIVER SWITCHING CHARACTERISTICS (1Mbps VERSIONS; ISL32453E, ISL32455E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	-	70	**200**	ns
Driver Differential Output Skew	t_{SKEW}	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	-	4	**25**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	**50**	130	**300**	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 9)	Full	**1**	-	-	Mbps
Driver Enable to Output High	t_{ZH}	SW = GND (Figure 8), (Note 12)	Full	-	-	**300**	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (Figure 8), (Note 12)	Full	-	-	**300**	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (Figure 8)	Full	-	-	**300**	ns
Driver Disable from Output High	t_{HZ}	SW = GND (Figure 8)	Full	-	-	**300**	ns
Time to Shutdown	t_{SHDN}	(Note 14)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	SW = GND (Figure 8), (Notes 14, 15)	Full	-	-	**3000**	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	SW = V_{CC} (Figure 8), (Notes 14, 15)	Full	-	-	**3000**	ns
DRIVER SWITCHING CHARACTERISTICS (20Mbps VERSIONS; ISL32458E, ISL32459E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	-	28	**45**	ns
Driver Differential Output Skew	t_{SKEW}	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	-	3	**9**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_D = 54Ω, C_D = 50pF (Figure 7)	Full	-	17	**35**	ns
Maximum Data Rate	f_{MAX}	C_D = 470pF (Figure 9)	Full	**20**	-	-	Mbps
Driver Enable to Output High	t_{ZH}	SW = GND (Figure 8), (Note 12)	Full	-	-	**180**	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (Figure 8), (Note 12)	Full	-	-	**180**	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (Figure 8)	Full	-	-	**300**	ns
Driver Disable from Output High	t_{HZ}	SW = GND (Figure 8)	Full	-	-	**300**	ns
Time to Shutdown	t_{SHDN}	(Notes 14, 19)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	SW = GND (Figure 8), (Notes 14, 15, 19)	Full	-	-	**3000**	ns

Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V, unless otherwise specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 9). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	SW = V_{CC} (Figure 8), (Notes 14, 15, 19)	Full	-	-	**3000**	ns
RECEIVER SWITCHING CHARACTERISTICS (250kbps VERSIONS; ISL32450E, ISL32452E, ISL32457E)							
Maximum Data Rate	f_{MAX}	(Figure 10)	Full	**250**	-	-	kbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 10)	Full	-	240	**325**	ns
Receiver Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKD}	(Figure 10)	Full	-	6	**25**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Notes 13, 19)	Full	-	-	**80**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Notes 13, 19)	Full	-	-	**80**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Note 19)	Full	-	-	**80**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Note 19)	Full	-	-	**80**	ns
Time to Shutdown	t_{SHDN}	(Notes 14, 19)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Notes 14, 16, 19)	Full	-	-	**2500**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Notes 14, 16, 19)	Full	-	-	**2500**	ns
RECEIVER SWITCHING CHARACTERISTICS (1Mbps VERSIONS; ISL32453E, ISL32455E)							
Maximum Data Rate	f_{MAX}	(Figure 10)	Full	**1**	-	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 10)	Full	-	115	**200**	ns
Receiver Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKD}	(Figure 10)	Full	-	4	**20**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Note 13)	Full	-	-	**80**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Note 13)	Full	-	-	**80**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11)	Full	-	-	**80**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11)	Full	-	-	**80**	ns
Time to Shutdown	t_{SHDN}	(Note 14)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Notes 14, 16)	Full	-	-	**2500**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Notes 14, 16)	Full	-	-	**2500**	ns
RECEIVER SWITCHING CHARACTERISTICS (20Mbps VERSIONS; ISL32458E, ISL32459E)							
Maximum Data Rate	f_{MAX}	(Figure 10)	Full	**20**	-	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 10)	Full	-	40	**80**	ns
Receiver Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKD}	(Figure 10)	Full	-	3	**9**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Notes 13, 19)	Full	-	-	**80**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Notes 13, 19)	Full	-	-	**80**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Note 19)	Full	-	-	**80**	ns

Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V, unless otherwise specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 9). **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 17)	TYP	MAX (Note 17)	UNIT
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Note 19)	Full	-	-	**80**	ns
Time to Shutdown	t_{SHDN}	(Notes 14, 19)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 11), (Notes 14, 16, 19)	Full	-	-	**2500**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 11), (Notes 14, 16, 19)	Full	-	-	**2500**	ns

NOTES:

9. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
10. Supply current specification is valid for loaded drivers when DE = 0V.
11. Applies to peak current. See "Typical Performance Curves" beginning on page 15 for more information.
12. Keep $\overline{RE}$ = 0 to prevent the device from entering SHDN (does not apply to the ISL32457E and ISL32459E).
13. The $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
14. Transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See "Low Power Shutdown Mode" on page 14
15. Keep $\overline{RE}$ = VCC, and set the DE signal low time >600ns to ensure that the device enters SHDN.
16. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
17. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.
18. See "Caution" statement below the "Recommended Operating Conditions" on page 6.
19. Does not apply to the ISL32457E and ISL32459E. These transceivers have no Rx enable function, and thus no SHDN function.

Test Circuits and Waveforms

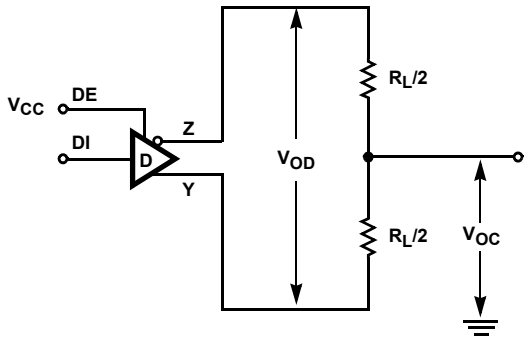


FIGURE 6A. V_{OD} AND V_{OC}

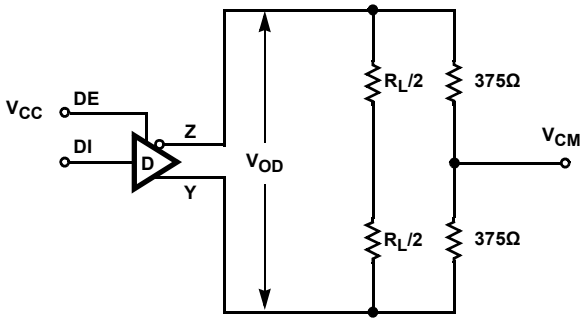


FIGURE 6B. V_{OD} WITH COMMON-MODE LOAD

FIGURE 6. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

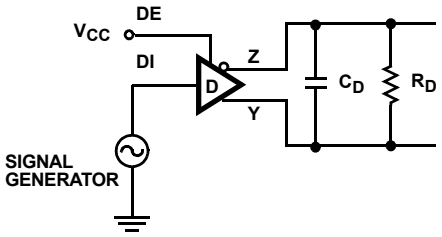


FIGURE 7A. TEST CIRCUIT

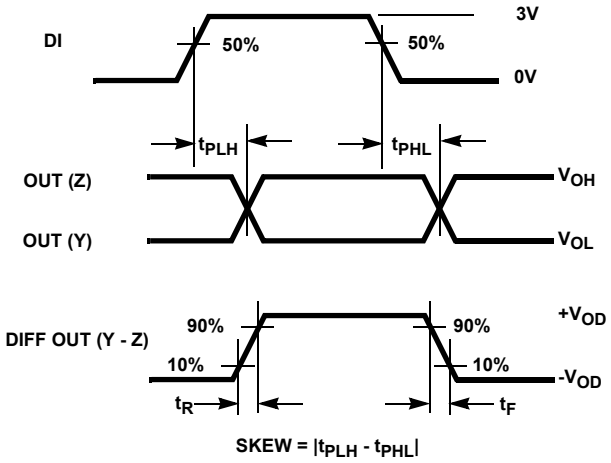
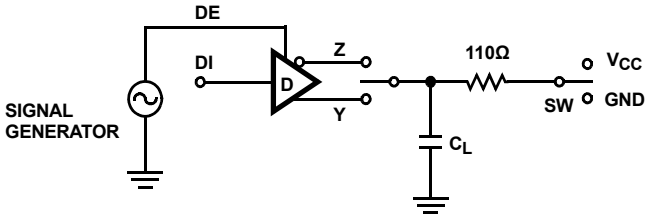


FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	50
t_{LZ}	Y/Z	X	0/1	V_{CC}	50
t_{ZH}	Y/Z	0 (Note 12)	1/0	GND	100
t_{ZL}	Y/Z	0 (Note 12)	0/1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 15)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 15)	0/1	V_{CC}	100

FIGURE 8A. TEST CIRCUIT

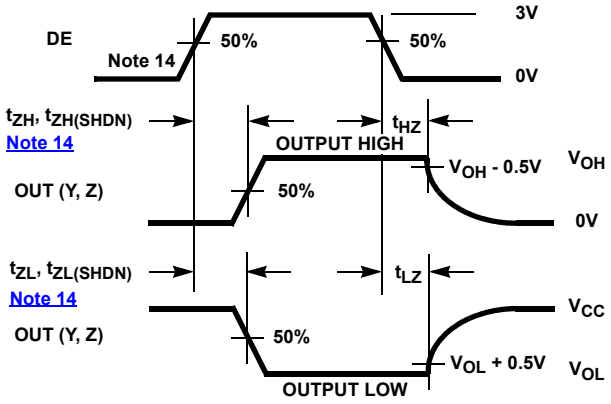


FIGURE 8B. MEASUREMENT POINTS

FIGURE 8. DRIVER ENABLE AND DISABLE TIMES

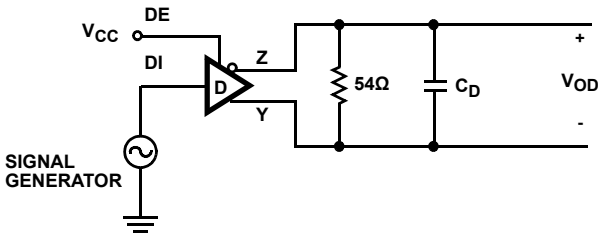


FIGURE 9A. TEST CIRCUIT

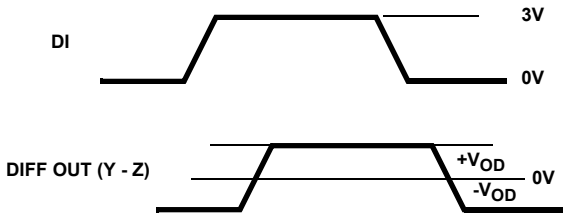


FIGURE 9B. MEASUREMENT POINTS

FIGURE 9. DRIVER DATA RATE

Test Circuits and Waveforms (Continued)

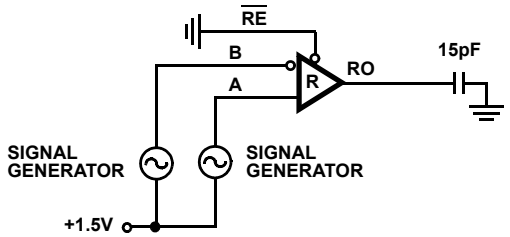


FIGURE 10A. TEST CIRCUIT

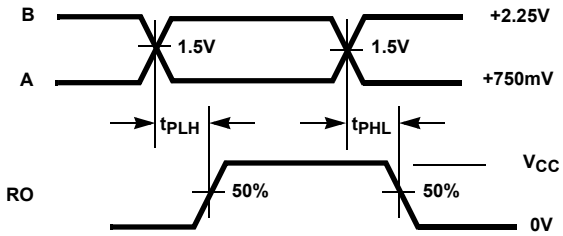
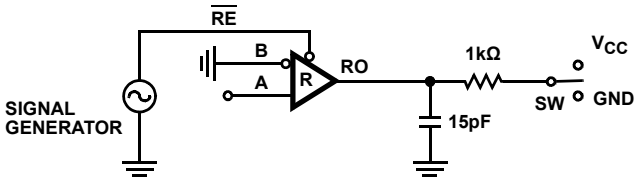


FIGURE 10B. MEASUREMENT POINTS

FIGURE 10. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 13)	0	+1.5V	GND
t_{ZL} (Note 13)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 16)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 16)	0	-1.5V	V_{CC}

FIGURE 11A. TEST CIRCUIT

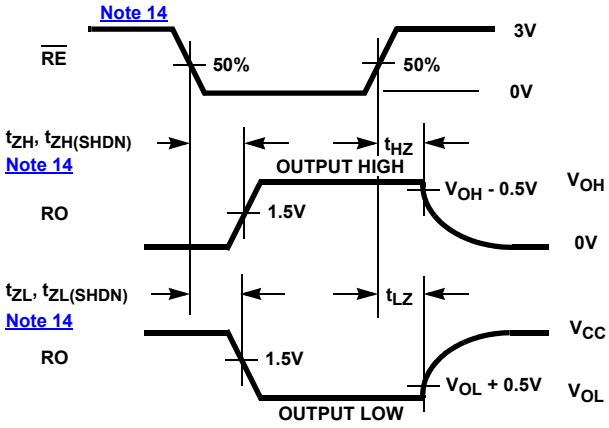


FIGURE 11B. MEASUREMENT POINTS

FIGURE 11. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards used for long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common-mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000 feet; thus, the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

The ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E, ISL32458E, ISL32459E are a family of ruggedized RS-485 transceivers that improve on the RS-485 basic requirements and therefore increases system reliability. The CMR increases to ±20V, while the RS-485 bus pins (receiver inputs and driver outputs) include fault protection against voltages and transients up to ±60V. Additionally, the ±15kV to ±16.5kV built-in ESD protection complements the fault protection.

Receiver (Rx) Features

These devices utilize a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is better than ±200mV (3.3V operation), as required by the RS-422 and RS-485 specifications.

Receiver input (load) current surpasses the RS-422 specification of 3mA, and is four times lower than the RS-485 “Unit Load (UL)” requirement of 1mA maximum. Thus, these products are known as “one-quarter UL” transceivers, and there can be up to 128 of these devices on a network while still complying with the RS-485 loading specification.

The Rx functions with common-mode voltages as great as ±20V, making them ideal for industrial or long networks where induced voltages are a realistic concern.

All the receivers include a “full fail-safe” function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled (i.e., an idle bus).

Receivers easily meet the data rates supported by the corresponding driver, and most receiver outputs are tri-statable via the active low $\overline{RE}$ input.

The Rx in the 250kbps and 1Mbps versions include noise filtering circuitry to reject high frequency signals. The 1Mbps version typically rejects pulses narrower than 50ns (equivalent to 20Mbps), while the 250kbps Rx rejects pulses below 150ns (6.7Mbps). The 20Mbps versions have no Rx noise filtering.

Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.7V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422) with $V_{CC} \geq 4.5V$. The drivers feature low propagation delay skew to maximize bit width and to minimize EMI, and all drivers are tri-statable via the active high DE input.

The 250kbps and 1Mbps driver outputs are slew rate limited to minimize EMI and to minimize reflections in unterminated or improperly terminated networks. Outputs of the ISL32458E and ISL32459E drivers are not limited; thus, faster output transition times allow data rates of at least 20Mbps.

High Overvoltage (Fault) Protection Increases Ruggedness

NOTE: The available smaller pitch package (MSOP) may not meet the Creepage and Clearance (C&C) requirements for ±60V levels. The user is advised to determine his C&C requirements before selecting a package type.

The ±60V (referenced to the IC GND) fault protection on the RS-485 pins makes these transceivers some of the most rugged on the market. This level of protection makes the ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E, ISL32458E, ISL32459E ideal for applications in which power (e.g., 24V and 48V supplies) must be routed in the conduit with the data lines and for outdoor applications where large transients are likely to occur. When power is routed with the data lines, even a momentary short between the supply and data lines will destroy an unprotected device. The ±60V fault levels of this family are *at least four times higher* than the levels specified for standard RS-485 ICs. The ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E, ISL32458E, ISL32459E protection is active whether the Tx is enabled or disabled, and even if the IC is powered down.

If transients or voltages (including overshoots and ringing) greater than ±60V are possible, then additional external protection is required. Use a protection device with the lowest clamping voltage acceptable for the application, and remember that TVS type devices typically clamp 5V to 10V above the designated stand-off voltage (e.g., a “54V TVS” clamps between 60V and 66V).

Wide Common-Mode Voltage (CMV) Tolerance Improves Operating Range

RS-485 networks operating in industrial complexes or over long distances are susceptible to large CMV variations. Either of these operating environments may suffer from large node-to-node ground potential differences or CMV pickup from external electromagnetic sources, and devices with only the minimum required +12V to -7V CMR may malfunction. The ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E, ISL32458E, ISL32459E extended ±20V CMR allows for operation in environments that would overwhelm lesser transceivers. Additionally, the Rx will not phase invert (erroneously change state) even with CMVs of ±25V or differential voltages as large as 40V.

Cable Invert (Polarity Reversal) Function

With large node count RS-485 networks, it is common for some cable data lines to be wired backwards during installation. When this happens, the node is unable to communicate over the network. Once a technician finds the miswired node, he must then rewire the connector, which is time consuming.

The ISL32457E and ISL32459E simplify this task by including a cable invert pin (INV) that allows the technician to invert the polarity of the Rx input and the Tx output pins simply by moving a jumper to change the state of the invert pin. When the invert pin is low, the IC operates like any standard RS-485 transceiver, and the bus pins have their normal polarity definition of A and Y as noninverting and B and Z as inverting. With the invert pin high, the corresponding bus pins reverse their polarity, so B and Z become noninverting, and A and Y become inverting.

Intersil's unique cable invert function is superior to that found on competing devices, because the Rx full fail-safe function is maintained, even when the Rx polarity is reversed. Competitor devices implement the Rx invert function simply by inverting the Rx output. This means that with the Rx inputs floating or shorted together, the Rx appropriately delivers a logic 1 in normal polarity, but outputs a logic low when the IC is operated in the inverted mode. Intersil's innovative Rx design guarantees that, with the Rx inputs floating or shorted together (V_{ID} = 0V), the Rx output remains high, regardless of the state of the invert pin.

Data Rate, Cables and Terminations

RS-485/RS-422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. High speed versions operating at 20Mbps may be used at lengths up to 150ft (46m), but the distance can be increased to 328ft (100m) by operating them at 5Mbps. 1Mbps versions can operate at full data rates with lengths up to 800ft (244m). Jitter is the limiting parameter at faster data rates, and may limit the network to shorter lengths, so employing encoded data streams (e.g., Manchester coded or Return-to-Zero) may allow increased transmission distances. The slow versions can operate at 115kbps or less at the full 4000ft (1220m) distance, or at 250kbps for lengths up to 3000ft (915m). DC cable attenuation is the limiting parameter, so using better quality cables (e.g., 22 AWG) may allow increased transmission distance.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

To minimize reflections, proper termination is imperative when using the 20Mbps devices. Short networks using the 250kbps versions need not be terminated; however, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point or point-to-multireceiver (single driver on bus like RS-422) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multireceiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multidriver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst-case bus contentions undamaged. These transceivers meet this requirement via driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate a double fold-back short-circuit current limiting scheme, which ensures that the output current never exceeds the RS-485 specification, even at the common-mode and fault condition voltage range extremes. The first fold-back current level (≈83mA) is set to ensure that the driver never folds back when driving loads with common-mode voltages up to ±20V. The very low second fold-back current setting (≈13mA) minimizes power dissipation if the Tx is enabled when a fault occurs.

In the event of a major short-circuit condition, devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about +15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode

These BiCMOS transceivers all use a fraction of the power required by competitive devices, but they (excluding ISL32457E and ISL32459E) also include a shutdown feature that reduces the already low quiescent I_{CC} to a 10µA trickle. These devices enter shutdown whenever the receiver and driver are *simultaneously* disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 12, 13, 14, 15 and 16, at the end of the "Electrical Specification" table on page 10, for more information.

Typical Performance Curves

T_A = +25°C; unless otherwise specified.

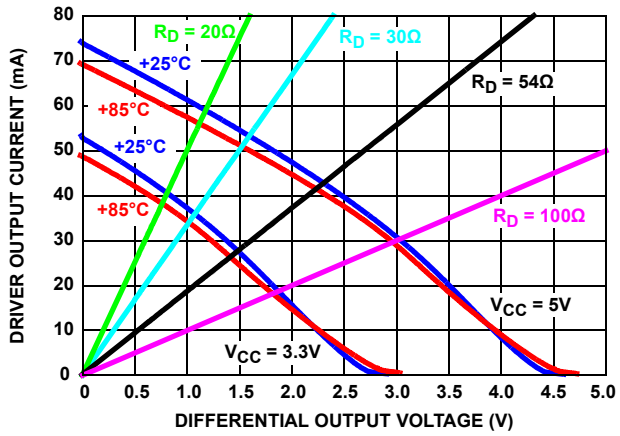


FIGURE 12. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

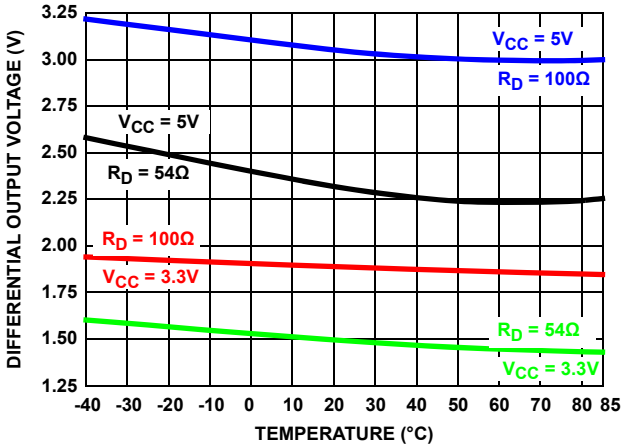


FIGURE 13. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

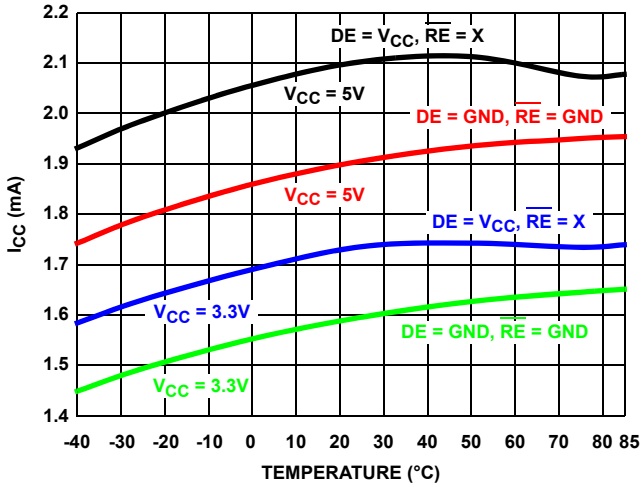


FIGURE 14. SUPPLY CURRENT vs TEMPERATURE

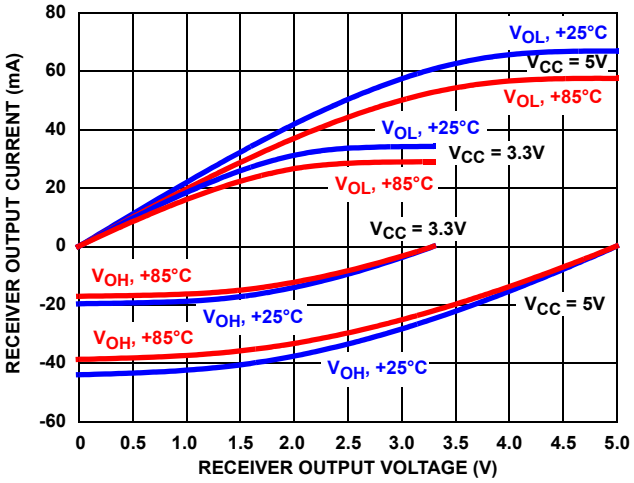


FIGURE 15. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

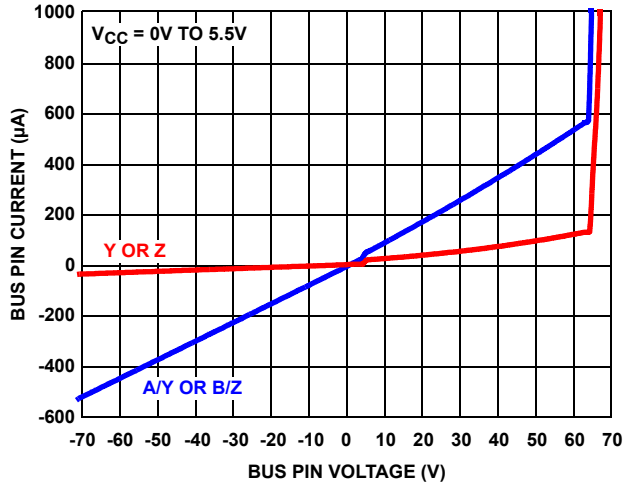


FIGURE 16. BUS PIN CURRENT vs BUS PIN VOLTAGE

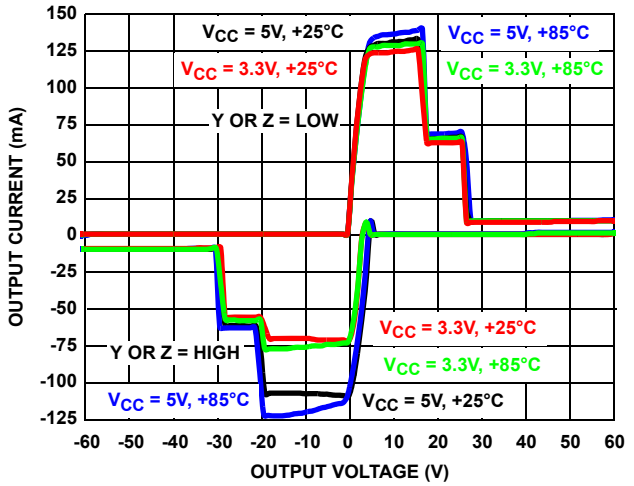


FIGURE 17. DRIVER OUTPUT CURRENT vs SHORT-CIRCUIT VOLTAGE

Typical Performance Curves

T_A = +25°C; unless otherwise specified. **(Continued)**

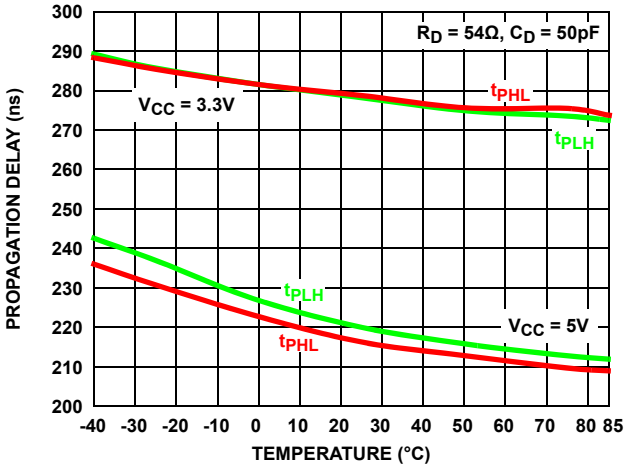


FIGURE 18. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32450E, ISL32452E, ISL32457E)

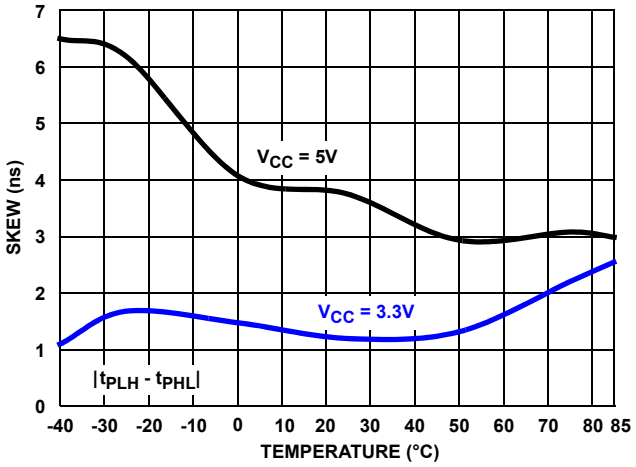


FIGURE 19. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32450E, ISL32452E, ISL32457E)

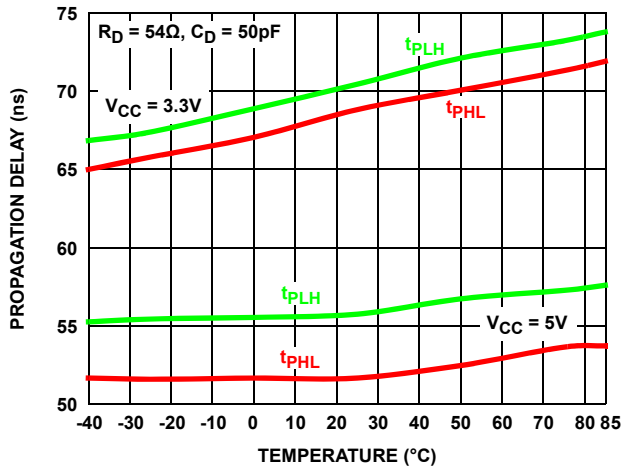


FIGURE 20. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32453E, ISL32455E)

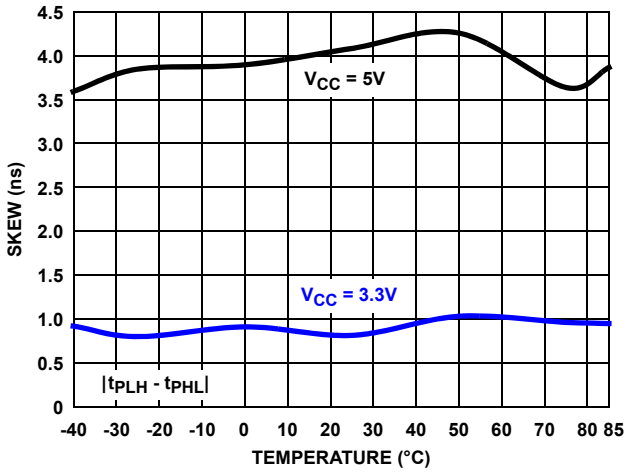


FIGURE 21. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32453E, ISL32455E)

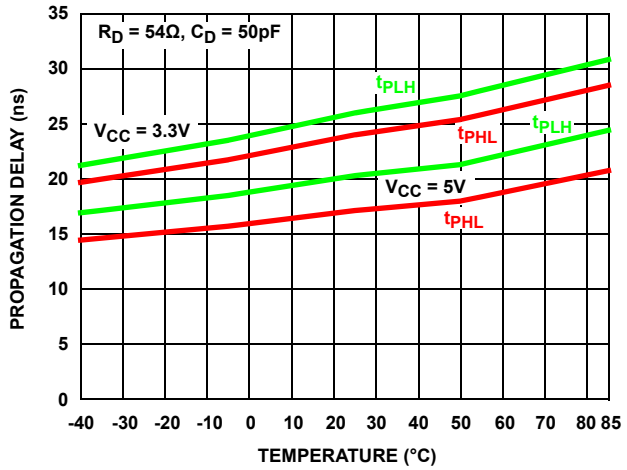


FIGURE 22. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32458E, ISL32459E)

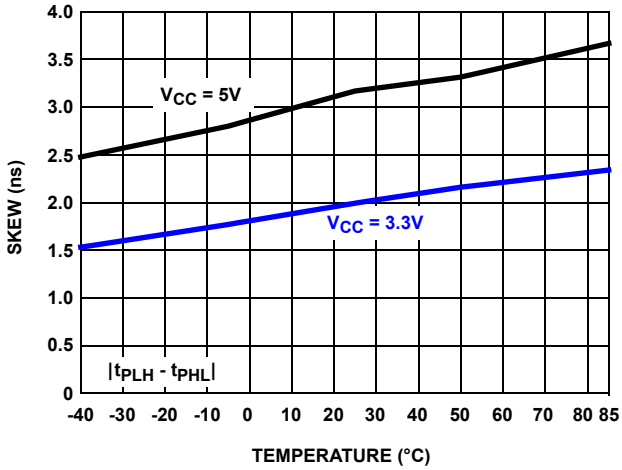


FIGURE 23. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32458E, ISL32459E)

Typical Performance Curves

T_A = +25°C; unless otherwise specified. **(Continued)**

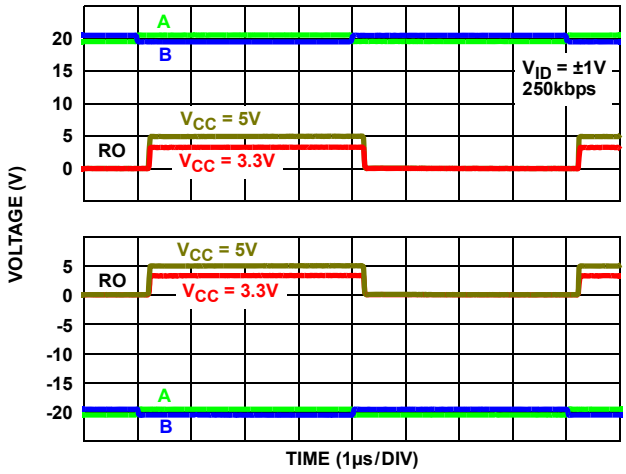


FIGURE 24. ±20V RECEIVER PERFORMANCE (ISL32450E, ISL32452E, ISL32457E)

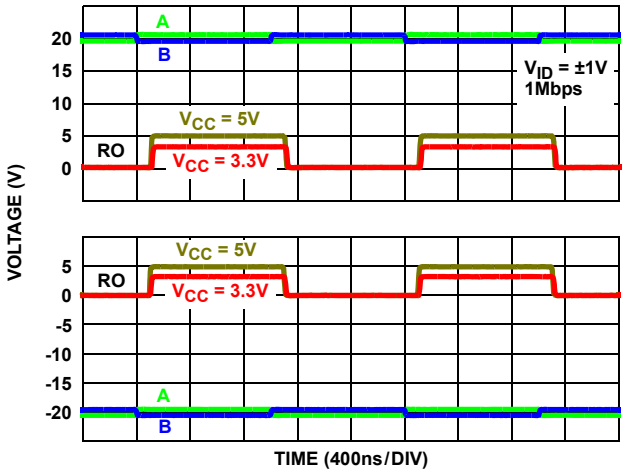


FIGURE 25. ±20V RECEIVER PERFORMANCE (ISL32453E, ISL32455E)

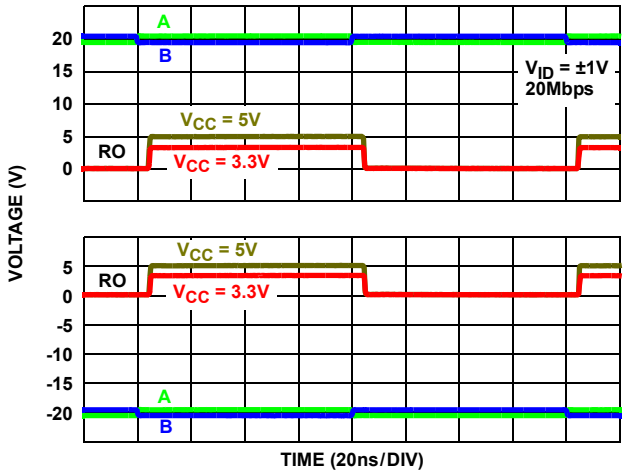


FIGURE 26. ±20V RECEIVER PERFORMANCE (ISL32458E, ISL32459E)

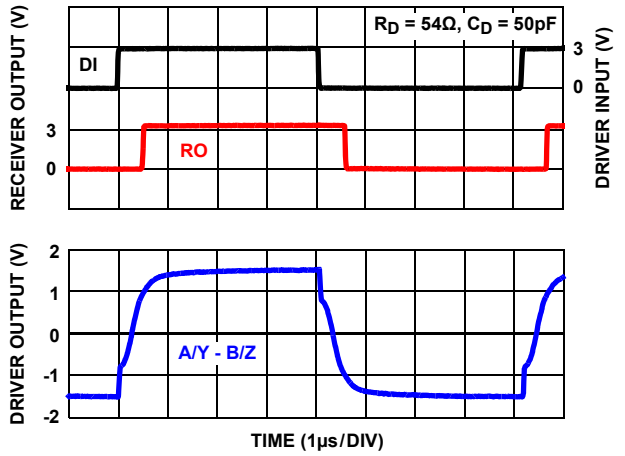


FIGURE 27. V_{CC} = 3.3V, DRIVER AND RECEIVER WAVEFORMS (ISL32450E, ISL32452E, ISL32457E)

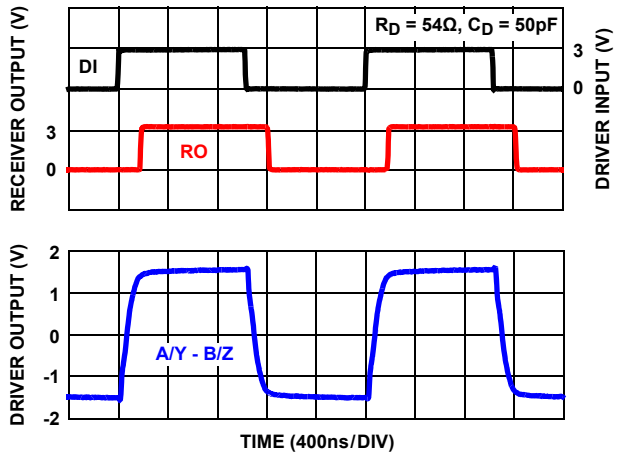


FIGURE 28. V_{CC} = 3.3V, DRIVER AND RECEIVER WAVEFORMS (ISL32453E, ISL32455E)

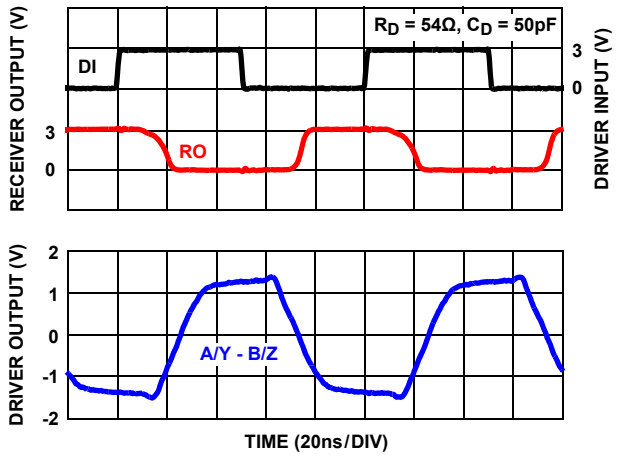


FIGURE 29. V_{CC} = 3.3V, DRIVER AND RECEIVER WAVEFORMS (ISL32458E, ISL32459E)

Typical Performance Curves

T_A = +25°C; unless otherwise specified. **(Continued)**

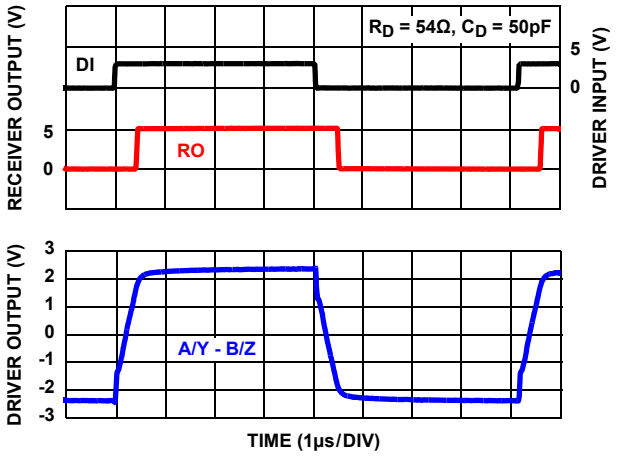


FIGURE 30. V_{CC} = 5V, DRIVER AND RECEIVER WAVEFORMS (ISL32450E, ISL32452E, ISL32457E)

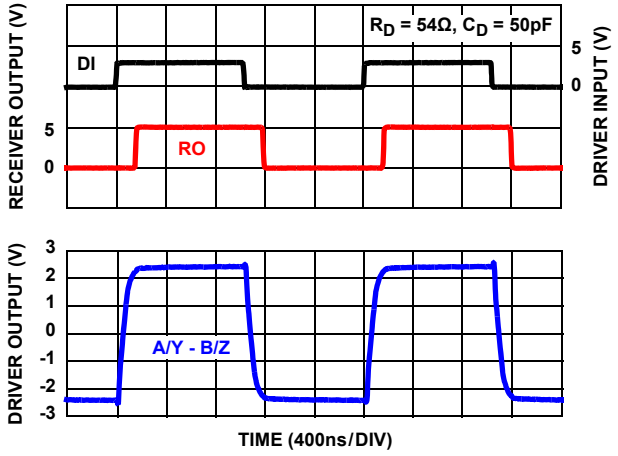


FIGURE 31. V_{CC} = 5V, DRIVER AND RECEIVER WAVEFORMS (ISL32453E, ISL32455E)

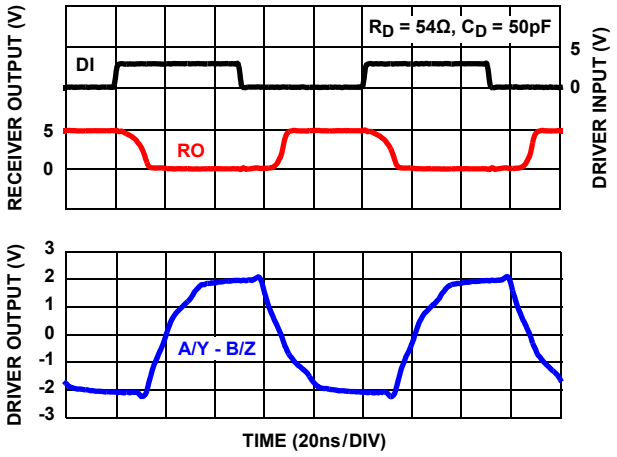


FIGURE 32. V_{CC} = 5V, DRIVER AND RECEIVER WAVEFORMS (ISL32458E, ISL32459E)

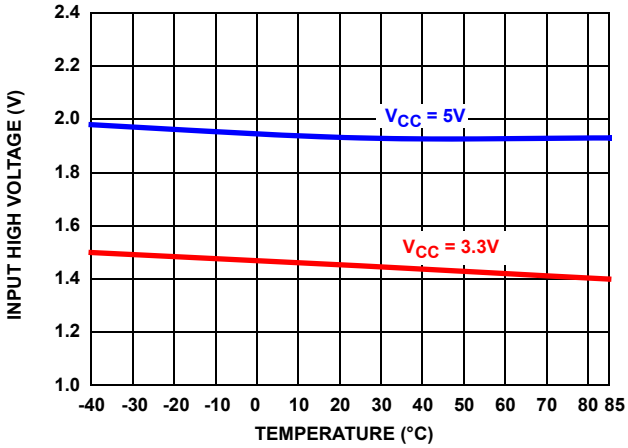


FIGURE 33. LOGIC INPUT HIGH VOLTAGE vs TEMPERATURE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

PROCESS:

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
December 1, 2015	FN7921.1	Added 20Mbps versions (ISL32458E and ISL32459E) to datasheet. Replaced Products section with About Intersil verbiage. Updated Package Outline Drawing M10.118 to the latest version. Changes are as follows: -Updated to new POD template. Added land pattern.
February 20, 2012	FN7921.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

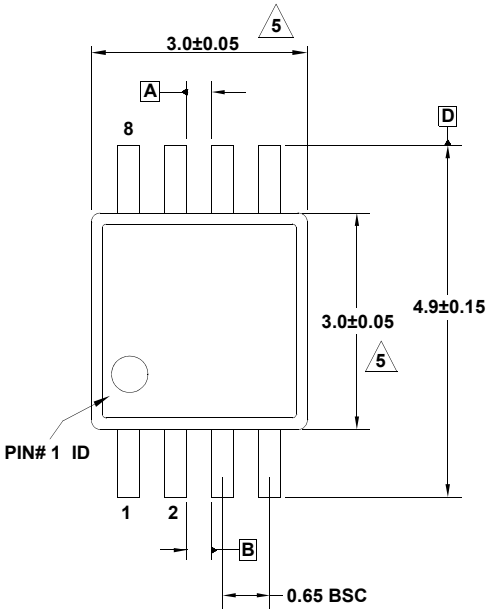
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

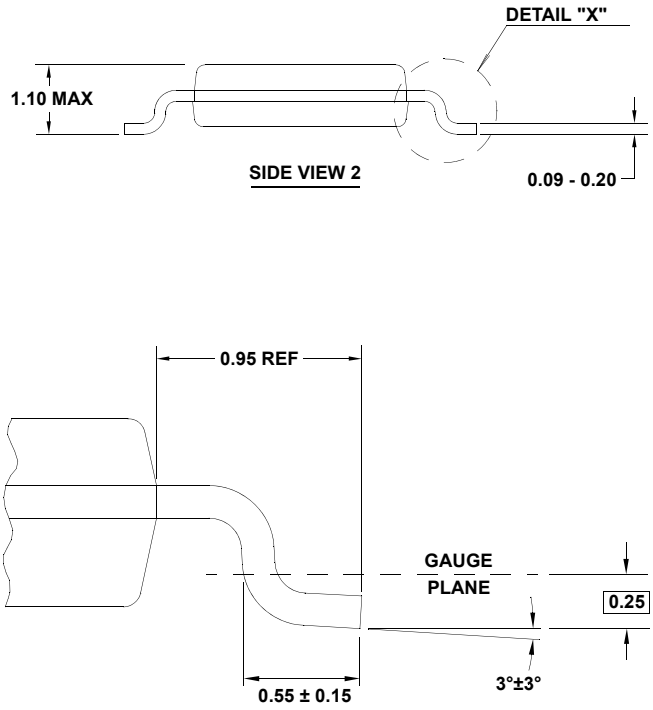
M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

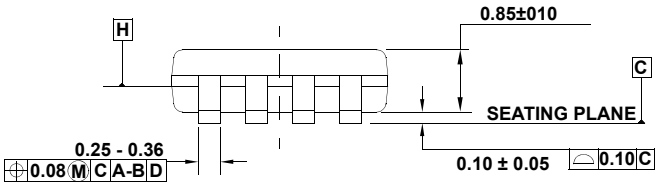
Rev 4, 7/11



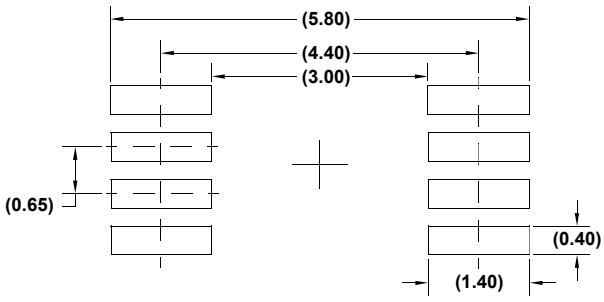
TOP VIEW



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

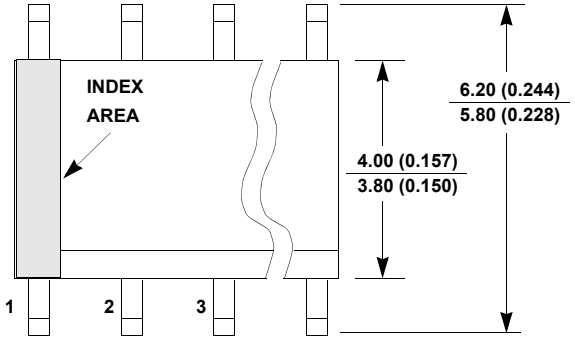
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

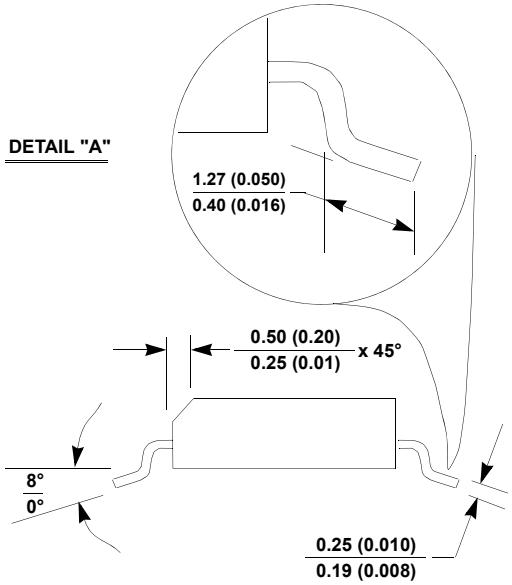
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

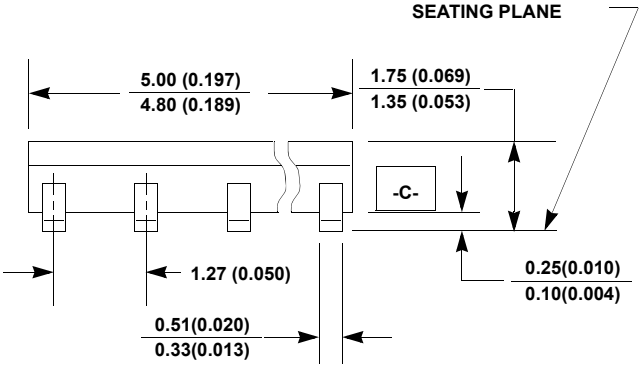
Rev 4, 1/12



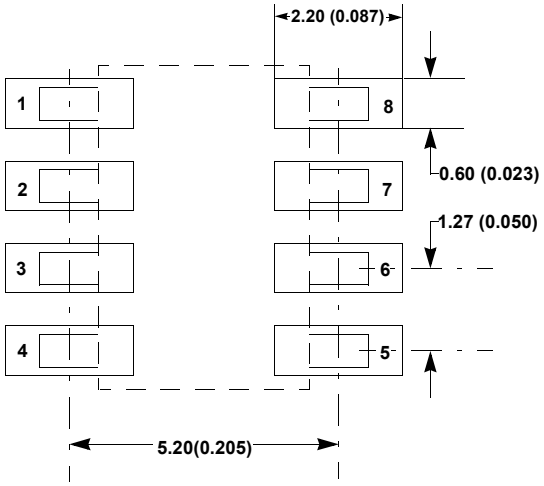
TOP VIEW



SIDE VIEW “B”



SIDE VIEW “A



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

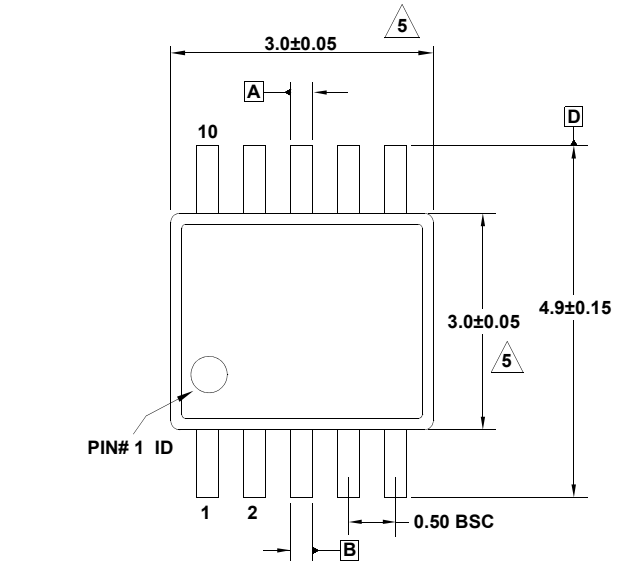
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

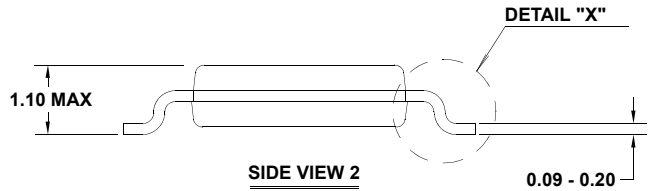
M10.118

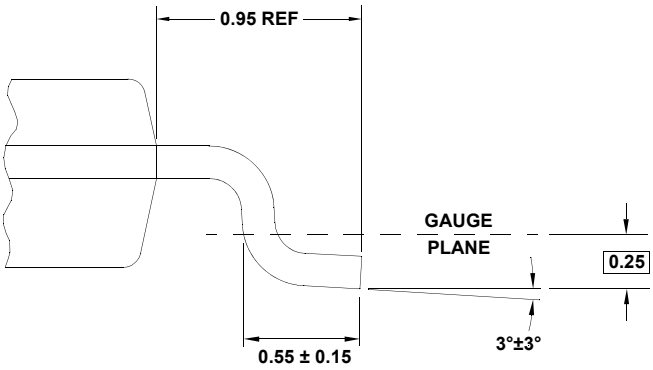
10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 4/12

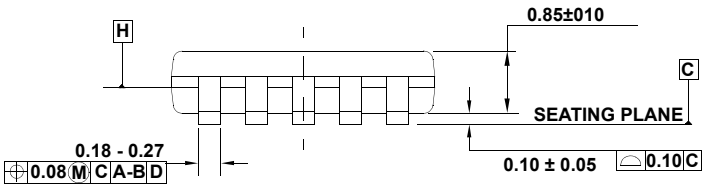


TOP VIEW

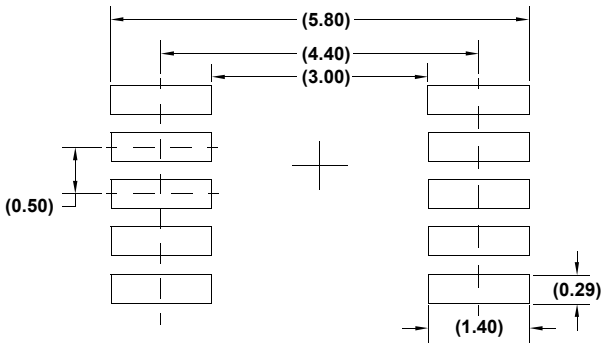




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

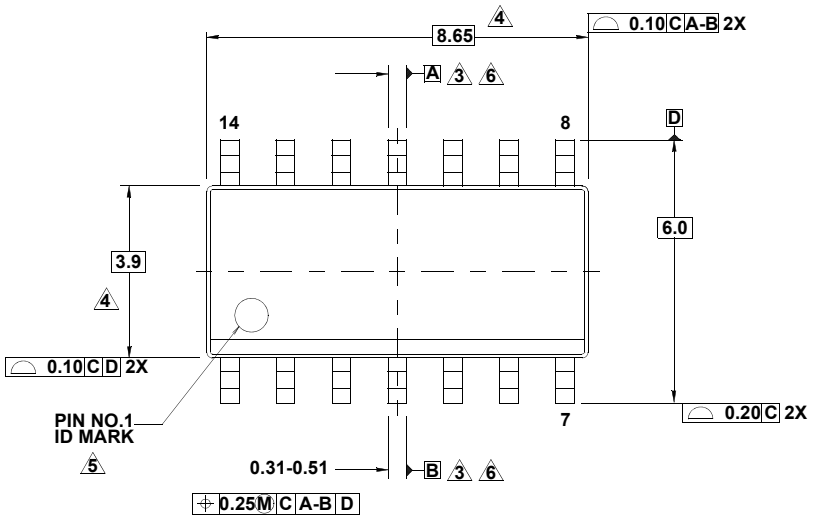
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

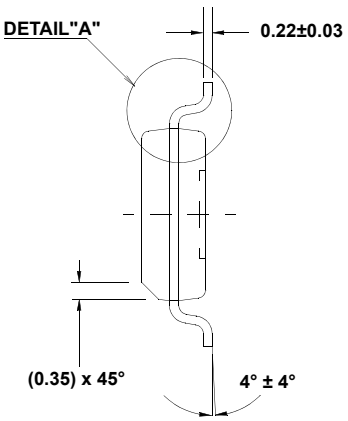
M14.15

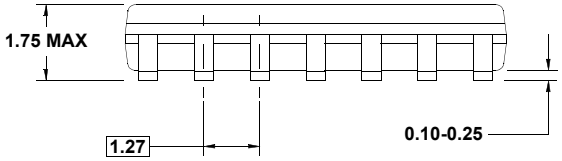
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 10/09

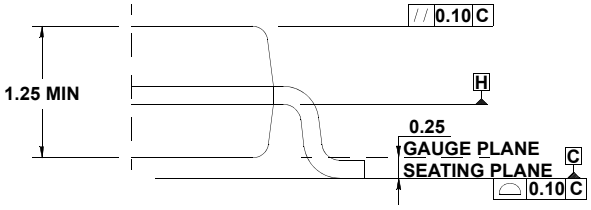


TOP VIEW

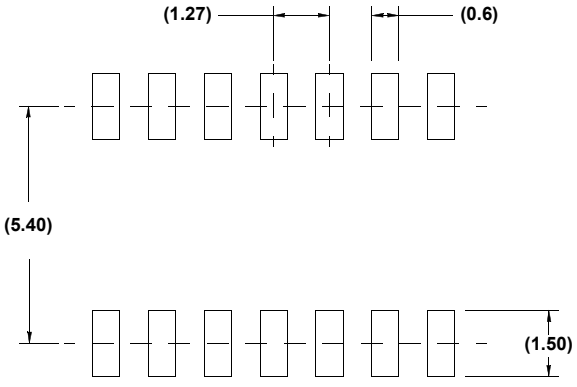




SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 indentifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

Mouser Electronics

Authorized Distributor

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Intersil:

ISL32450EIBZ-T7A ISL32450EIUZ-T7A ISL32452EIBZ-T7A ISL32452EIUZ-T7A ISL32453EIBZ-T7A ISL32453EIUZ-T7A ISL32455EIBZ-T7A ISL32455EIUZ-T7A ISL32457EIBZ-T7A ISL32457EIUZ-T7A ISL32450EIUZ-T ISL32452EIBZ-T ISL32452EIUZ-T ISL32453EIUZ-T ISL32455EIBZ-T ISL32455EIUZ-T ISL32457EIBZ-T ISL32457EIUZ-T ISL32450EIBZ-T ISL32453EIBZ-T ISL32450EIUZ ISL32452EIUZ ISL32453EIUZ ISL32455EIUZ ISL32457EIUZ ISL32450EIBZ ISL32453EIBZ ISL32452EIBZ ISL32455EIBZ ISL32457EIBZ ISL32458EIBZ ISL32458EIBZ-T ISL32458EIBZ-T7A ISL32459EIBZ ISL32459EIBZ-T ISL32459EIBZ-T7A