

3Q Hi-Com Triac 28 April 2015

Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT404 (D2PAK) surface mountable plastic package intended for use in circuits where high static and dynamic dV/ dt and high dl/dt can occur. This "series CT" triac will commutate the full RMS current at maximum rated junction temperature ($T_j = 150$ °C) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High junction operating temperature capability
- High voltage capability
- Less sensitive gate for high noise immunity
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- Applications subject to high temperature
- Electronic thermostats (heating and cooling)
- High power motor controls e.g. washing machines and vacuum cleaners
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids

4. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{DRM}	repetitive peak off- state voltage		-	-	600	V
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C};$ t _p = 20 ms; <u>Fig. 4; Fig. 5</u>	-	-	100	A
Tj	junction temperature		-	-	150	°C
I _{T(RMS)}	RMS on-state current	full sine wave; T _{mb} ≤ 125 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	-	12	A





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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	$V_D = 12 V; I_T = 0.1 A; T2+G+;$ T _j = 25 °C; <u>Fig. 7</u>	2	-	35	mA
		$V_D = 12 \text{ V}; \text{ I}_T = 0.1 \text{ A}; \text{ T2+ G-};$ T _j = 25 °C; <u>Fig. 7</u>	2	-	35	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	2	-	35	mA

5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	mb	T2-T1
2	T2	main terminal 2		sym051
3	G	gate		
mb	T2	mounting base; main terminal 2		
			D2PAK (SOT404)	

6. Ordering information

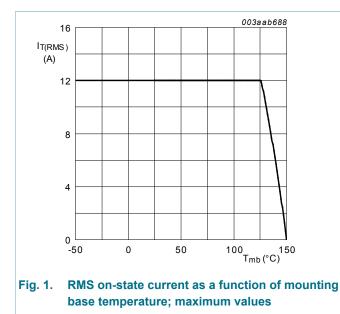
Table 3. Ordering inf	formation		
Type number	Package		
	Name	Description	Version
BTA312B-600CT	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

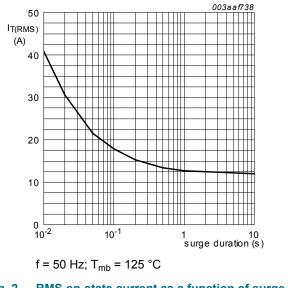
7. Limiting values

Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

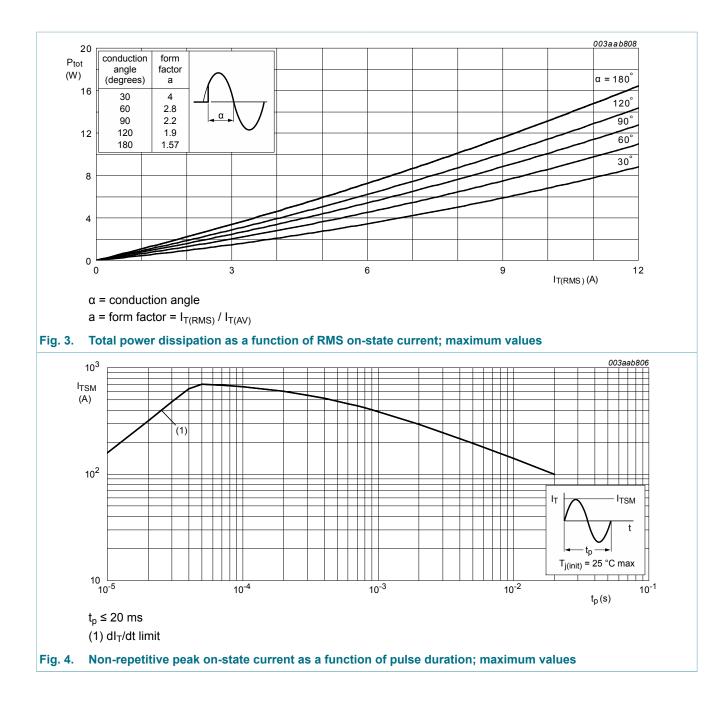
Symbol	Parameter	Conditions	Min	Мах	Unit
V _{DRM}	repetitive peak off-state voltage		-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{mb} ≤ 125 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	12	A
I _{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25 \text{ °C};$ $t_p = 20 \text{ ms}; \text{Fig. 4}; \text{Fig. 5}$	-	100	A
		full sine wave; $T_{j(init)} = 25 \text{ °C};$ $t_p = 16.7 \text{ ms}$	-	110	A
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	50	A ² s
dI _T /dt	rate of rise of on-state current	I _G = 70 mA	-	100	A/µs
I _{GM}	peak gate current		-	2	А
P _{GM}	peak gate power		-	5	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	150	°C





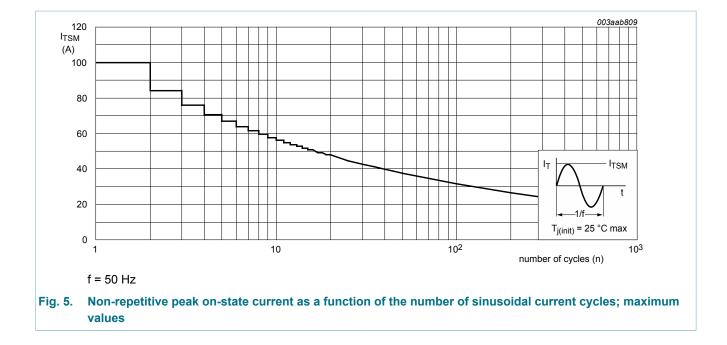


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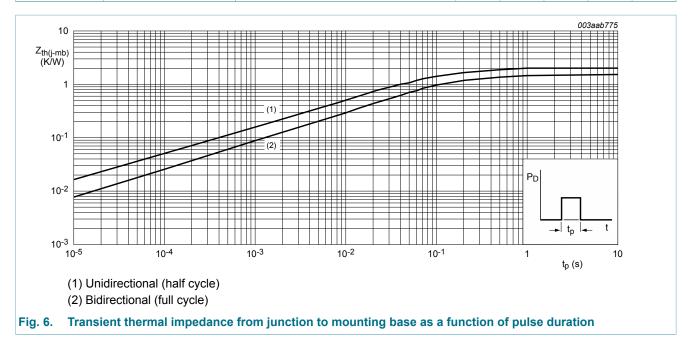
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8. Thermal characteristics

Table 5. The	rmal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance	full cycle; <u>Fig. 6</u>	-	-	1.5	K/W
	from junction to mounting base	half cycle; <u>Fig. 6</u>	-	-	2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	printed circuit board mounted; minimum footprint	-	55	-	K/W



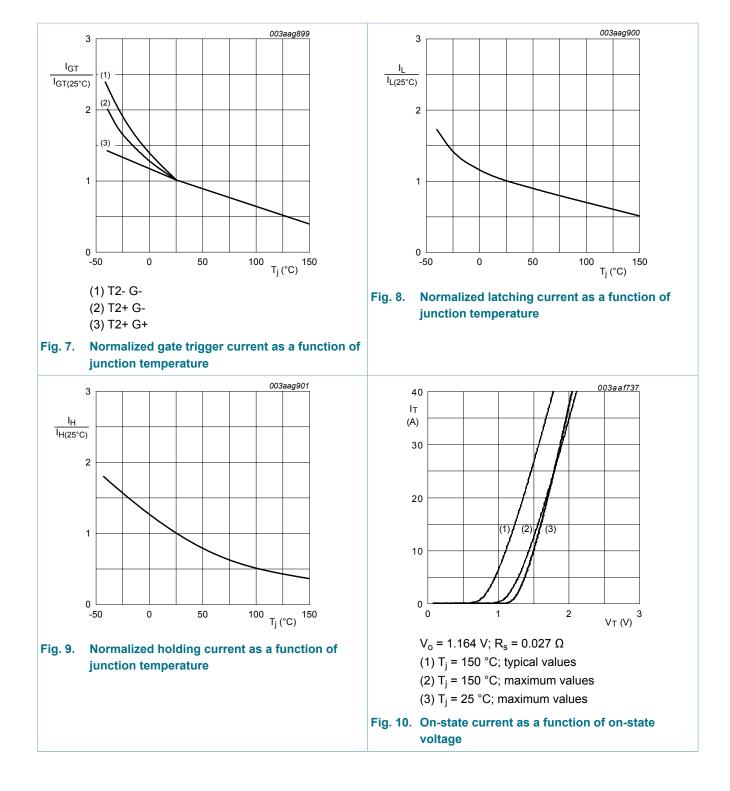
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9. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	V_D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 7</u>	2	-	35	mA
		V_D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 7</u>	2	-	35	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	2	-	35	mA
IL	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 8</u>	-	-	50	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	60	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	50	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	35	mA
V _T	on-state voltage	I _T = 15 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.6	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	0.8	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 150 °C; Fig. 11	0.25	0.4	-	V
I _D	off-state current	V _D = 600 V; T _j = 150 °C	-	0.4	2	mA
Dynamic ch	naracteristics	· · · ·	- I			
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	300	-	-	V/µs
dI _{com} /dt	rate of change of commutating current	$\label{eq:VD} \begin{split} V_D &= 400 \text{ V}; \text{T}_{\text{j}} = 150 ^\circ\text{C}; \text{I}_{\text{T}(\text{RMS})} = 12 \text{ A}; \\ \text{d} V_{\text{com}}/\text{d} \text{t} &= 20 \text{V}/\text{\mu}\text{s}; \text{ (snubberless condition); gate open circuit} \end{split}$	8	-	-	A/ms
		V_D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 10 V/µs; gate open circuit	13	-	-	A/ms
		V_D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 1 V/µs; gate open circuit	20	-	-	A/ms

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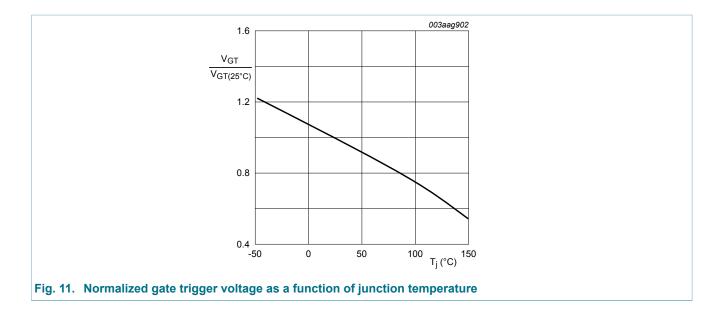


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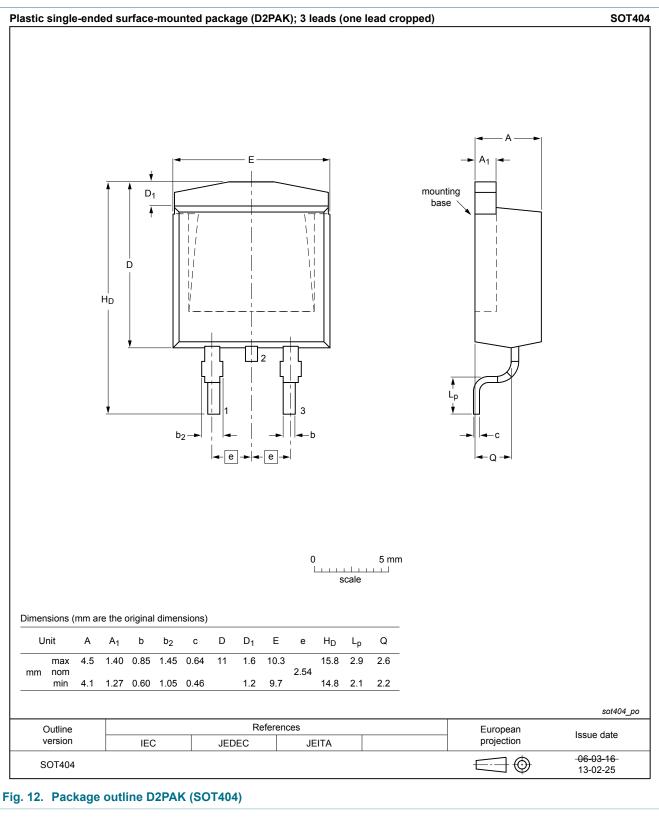
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10. Package outline



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11. Legal information

11.1 Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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