



# PMZ350UPE

20 V, P-channel Trench MOSFET

14 May 2014

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006-3 (SOT883) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Very fast switching
- ElectroStatic Discharge (ESD) protection > 1.8 kV HBM
- Leadless ultra small SMD plastic package: 1.0 × 0.6 × 0.48 mm

## 3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_J = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-1.4	A
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -0.3\text{ A}; T_J = 25\text{ °C}$	-	330	450	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

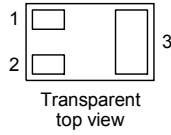
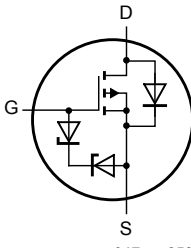


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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1006-3 (SOT883)</p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZ350UPE	DFN1006-3	DFN1006-3: leadless ultra small plastic package; 3 solder lands	SOT883

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMZ350UPE	ZP

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	-20	V
$V_{GS}$	gate-source voltage			-8	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-1.4	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-1	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-0.7	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-2.8	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	360	mW
			[1]	-	715	mW
		$T_{sp} = 25\text{ °C}$		-	3125	mW
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-0.8	A
<b>ESD maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	1800	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $1\text{ cm}^2$ .

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



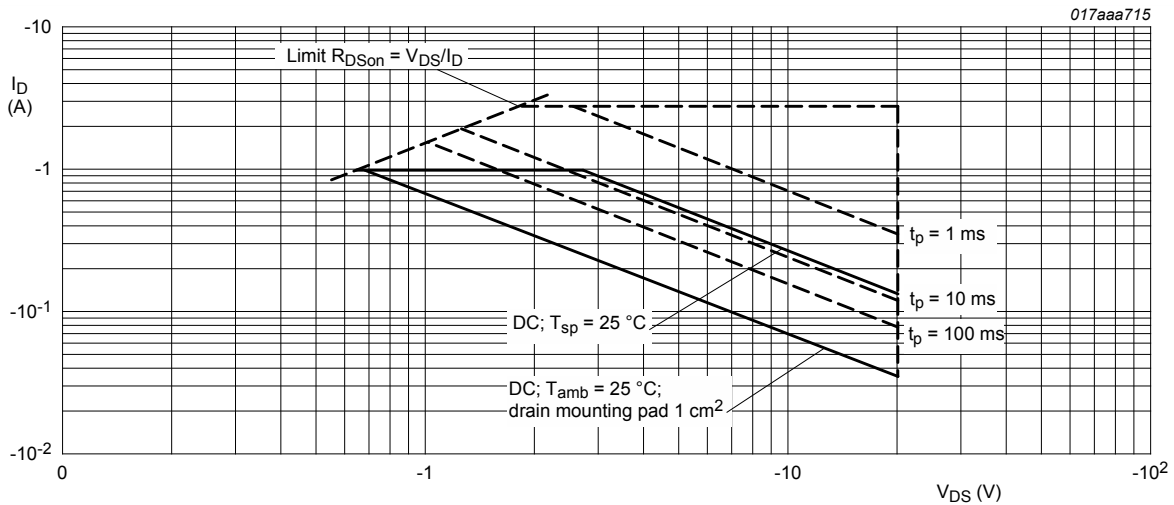
Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$



Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$



$I_{DM}$  = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	304	350	K/W
			[2]	-	150	175	K/W
			[3]	-	90	103	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	35	40	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>, t ≤ 5 s.

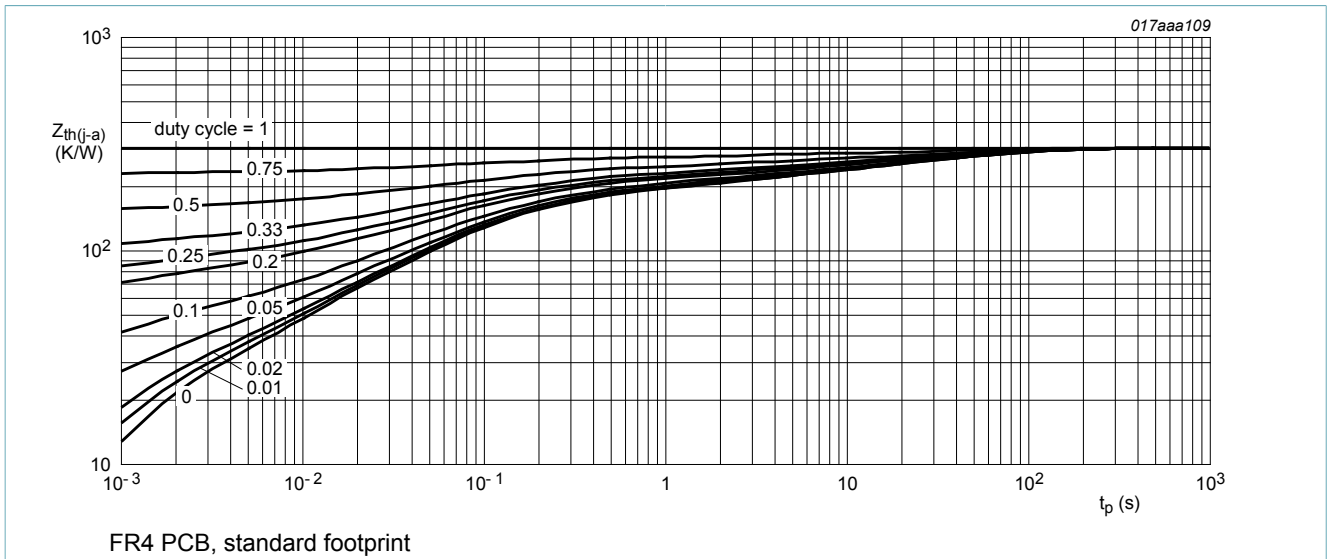


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

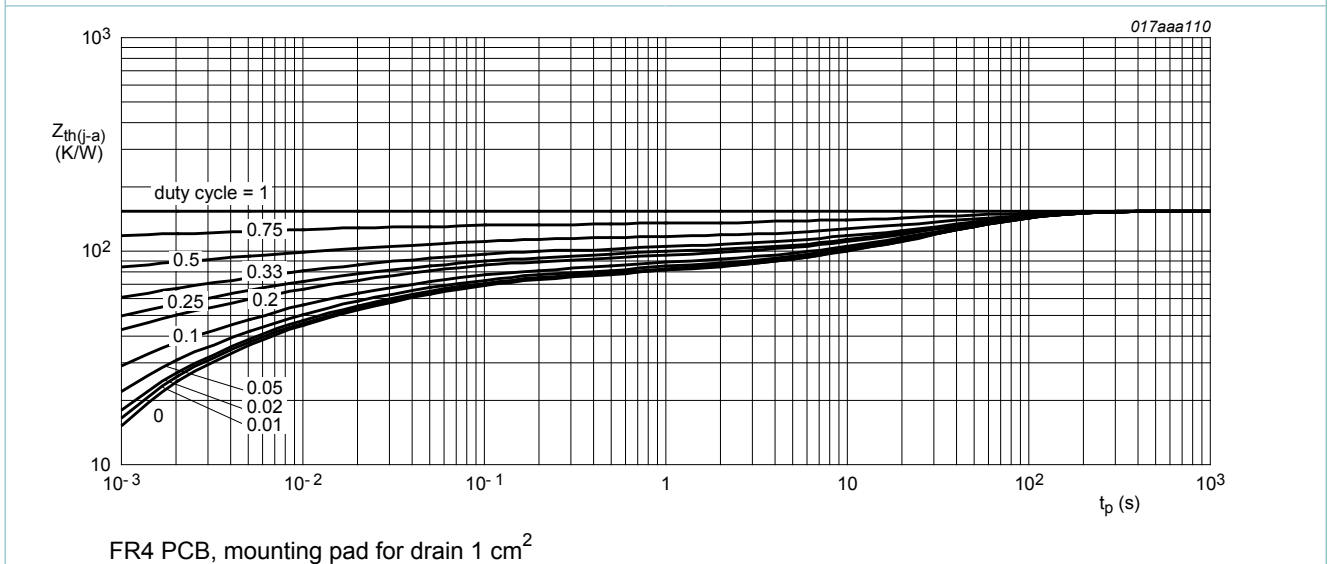


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.45	-0.7	-0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
		$V_{GS} = 8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -0.3 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	330	450	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -0.3 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	478	645	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -0.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	420	645	m $\Omega$
		$V_{GS} = -1.8 \text{ V}$ ; $I_D = -0.1 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	520	940	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -0.3 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	1.4	-	S
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$ ; $I_D = -0.3 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	1.3	1.9	nC
$Q_{GS}$	gate-source charge		-	0.2	-	nC
$Q_{GD}$	gate-drain charge		-	0.25	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	127	-	pF
$C_{oss}$	output capacitance		-	34	-	pF
$C_{rss}$	reverse transfer capacitance		-	25	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = -10 \text{ V}$ ; $I_D = -0.3 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 6 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	4	-
$t_r$	rise time		-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	26	-	ns
$t_f$	fall time		-	9	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -0.1 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.7	-1.2	V

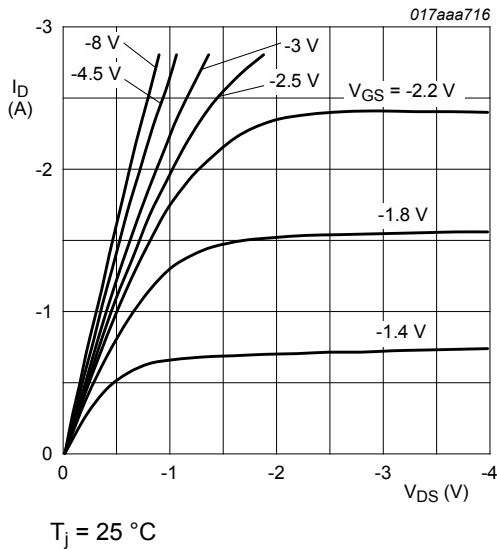


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

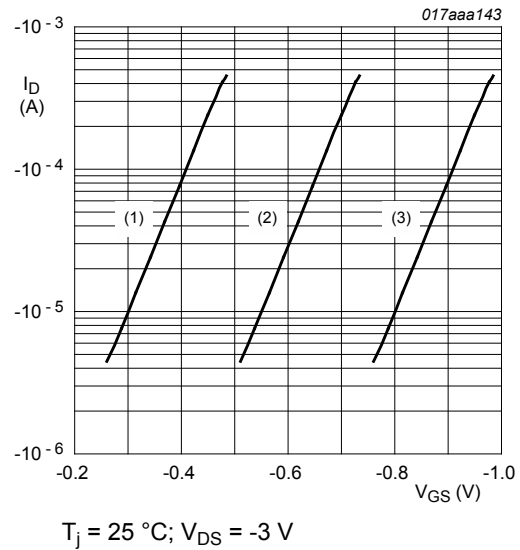


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

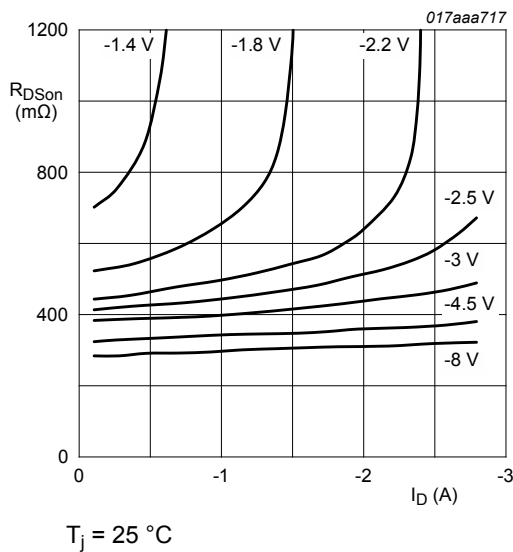


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

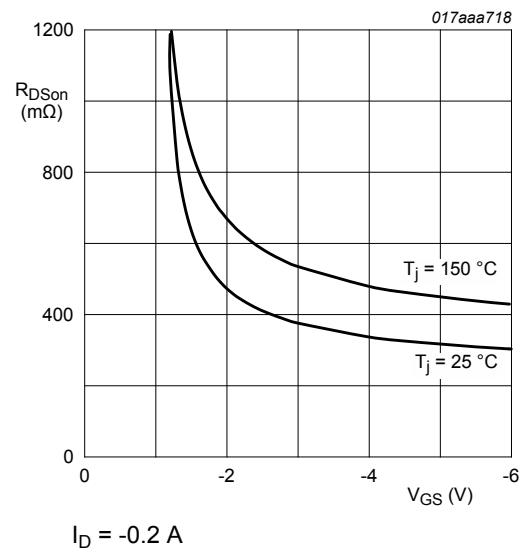
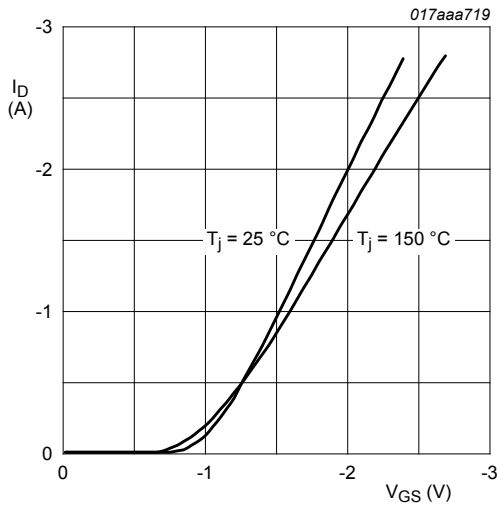


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

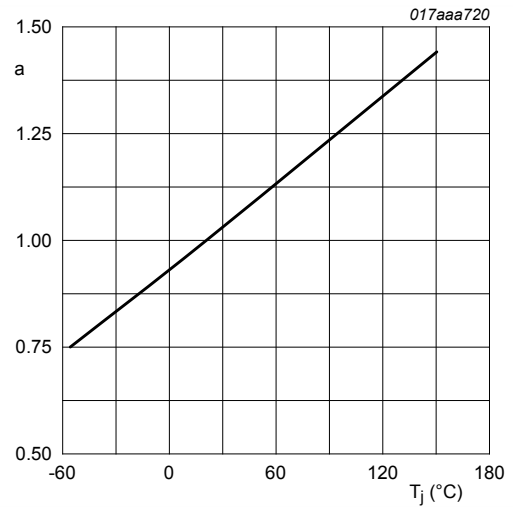
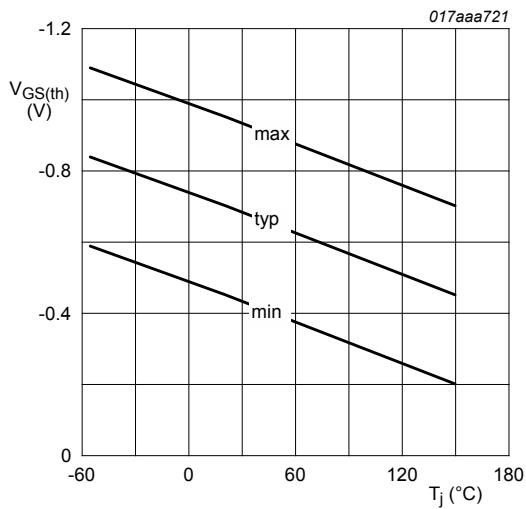


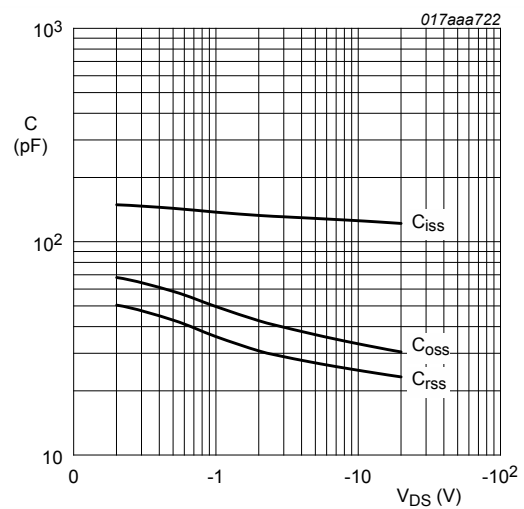
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

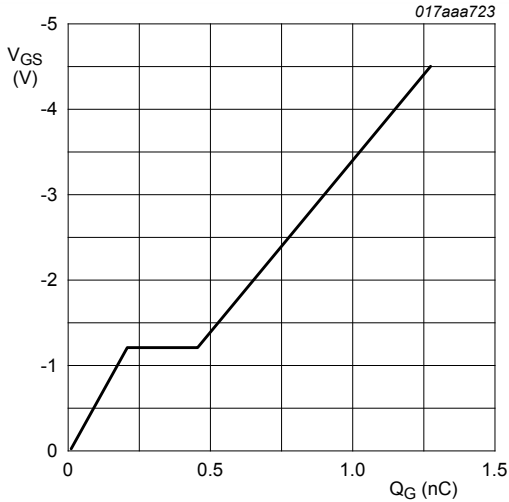
Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$I_D = -0.3$  A;  $V_{DS} = -10$  V;  $T_{amb} = 25$  °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

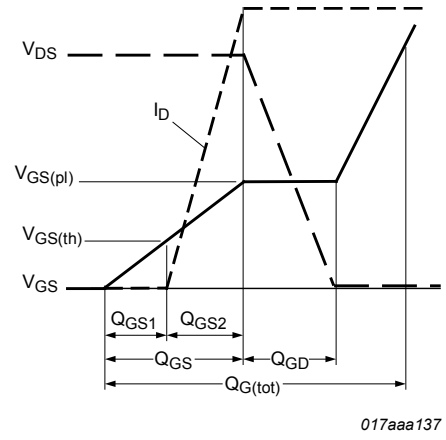
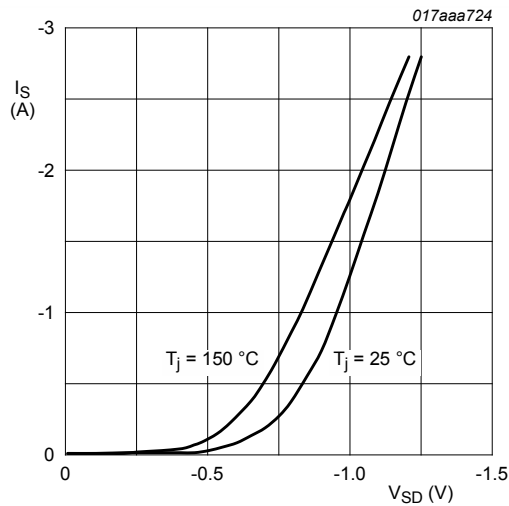


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$  V

Fig. 16. Source current as a function of source-drain voltage; typical values

### 11. Test information



Fig. 17. Duty cycle definition

### 12. Package outline

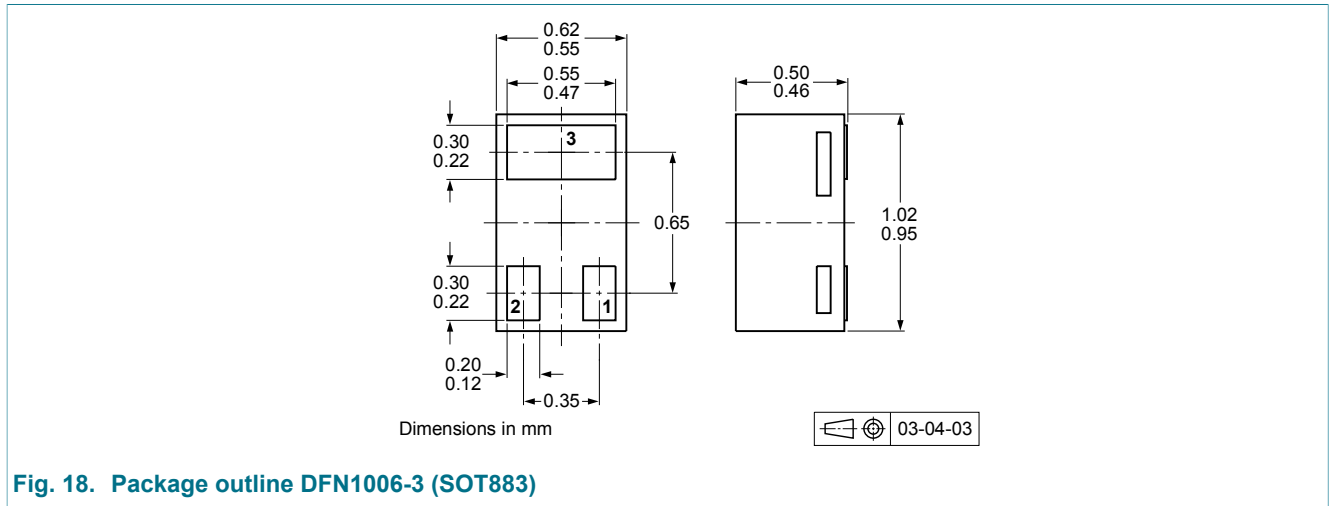


Fig. 18. Package outline DFN1006-3 (SOT883)

### 13. Soldering

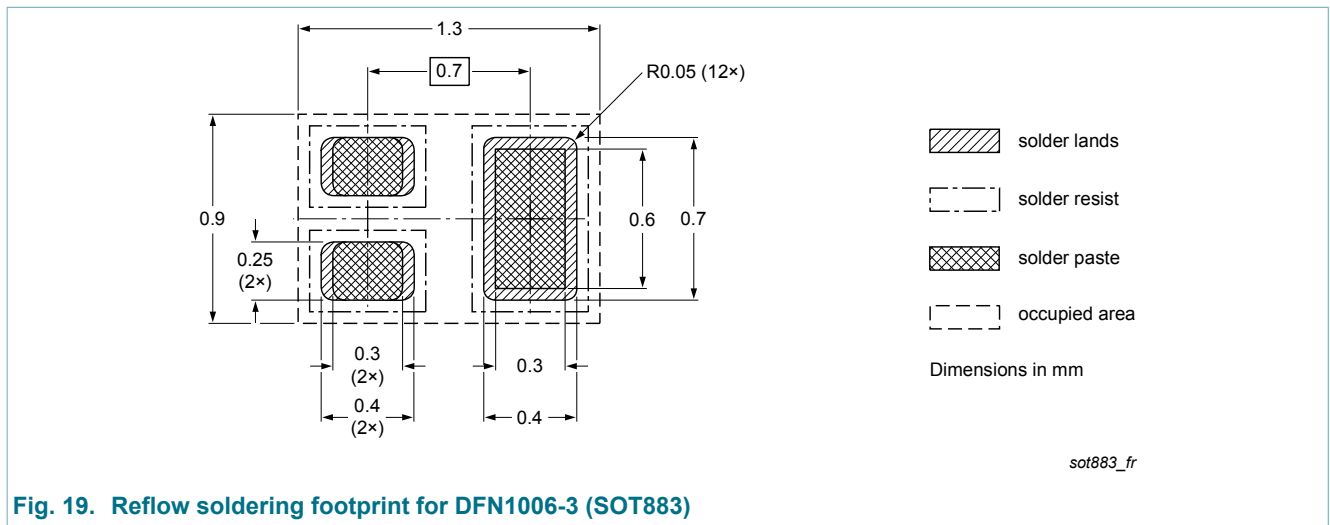


Fig. 19. Reflow soldering footprint for DFN1006-3 (SOT883)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZ350UPE v.1	20140514	Product data sheet	-	-

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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