NCS333, NCV333, NCS2333, NCV2333, NCS4333, NCV4333

10 μV Offset, 0.07 μV/°C, Low Power, Zero-Drift Operational Amplifier

The NCS333 family of high precision op amps feature very low input offset voltage and near−zero drift over time and temperature. These low quiescent current amplifiers have high impedance inputs with a common−mode range 100 mV beyond the rails as well as rail−to−rail output swing within 50 mV of the rails. These op amps operate over a wide supply range from 1.8 V to 5.5 V. The NCS333 family exhibits outstanding CMRR without the crossover associated with traditional complementary input stages. The NCS333, as well as the dual version, NCS2333, and the quad version, NCS4333, come in a variety of packages and pinouts. Automotive qualified options are available under NCV prefix.

Features

- Low Offset Voltage: 10 μV max for NCS333, 30 μV max for NCS2333 and NCS4333
- Zero Drift: 0.07 μV/°C max
- Low Noise: 1.1 μVpp, 0.1 Hz to 10 Hz
- Quiescent Current per Channel: 17 μA Typical at 3.3 V Supply
- Supply Voltage: 1.8 V to 5.5 V
- Rail−to−Rail Input and Output
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Temperature Measurements
- Transducer Applications
- Current Sensing

End Products

- Battery Powered Instruments
- Electronic Scales
- Medical Instrumentation

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

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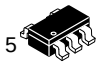
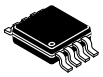


SOT23−5
SN SUFFIX
CASE 483

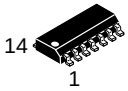
SC70−5
SQ SUFFIX
CASE 419A

DFN−8
MN SUFFIX
CASE 506BW



MSOP−8
DM SUFFIX
CASE 846A−02

SOIC−8
D SUFFIX
CASE 751



SOIC−14
D SUFFIX
CASE 751A

DEVICE MARKING INFORMATION

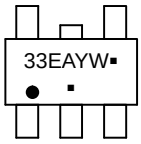
See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

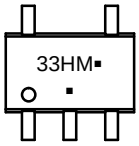
See detailed ordering and shipping information on page 3 of this data sheet.

DEVICE MARKING INFORMATION

Single Channel Configuration
NCS333, NCV333

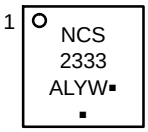


TSOP−5/SOT23−5
CASE 483

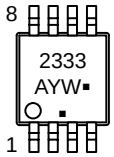


SC70−5
CASE 419A

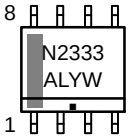
Dual Channel Configuration
NCS2333, NCV2333



DFN8, 3x3, 0.65P
CASE 506BW

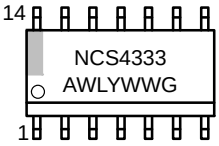


Micro8/MSOP8
CASE 846A−02



SOIC−8
CASE 751

Quad Channel Configuration
NCS4333, NCV4333



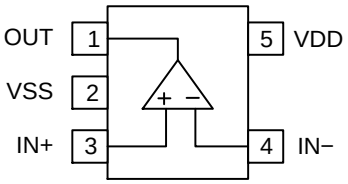
SOIC−14
CASE 751A

33E	= Specific Device Code (SOT23−5)
33H	= Specific Device Code (SC70−5)
A	= Assembly Location
Y	= Year
W	= Work Week
M	= Date Code
G or ▪	= Pb−Free Package

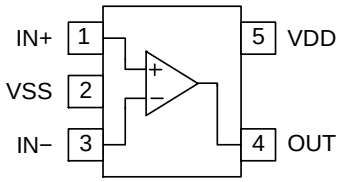
(Note: Microdot may be in either location)

PIN CONNECTIONS

Single Channel Configuration
NCS333, NCV333

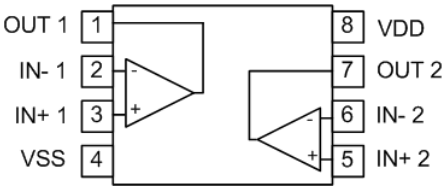


SOT23−5 / TSOP−5

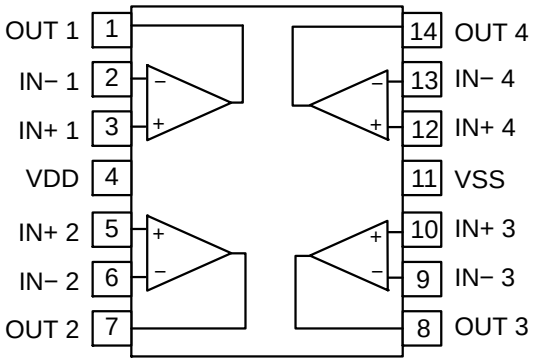


SC70−5 / SC−88−5 / SOT−353−5

Dual Channel Configuration
NCS2333, NCV2333



Quad Channel Configuration
NCS4333, NCV4333



ORDERING INFORMATION

Configuration	Automotive	Device	Package	Shipping †
Single	No	NCS333SN2T1G	SOT23−5 / TSOP−5	3000 / Tape & Reel
		NCS333ASN2T1G* (In Development)		3000 / Tape & Reel
		NCS333SQ3T2G	SC70−5 / SC−88−5 / SOT−353−5	3000 / Tape & Reel
		NCS333ASQ3T2G* (In Development)		3000 / Tape & Reel
	Yes	NCV333SN2T1G* (In Development)	SOT23−5 / TSOP−5	3000 / Tape & Reel
Dual	No	NCS2333MNTXG* (In Development)	DFN8	3000 / Tape & Reel
		NCS2333DR2G	SOIC−8	2500 / Tape & Reel
		NCS2333DMR2G	MICRO−8	4000 / Tape & Reel
	Yes	NCV2333DR2G	SOIC−8	2500 / Tape & Reel
		NCV2333DMR2G* (In Development)	MICRO−8	4000 / Tape & Reel
Quad	No	NCS4333DR2G* (In Development)	SOIC−14	2500 / Tape & Reel
	Yes	NCV4333DR2G* (In Development)	SOIC−14	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Contact local sales office for more information

ABSOLUTE MAXIMUM RATINGS

Over operating free−air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage	7	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	(VSS) − 0.3 to (VDD) + 0.3	V
Input Current (Note 1)	±10	mA
Output Short Circuit Current (Note 2)	Continuous	
TEMPERATURE		
Operating Temperature	−40 to +125	°C
Storage Temperature	−65 to +150	°C
Junction Temperature	−65 to +150	°C
ESD RATINGS (Note 3)		
Human Body Model (HBM)	4000	V
Machine Model (MM)	200	V
Charged Device Model (CDM)	2000	V
OTHER RATINGS		
Latch−up Current (Note 4)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Input terminals are diode−clamped to the power−supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
2. Short−circuit to ground.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)
4. Latch−up Current tested per JEDEC standard: JESD78.

THERMAL INFORMATION (Note 5)

Parameter	Symbol	Package	Value	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	SOT23−5/ TSOP5	290	°C/W
		SC70−5 / SC−88−5 / SOT−353−5	425	
		Micro8/MSOP8	298	
		SOIC−8	250	
		DFN−8	130	
		SOIC−14	216	

5. As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm^2 and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Range	Unit
Supply Voltage (V_{DD} − V_{SS})		V_S	1.8 to 5.5	V
Specified Operating Range	NCS333	T_A	−40 to 105	°C
	NCS333A, NCV333, NCx2333, NCx4333		−40 to 125	
Input Common Mode Voltage Range		V_{ICMR}	V_{SS}−0.1 to V_{DD}+0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	V_S = +5 V	NCS333		3.5	10	μV
			NCx2333, NCx4333		6.0	30	
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta T$	NCS333			**0.03**	**0.07**	μV/°C
		NCx2333, NCx4333, V_S = 5 V			**0.04**	**0.07**	
Offset Voltage Drift vs Supply	$\Delta V_{OS}/\Delta V_S$	NCS333	Full temperature range		**0.32**	**5**	μV/V
		NCx2333, NCx4333	T_A = +25°C		0.32	5	
			Full temperature range			**12.6**	
Input Bias Current	I_{IB}	T_A = +25°C	NCS333		±60	±200	pA
			NCx2333, NCx4333		±60	±400	
		Full temperature range			**±400**		
Input Offset Current	I_{OS}	T_A = +25°C	NCS333		±50	±400	pA
			NCx2333, NCx4333		±50	±800	
Common Mode Rejection Ratio	CMRR	V_{SS} − 0.1 < V_{CM} < V_{DD} + 0.1	V_S = 1.8 V		111		dB
			V_S = 3.3 V		118		
			V_S = 5.0 V	106	123		
			V_S = 5.5 V		127		
Input Resistance	R_{IN}	Differential			180		GΩ
		Common Mode			90		
Input Capacitance	C_{IN}	NCS333	Differential		2.3		pF
			Common Mode		4.6		
		NCx2333, NCx4333	Differential		4.1		
			Common Mode		7.9		
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	A_{VOL}	V_{SS} + 100 mV < V_O < V_{DD} − 100 mV		**106**	145		dB
Open Loop Output Impedance	Z_{out-OL}	f = UGBW, I_O = 0 mA			300		Ω
Output Voltage High, Referenced to V_{DD}	V_{OH}	T_A = +25°C			10	50	mV
		Full temperature range				**70**	
Output Voltage Low, Referenced to V_{SS}	V_{OL}	T_A = +25°C			10	50	mV
		Full temperature range				**70**	
Output Current Capability	I_O	Sinking Current	NCS333		25		mA
			NCx2333, NCx4333		11		
		Sourcing Current			5.0		
Capacitive Load Drive	C_L			See Figure 13			

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
NOISE PERFORMANCE							
Voltage Noise Density	e_N	f_{IN} = 1 kHz			62		nV / $\sqrt{Hz}$
Voltage Noise	e_{P-P}	f_{IN} = 0.1 Hz to 10 Hz			1.1		μV_{PP}
		f_{IN} = 0.01 Hz to 1 Hz			0.5		
Current Noise Density	i_N	f_{IN} = 10 Hz			350		fA / $\sqrt{Hz}$
Channel Separation		NCx2333, NCx4333			135		dB
DYNAMIC PERFORMANCE							
Gain Bandwidth Product	GBWP	C_L = 100 pF	NCS333, NCx4333		350		kHz
			NCx2333		270		
Gain Margin	A_M	C_L = 100 pF			18		dB
Phase Margin	ϕ_M	C_L = 100 pF			55		°
Slew Rate	SR	G = +1			0.15		V/μs
POWER SUPPLY							
Power Supply Rejection Ratio	PSRR	NCS333	Full temperature range	**106**	130		dB
		NCx2333, NCx4333, NCV333	T_A = +25°C	106	130		
			Full temperature range	**98**			
Turn−on Time	t_{ON}	V_S = 5 V			100		μs
Quiescent Current	I_Q	No load, per channel	1.8 V ≤ V_S ≤ 3.3 V		17	25	μA
						27	
			3.3 V < V_S ≤ 5.5 V		21	33	
						35	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

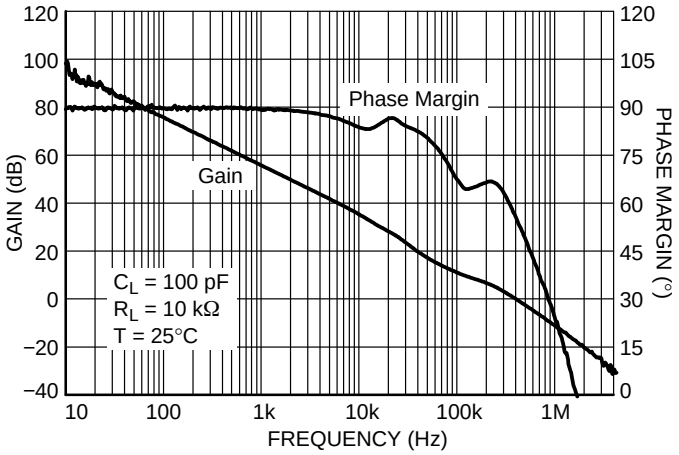


Figure 1. Open Loop Gain and Phase Margin vs. Frequency

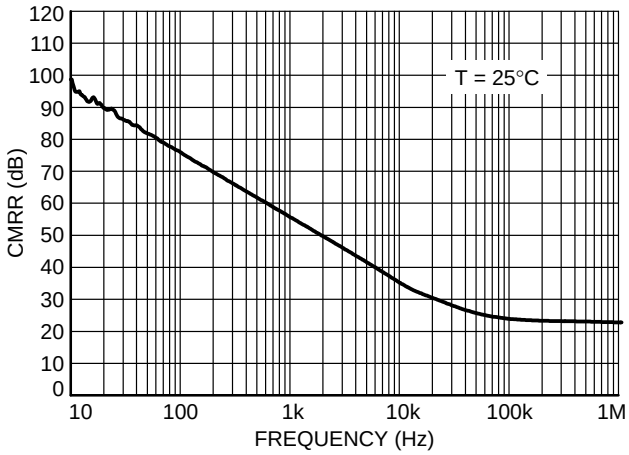


Figure 2. CMRR vs. Frequency

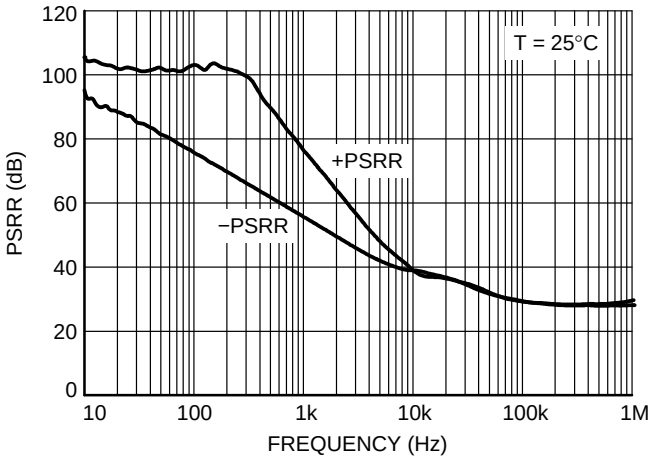


Figure 3. PSRR vs. Frequency

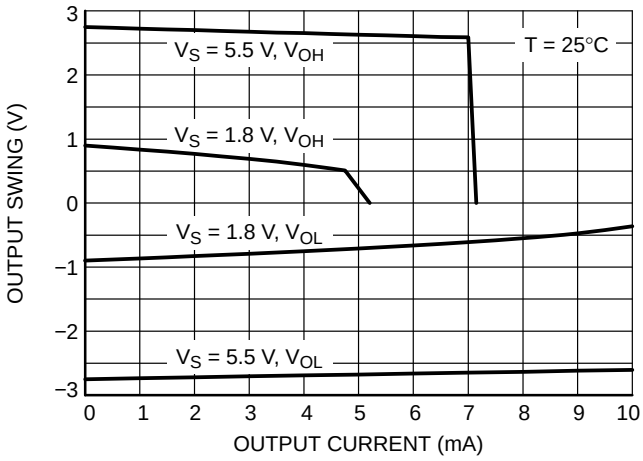


Figure 4. Output Voltage Swing vs. Output Current

TYPICAL CHARACTERISTICS

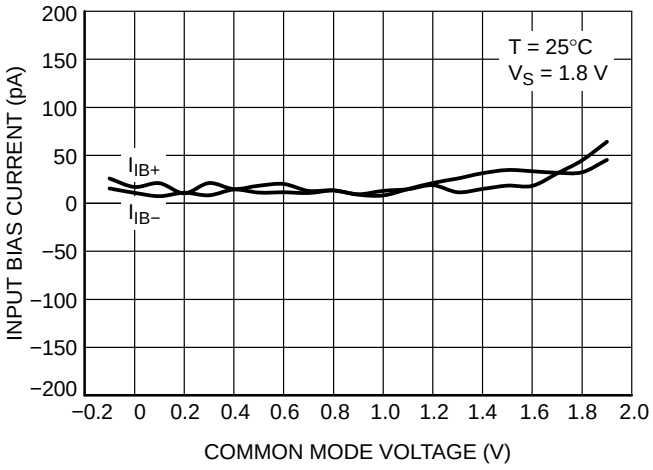


Figure 5. Input Bias Current vs. Common Mode Voltage

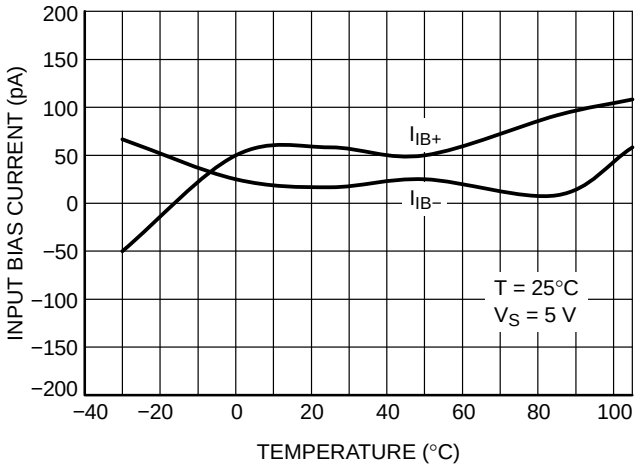


Figure 6. Input Bias Current vs. Temperature

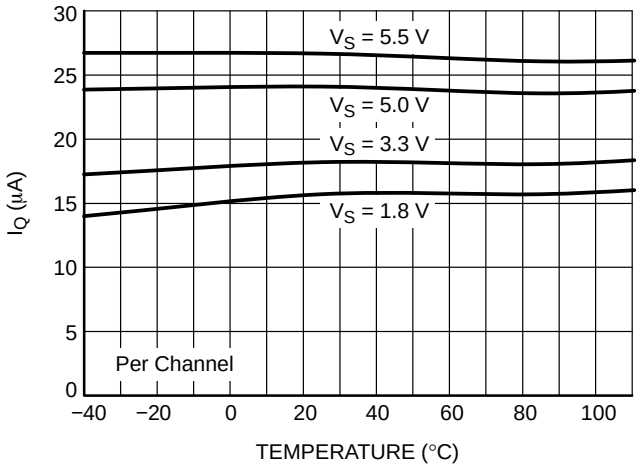


Figure 7. Quiescent Current vs. Temperature

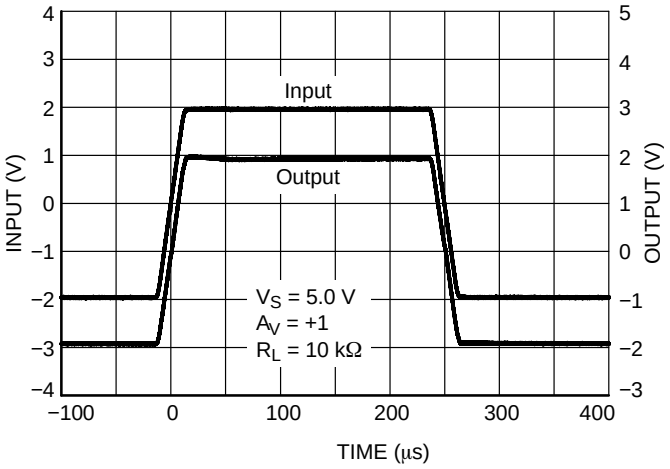


Figure 8. Large Signal Step Response

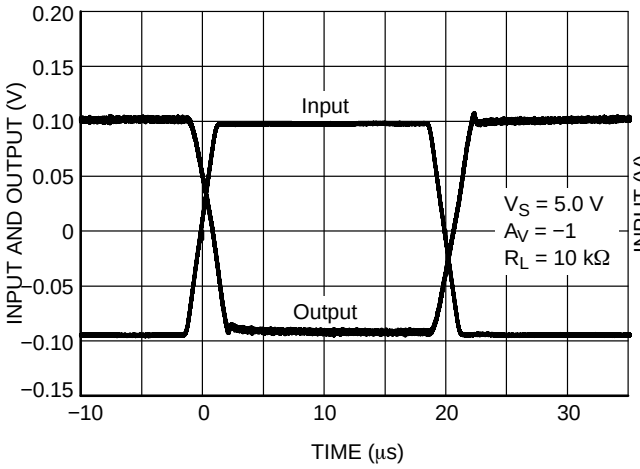


Figure 9. Small Signal Step Response

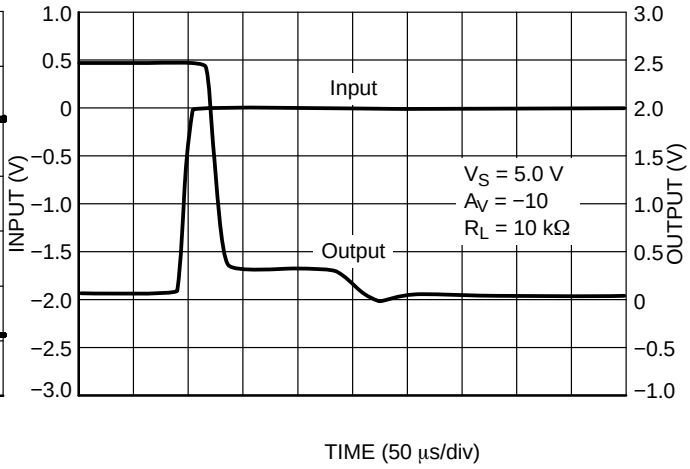


Figure 10. Positive Overvoltage Recovery

TYPICAL CHARACTERISTICS

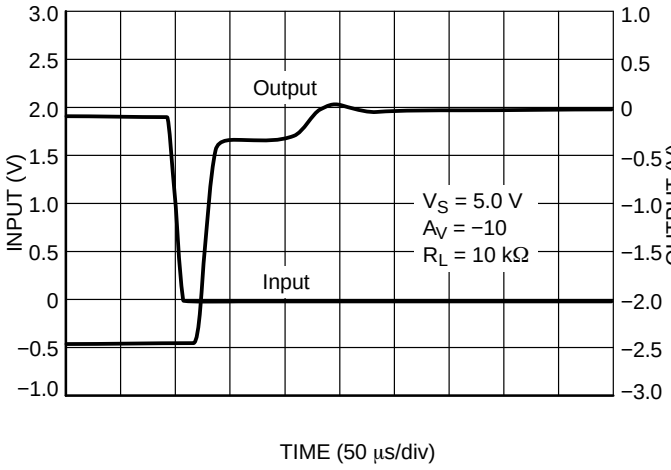


Figure 11. Negative Overvoltage Recovery

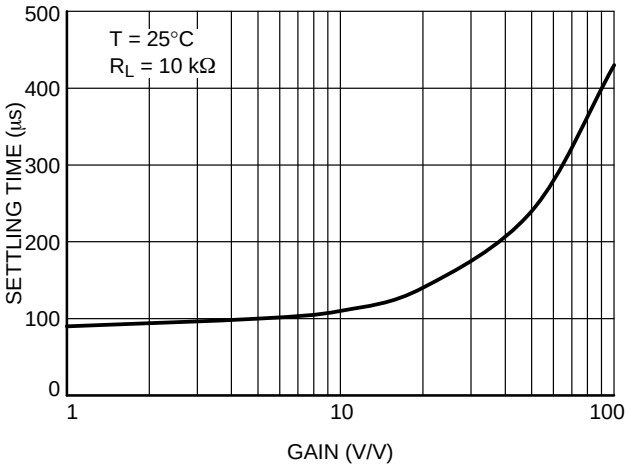


Figure 12. Setting Time to 0.1% vs. Closed−Loop Gain

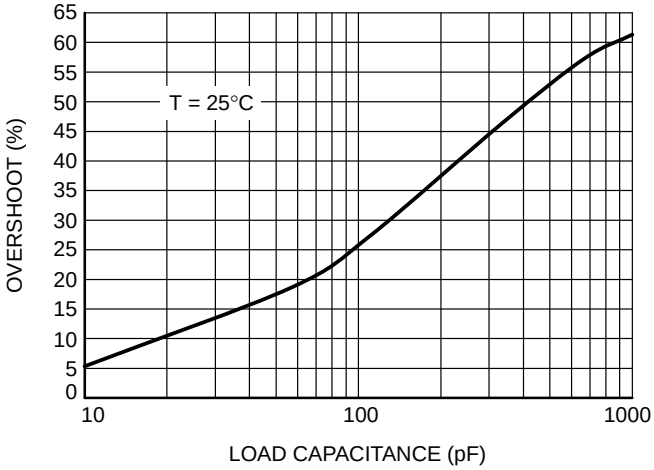


Figure 13. Small−Signal Overshoot vs. Load Capacitance

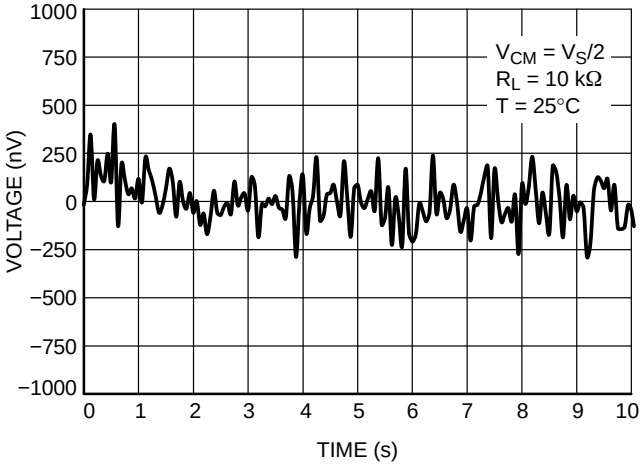


Figure 14. 0.1 Hz to 10 Hz Noise

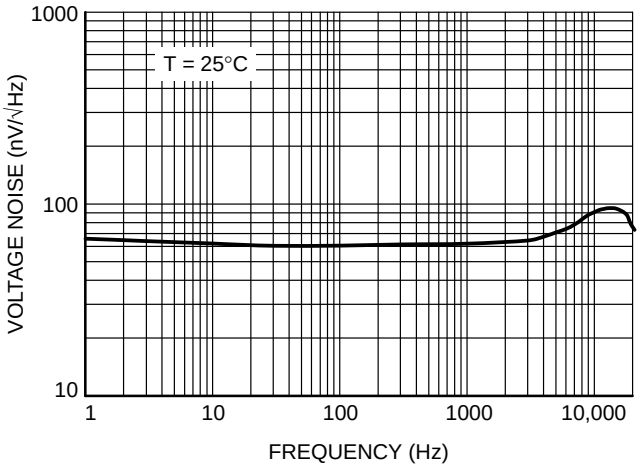


Figure 15. Voltage Noise Density vs. Frequency

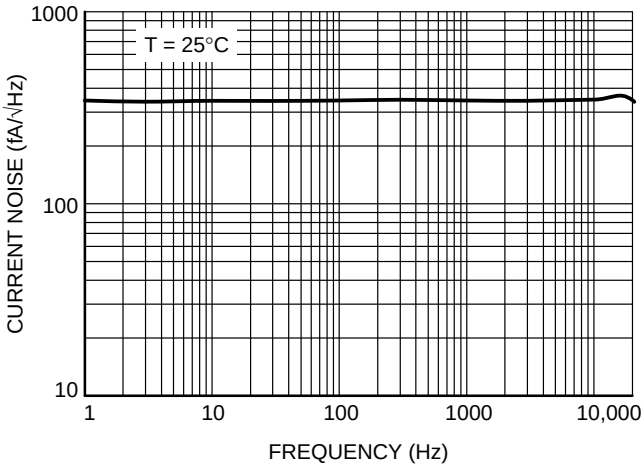


Figure 16. Current Noise Density vs. Frequency

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

Low−Side Current Sensing

The goal of low−side current sensing is to detect over−current conditions or as a method of feedback control. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

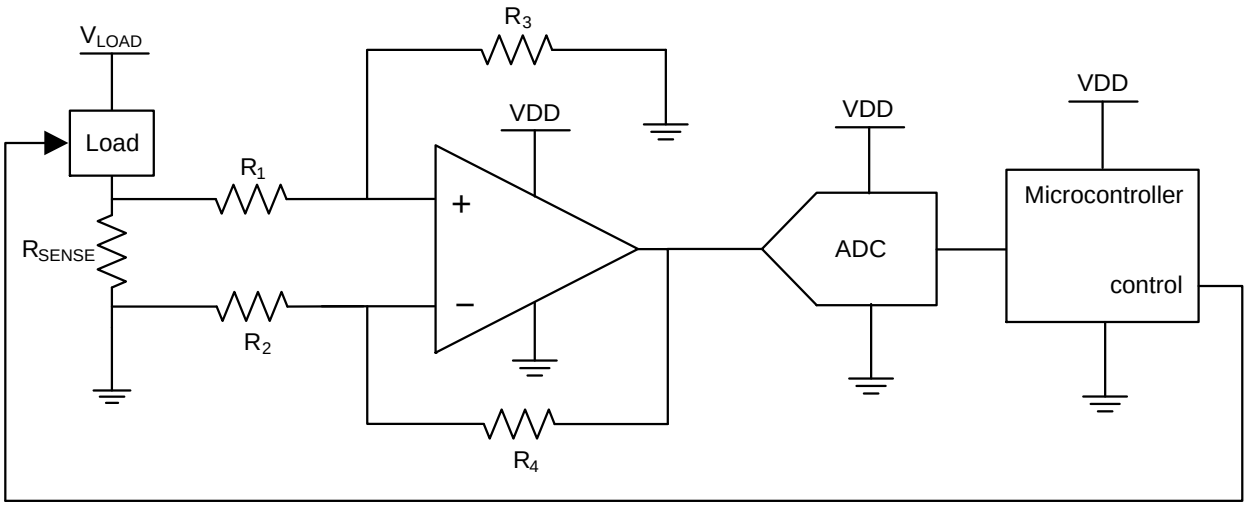


Figure 17. Low−Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 18. In the measurement, the voltage change that is produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

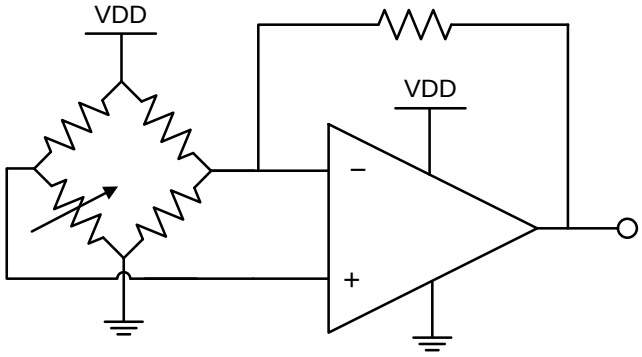


Figure 18. Bridge Circuit Amplification

EMI Susceptibility and Input Filtering

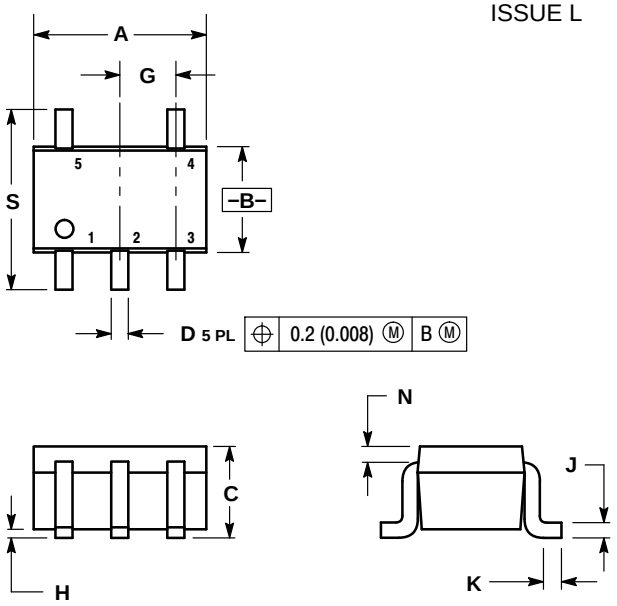
Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI−induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS333 op amp family integrates low−pass filters to decrease sensitivity to EMI.

General Layout Guidelines

To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface−mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric−coefficients and prevent temperature gradients from heat sources or cooling fans.

PACKAGE DIMENSIONS

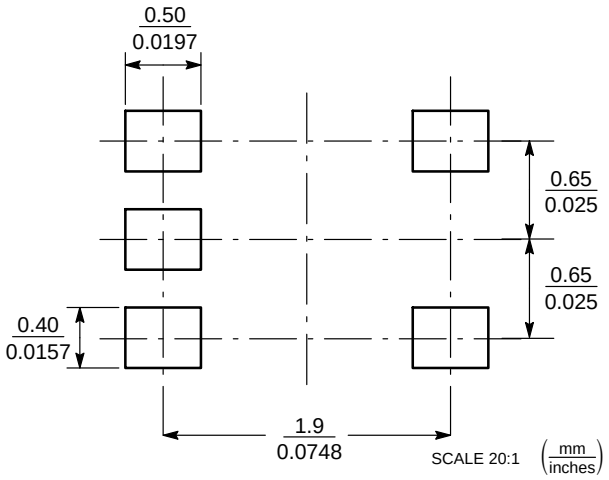
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

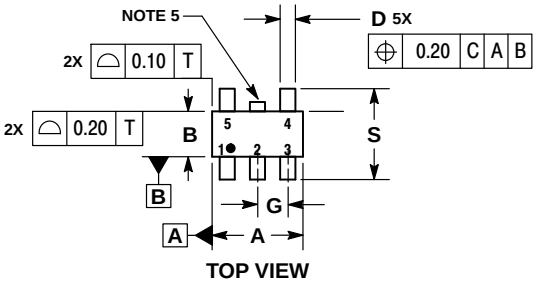
SOLDER FOOTPRINT

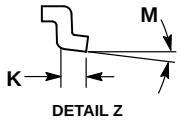


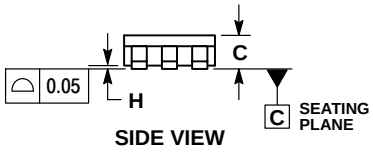
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

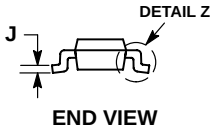
PACKAGE DIMENSIONS

TSOP−5
CASE 483−02
ISSUE K





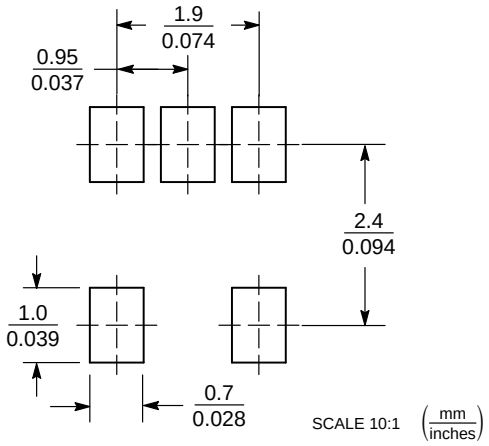




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

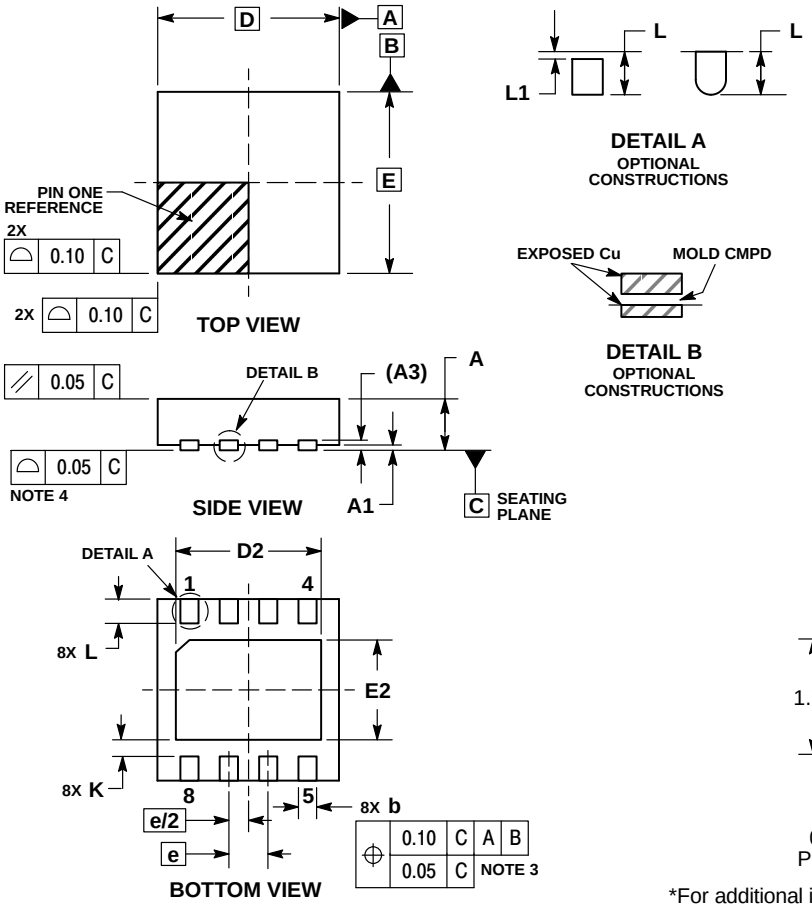
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

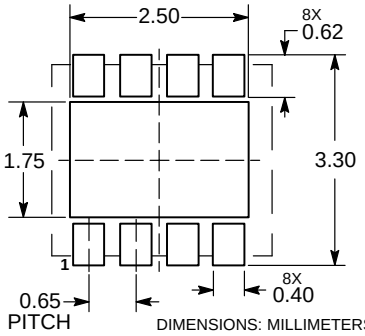
DFN8, 3x3, 0.65P
CASE 506BW
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.30	2.50
E	3.00 BSC	
E2	1.55	1.75
e	0.65 BSC	
K	0.20	–––
L	0.35	0.45
L1	0.00	0.15

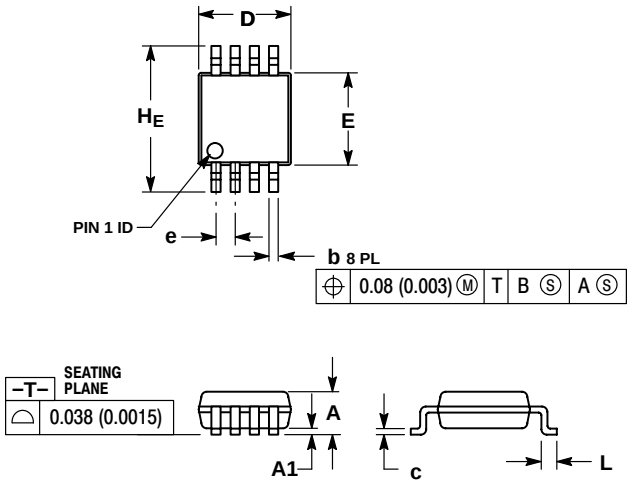
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

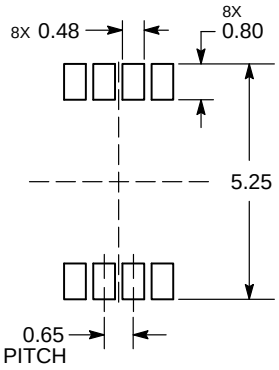
Micro8™
CASE 846A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65 BSC			0.026 BSC	
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

RECOMMENDED SOLDERING FOOTPRINT*

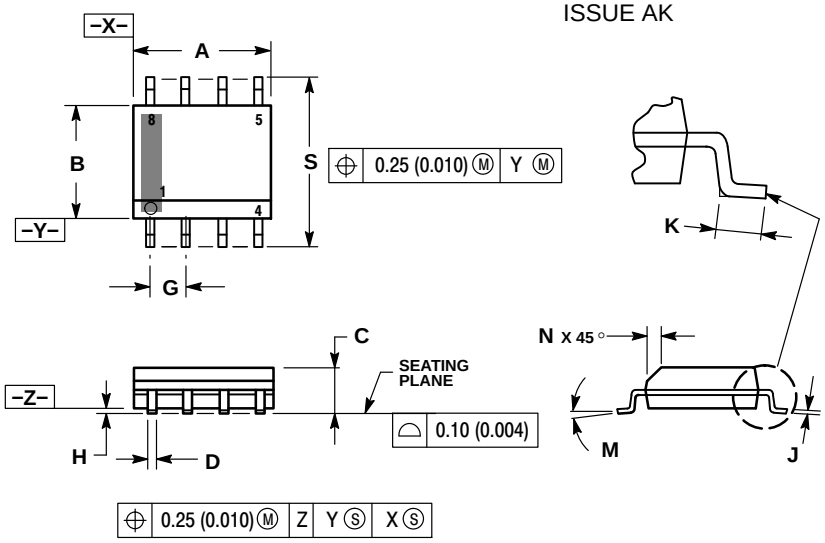


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

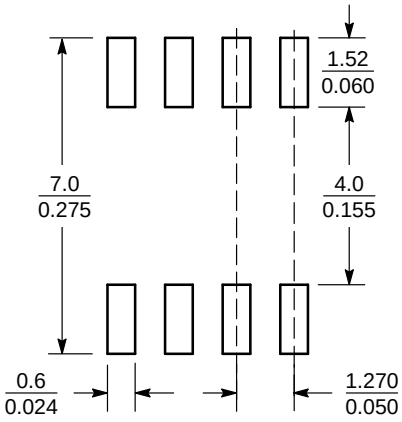
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

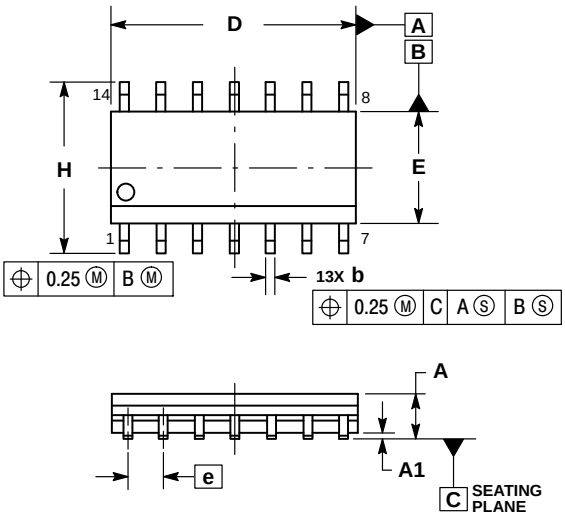


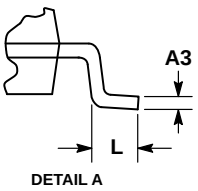
SCALE 6:1 (mm / inches)

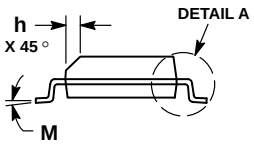
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE K



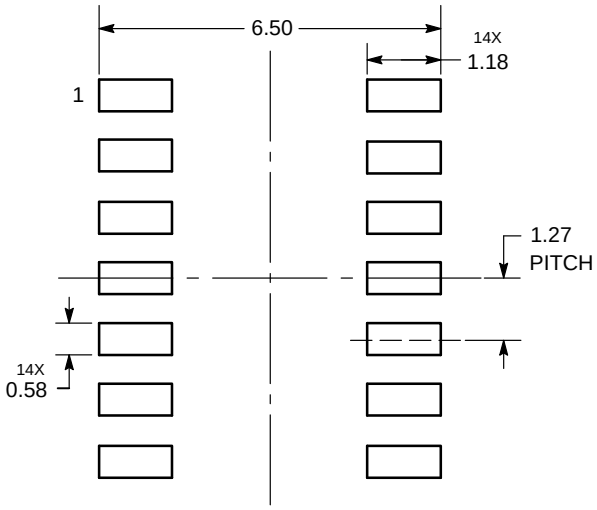




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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