NIV1161, NIS1161

ESD Protection with Automotive Short-to-Battery Blocking

Low Capacitance ESD Protection with short−to−battery blocking for Automotive High Speed Data Lines

The NIS/NIV1161 is designed to protect high speed data lines from ESD as well as short to vehicle battery situations. The ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines while the low $R_{DS(on)}$ FET limits distortion on the signal lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB and LVDS protocols.

Features

- Low Capacitance (0.65 pF Typical, I/O to GND)
- Protection for the Following Standards:
  IEC 61000−4−2 (Level 4) & ISO 10605
- Integrated MOSFETs for Short−to−Battery Blocking
- NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive High Speed Signal Pairs
- USB 2.0/3.0
- LVDS
- APIX 2/3

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	$T_{J(max)}$	−55 to +150	°C
Storage Temperature Range	TSTG	−55 to +150	°C
Drain−to−Source Voltage	V_{DSS}	30	V
Gate−to−Source Voltage	V_{GS}	±10	V
Lead Temperature Soldering	T_{SLD}	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±8 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ON Semiconductor®

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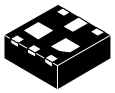
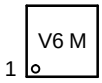
MARKING DIAGRAM

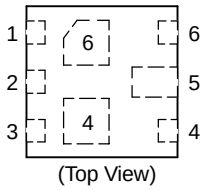


WDFN6
CASE 511CB

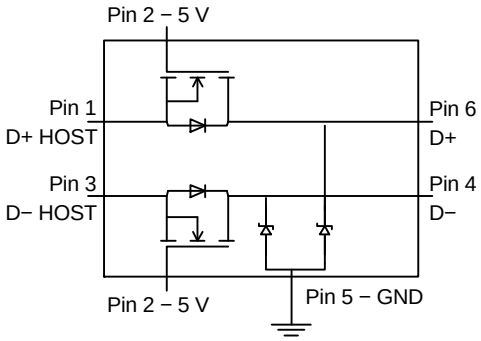


V6 = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATICS



(Top View)



ORDERING INFORMATION

Device	Package	Shipping†
NIV1161MTTAG	WDFN−6 (Pb−Free)	3000 / Tape & Reel
NIS1161MTTAG	WDFN−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND		5	16	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	16.5			V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND			1.0	μA
Clamping Voltage	V_C	I_{PP} = 1 A, I/O Pin to GND (8/20 μs pulse)			26	V
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 KV Contact	See Figures 1 & 2			
Clamping Voltage TLP (Note 2) See Figures 5 & 6	V_C	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		34 55 −5.2 −10		V V V V
Junction Capacitance Match	ΔC_J	V_R = 0 V, f = 1 MHz between I/O 1 to GND and I/O 2 to GND		1.0		%
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND (Pin 4 to GND, Pin 6 to GND)		0.65		pF
Drain−to−Source Breakdown Voltage	$V_{BR(DSS)}$	V_{GS} = 0 V, I_D = 100 μA	30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{BR(DSS)}/T_J$	Reference to 25°C, I_D = 100 μA		27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 30 V			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V			±1.0	μA
Gate Threshold Voltage (Note 3)	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 100 μA	0.1	1.0	1.5	V
Gate Threshold Voltage Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to 25°C, I_D = 100 μA		−2.5		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 125 mA		1.4	7.0	Ω
		V_{GS} = 2.5 V, I_D = 125 mA		2.3	7.5	
Forward Transconductance	g_{FS}	V_{DS} = 3.0 V, I_D = 125 mA		80		mS
Switching Turn−On Delay Time (Note 4)	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 24 V I_D = 125 mA, R_G = 10 VΩ		9		nS
Switching Turn−On Rise Time (Note 4)	t_r			41		nS
Switching Turn−Off Delay Time (Note 4)	$t_{d(OFF)}$			96		nS
Switching Turn−Off Fall Time (Note 4)	t_f			72		nS
Drain−to−Source Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_s = 125 mA		0.79	0.9	V
3 dB Bandwidth	f_{BW}	R_L = 50 Ω		5		GHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 3 and 4 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.
3. Pulse test: pulse width ≤ 300 μS, duty cycle ≤ 2%
4. Switching characteristics are independent of operating junction temperatures.

Figure 1. IEC61000−4−2 +8kV Contact ESD Clamping Voltage

Figure 2. IEC61000−4−2 −8kV Contact ESD Clamping Voltage

IEC61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

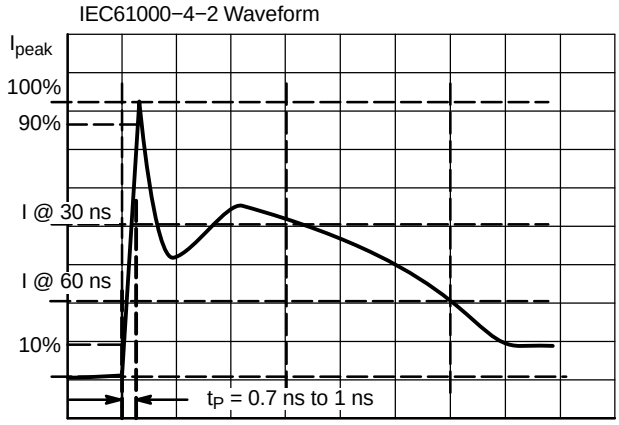


Figure 3. IEC61000−4−2 Spec

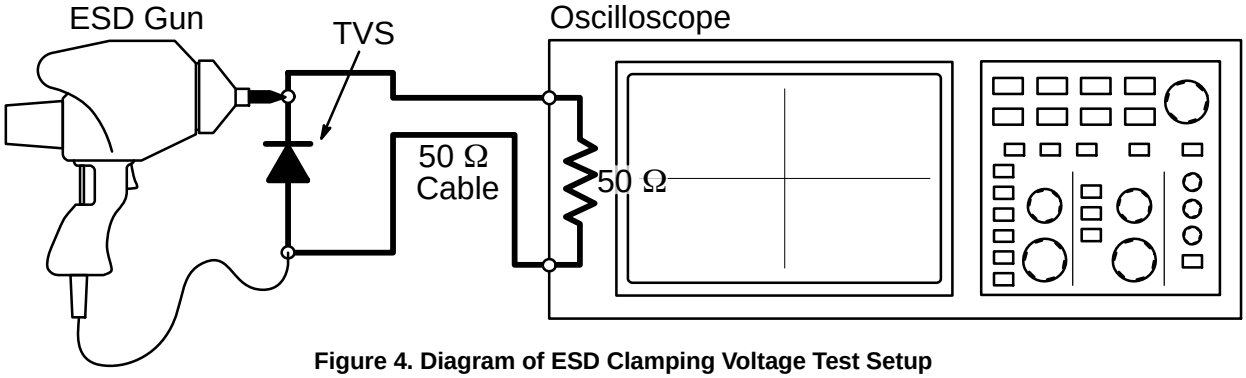


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8307/D − Characterization of ESD Clamping Performance.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

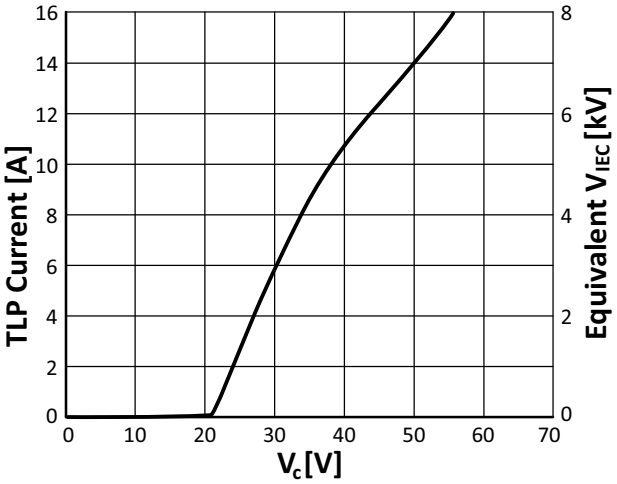


Figure 5. Positive TLP I−V Curve

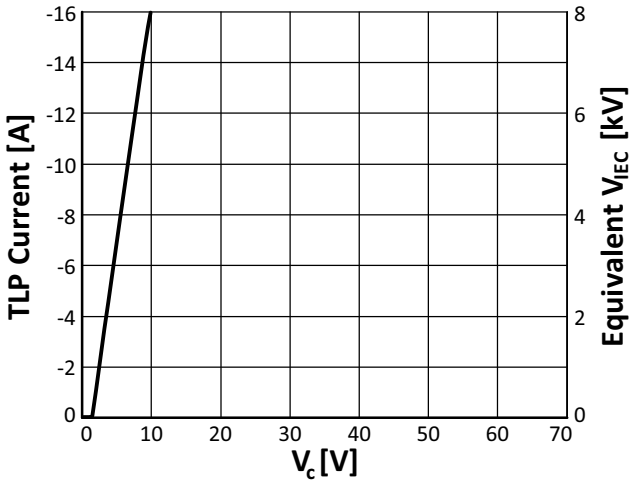


Figure 6. Negative TLP I−V Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

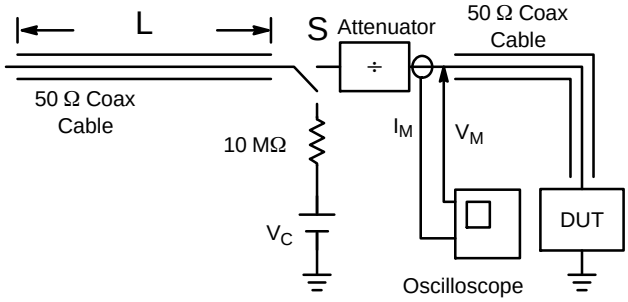


Figure 7. Simplified Schematic of a Typical TLP System

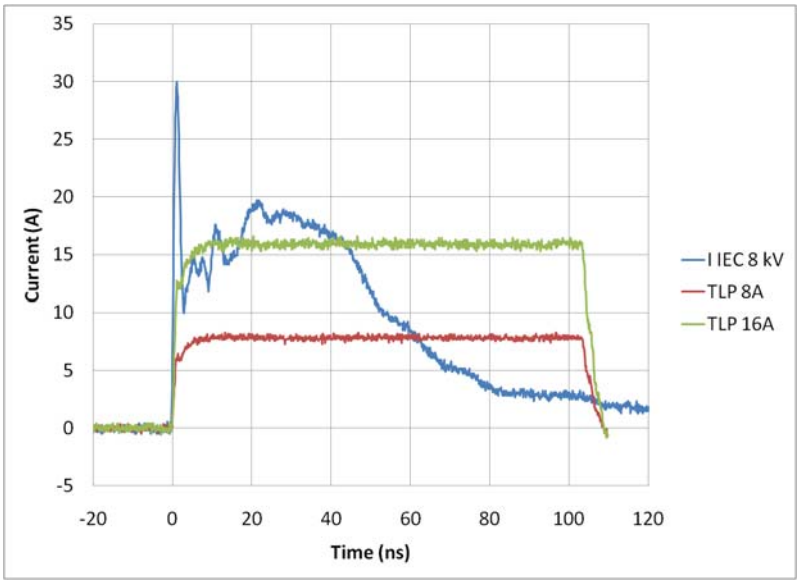


Figure 8. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

TYPICAL MOSFET PERFORMANCE CURVES

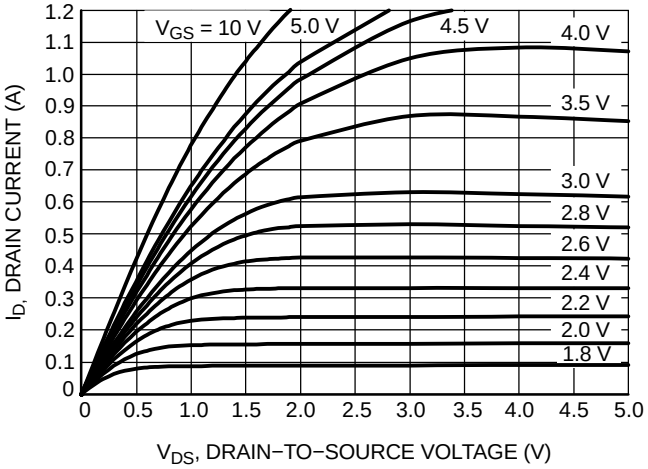


Figure 9. On−Region Characteristics

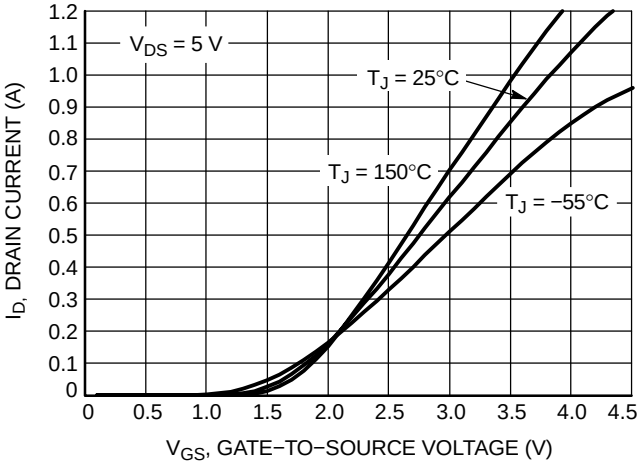


Figure 10. Transfer Characteristics

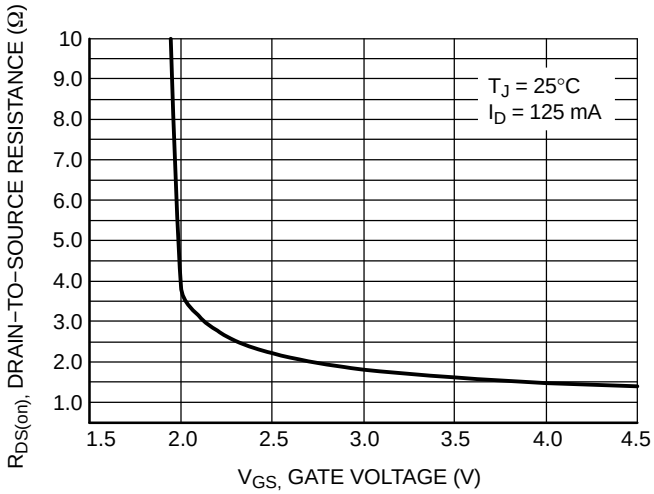


Figure 11. On−Resistance vs. Gate−to−Source Voltage

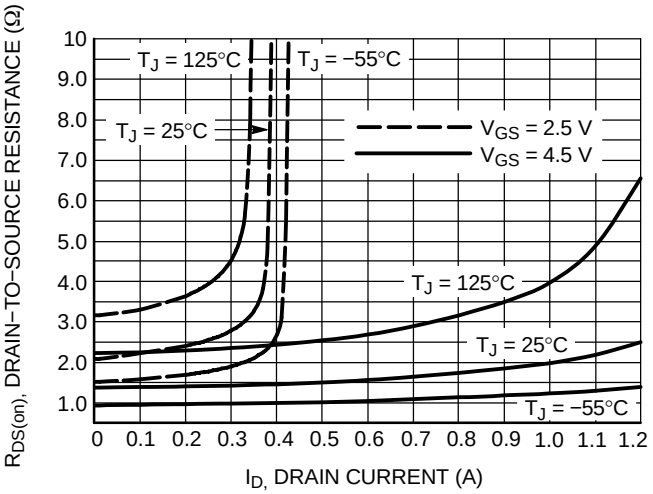


Figure 12. On−Resistance vs. Drain Current and Gate Voltage

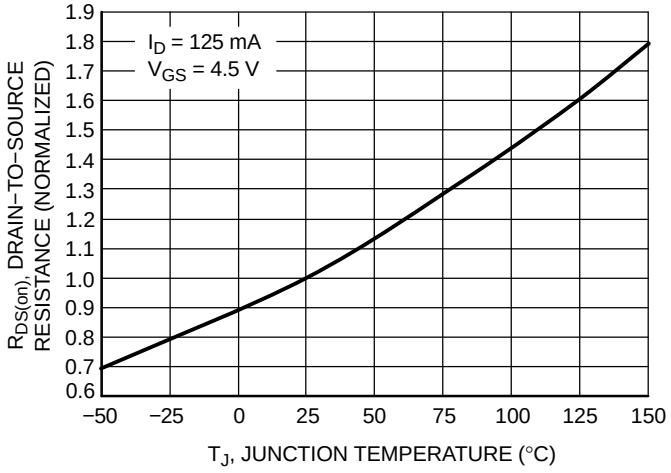


Figure 13. On−Resistance Variation with Temperature

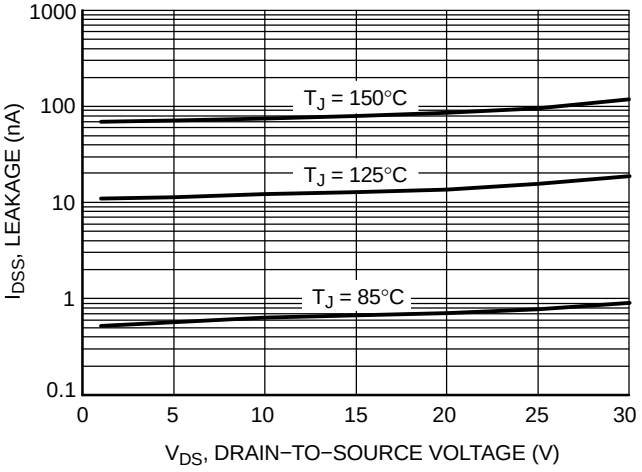
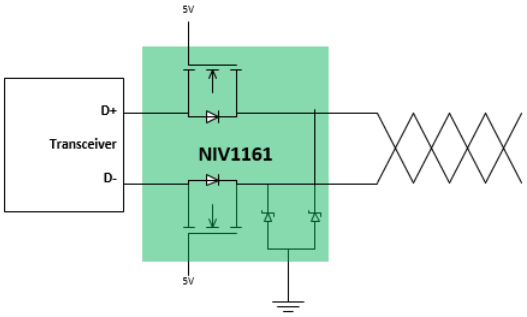


Figure 14. Drain−to−Source Leakage Current vs. Voltage

APPLICATION INFORMATION

Today's connected cars are using multiple high speed signal pair interfaces for various applications such as infotainment, connectivity and ADAS. The electrical hazards likely to be encountered in these automotive high speed signal interfaces include damaging ESD and transient events which occur during manufacturing and assembly, by vehicle occupants or other electrical circuits in the vehicle. The major documents discussing ESD and transient events as far as road vehicles are concerned are ISO 10605 (Road vehicles − Test methods for electrical disturbances from electrostatic discharge) which describes ESD test methods and ISO 7637 (Road vehicles − Electrical disturbances from conduction and coupling) for effects caused by other electronics in the vehicle. IS0 10605 is based on IEC 61000−4−2 Industry Standard, which specifies the various levels of ESD signal characteristics, but also includes additional vehicle−specific requirements. Further, OEM specific test requirements are usually also imposed. In addition, these high speed signal pairs require protection from short−to−battery (which goes up to 16 VDC) and short−to−ground faults.

A suitable protection solution must satisfy well known constraints, such as low capacitive loading of the signal lines to minimize signal attenuation, and also respond quickly to surges and transients with low clamping voltage. In addition, small package sizes help to minimize demand for board−space while providing the ability to route the trace signals with minimal bending to maintain signal integrity.



PCB Layout Guidelines

It is optional to route both pins 4 & 6 to their respective belly pads with a top metal trace as both pins are internally connected respectively. Also, steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
  - Use curved traces when possible to avoid unwanted reflections.
  - Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
  - Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

Modes of Operation

There are two distinct modes of operation of the NIV1161: normal (steady state) and short−to−battery event. The below describes each of these in more detail.

Normal Operation (Steady State)

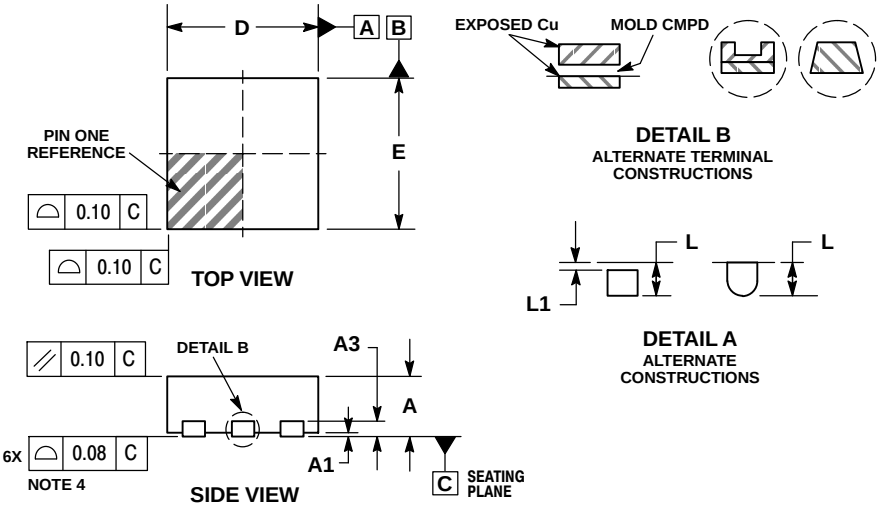
In normal operation, the MOSFETs operate in linear mode, with all source and drain voltages nearly equal, passing the signal levels effectively from the USB transceiver. To ensure successful link communication, the applied gate voltage must be greater than the maximum signal level from the data line plus the maximum threshold voltage of the MOSFET device. Due to the NIV1161's low of 1.5 V, both 3.3 and 5 V gate drives are suitable to provide headroom for most communication protocols. The net effect of the 1 kΩ pull−up resistor on the MOSFET gate to the source effectively level−shifts the common mode voltage on the individual data lines up to the gate voltage. This action is cancelled out when an appropriate NIV1161 is used on the opposite side of the data line to level−shift the common−mode voltage back down to levels appropriate for the reader. If a NIV1161 is not used on the opposite side of the data line, the pull−up resistor may either not be populated or populated with high value resistor (15 kΩ+); differential data signal integrity is maintained.

Short−to−Battery (STB) Event

While the NIV1161 and data channel are off, one pair of MOSFET body diodes passively protects the USB transceiver's ports. While the data channel is on during an event, the NIV1161 actively uses the internal MOSFETs to clamp in a manner akin to level−shifting as the MOSFET operates in the saturation region. The source node will increase to a threshold voltage minus a working below the gate voltage thus allowing current to flow into the data port impedance until the gate−source voltage comes to rest just above the threshold voltage. In this way, the NIV1161 protects the data port by limiting the termination current as well as voltage clamping the data port itself.

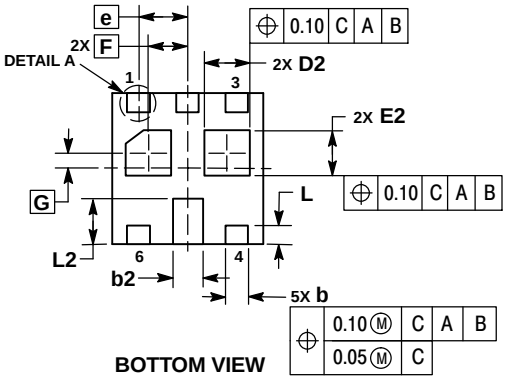
PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P
CASE 511CB
ISSUE O

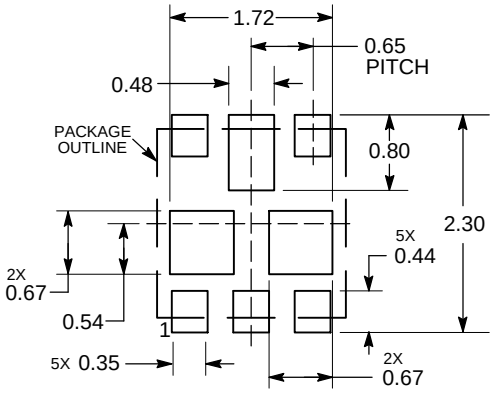


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b2	0.35	0.45
D	2.00 BSC	
D2	0.55	0.65
E	2.00 BSC	
E2	0.55	0.65
e	0.65 BSC	
F	0.52 BSC	
G	0.20 BSC	
L	0.20	0.30
L1	---	0.15
L2	0.55	0.65



RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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