

# NJW3281G (NPN) NJW1302G (PNP)

## Complementary NPN-PNP Silicon Power Bipolar Transistors

The NJW3281G and NJW1302G are power transistors for high power audio, disk head positioners and other linear applications.

### Features

- Exceptional Safe Operating Area
- NPN/PNP Gain Matching within 10% from 50 mA to 5 A
- Excellent Gain Linearity
- High BVCEO
- High Frequency
- These Devices are Pb-Free and are RoHS Compliant

### Benefits

- Reliable Performance at Higher Powers
- Symmetrical Characteristics in Complementary Configurations
- Accurate Reproduction of Input Signal
- Greater Dynamic Range
- High Amplifier Bandwidth

### Applications

- High-End Consumer Audio Products
  - ◆ Home Amplifiers
  - ◆ Home Receivers
- Professional Audio Amplifiers
  - ◆ Theater and Stadium Sound Systems
  - ◆ Public Address Systems (PAs)

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	250	Vdc
Collector-Base Voltage	$V_{CBO}$	250	Vdc
Emitter-Base Voltage	$V_{EBO}$	5.0	Vdc
Collector-Emitter Voltage - 1.5 V	$V_{CEX}$	250	Vdc
Collector Current - Continuous	$I_C$	15	Adc
Collector Current - Peak (Note 1)	$I_{CM}$	30	Adc
Base Current - Continuous	$I_B$	1.6	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.625	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

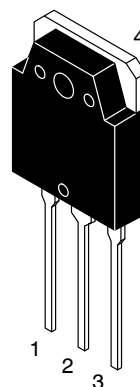
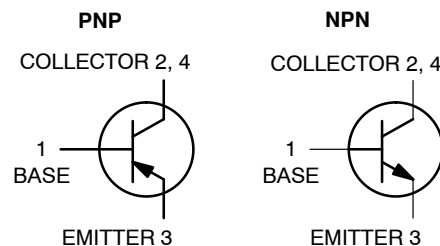
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.



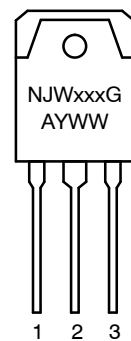
ON Semiconductor®

<http://onsemi.com>

## 15 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS 200 WATTS



### MARKING DIAGRAM



TO-3P  
CASE 340AB  
STYLES 1,2,3

xxxx = 0281 or 0302  
G = Pb-Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
NJW3281G	TO-3P (Pb-Free)	30 Units/Rail
NJW1302G	TO-3P (Pb-Free)	30 Units/Rail

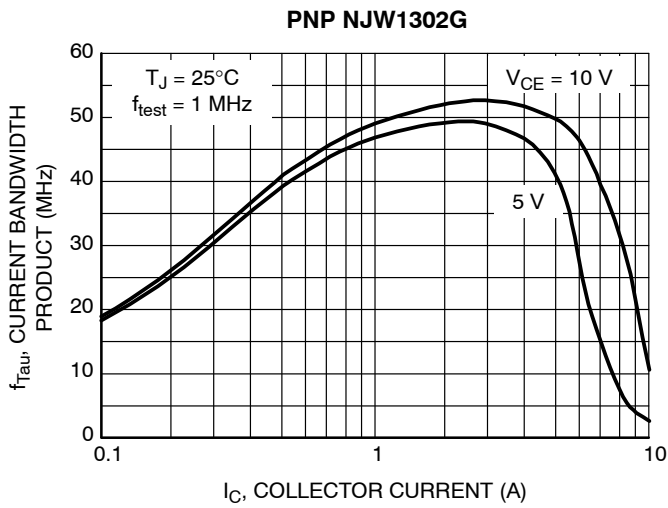
## NJW3281G (NPN) NJW1302G (PNP)

### ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

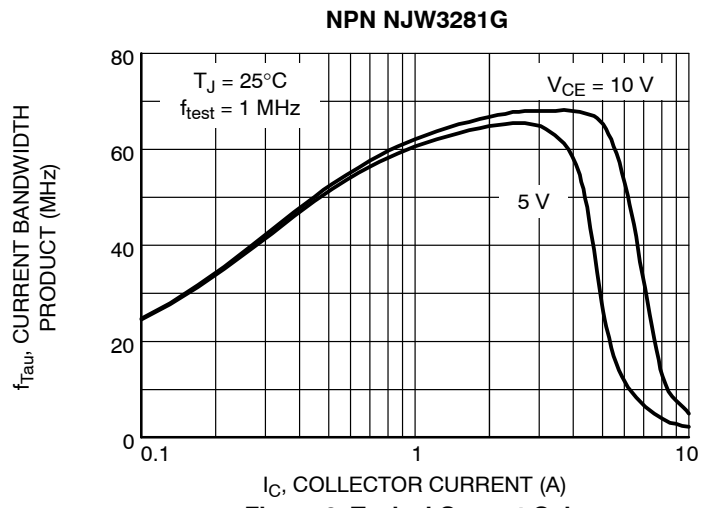
Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 100 mAdc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	250	–	–	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 250 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	50	μAdc
Emitter Cutoff Current (V <sub>EB</sub> = 5 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	5	μAdc
<b>SECOND BREAKDOWN</b>					
Second Breakdown Collector with Base Forward Biased (V <sub>CE</sub> = 50 Vdc, t = 1 s (non-repetitive))	I <sub>S/b</sub>	4	–	–	Adc
<b>ON CHARACTERISTICS</b>					
DC Current Gain (I <sub>C</sub> = 100 mAdc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 1 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 3 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 5 Adc, V <sub>CE</sub> = 5 Vdc) (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc)	h <sub>FE</sub>	75 75 75 60 45	– – – – –	150 150 150 – –	–
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 8 Adc, I <sub>B</sub> = 0.8 Adc)	V <sub>CE(sat)</sub>	–	0.4	0.6	Vdc
Base-Emitter On Voltage (I <sub>C</sub> = 8 Adc, V <sub>CE</sub> = 5 Vdc)	V <sub>BE(on)</sub>	–	–	1.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current-Gain – Bandwidth Product (I <sub>C</sub> = 1 Adc, V <sub>CE</sub> = 5 Vdc, f <sub>test</sub> = 1 MHz)	f <sub>T</sub>	–	30	–	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f <sub>test</sub> = 1 MHz)	C <sub>ob</sub>	–	–	600	pF

# NJW3281G (NPN) NJW1302G (PNP)

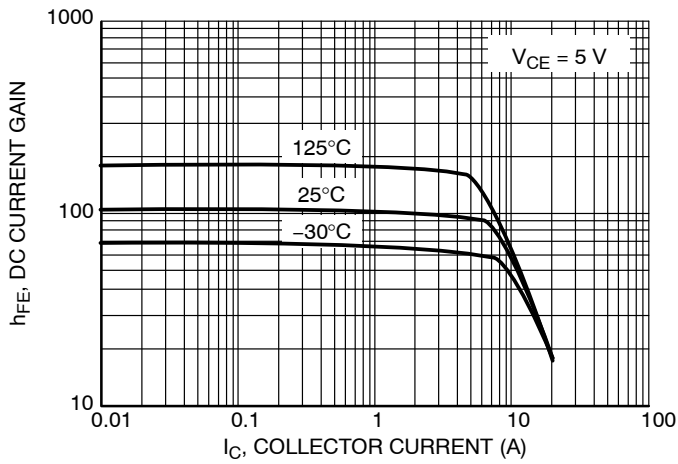
## TYPICAL CHARACTERISTICS



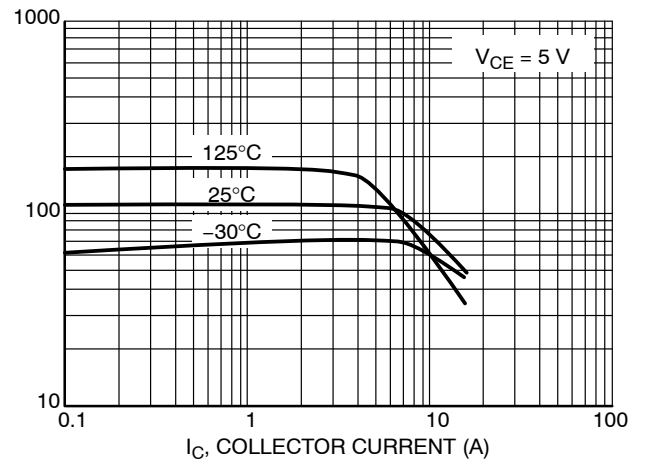
**Figure 1. Typical Current Gain Bandwidth Product**



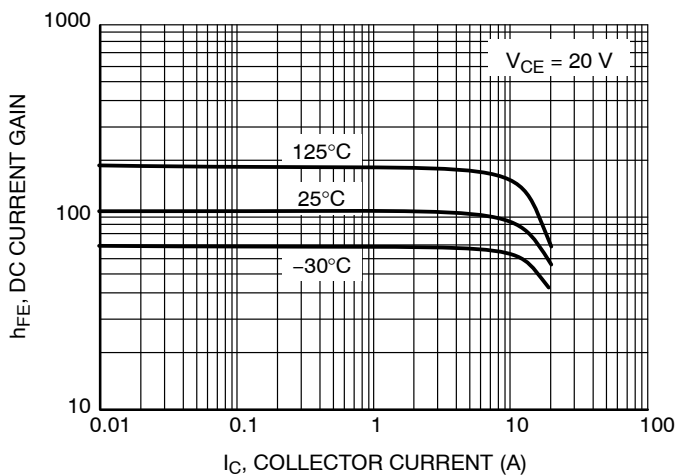
**Figure 2. Typical Current Gain Bandwidth Product**



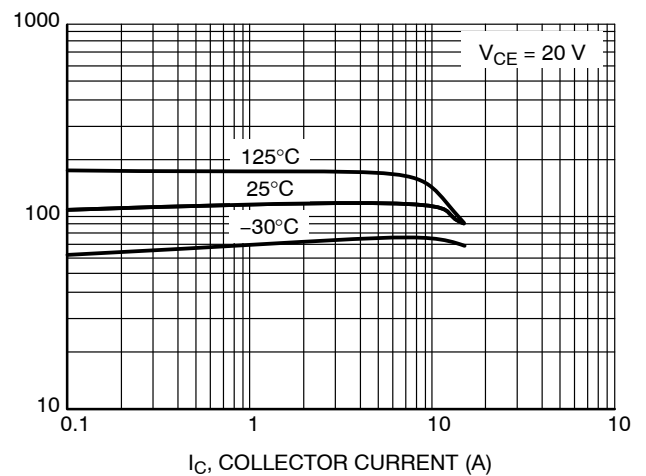
**Figure 3. DC Current Gain**



**Figure 4. DC Current Gain**



**Figure 5. DC Current Gain**



**Figure 6. DC Current Gain**

TYPICAL CHARACTERISTICS

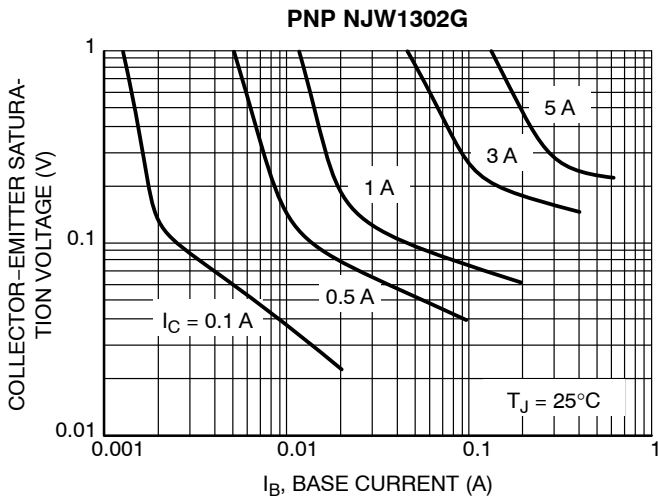


Figure 7. Saturation Region

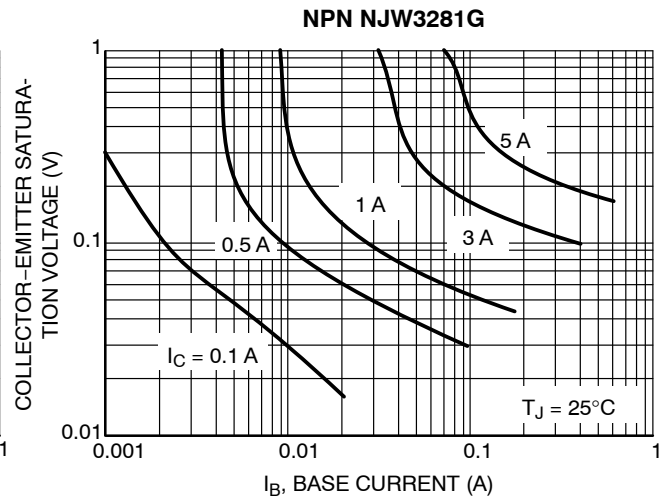


Figure 8. Saturation Region

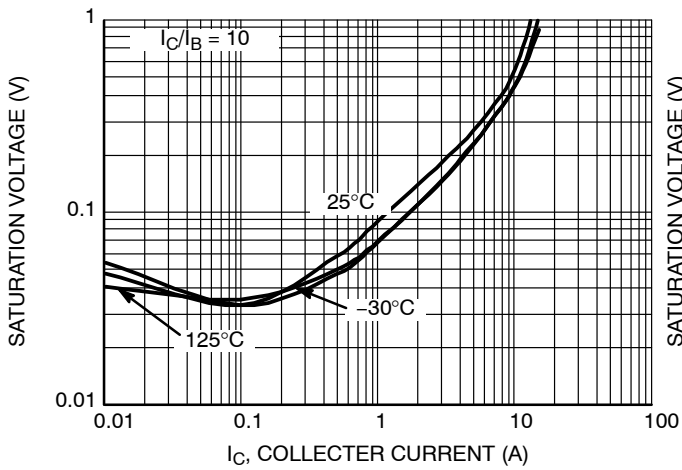


Figure 9.  $V_{CE(sat)}$ , Collector-Emitter Saturation Voltage

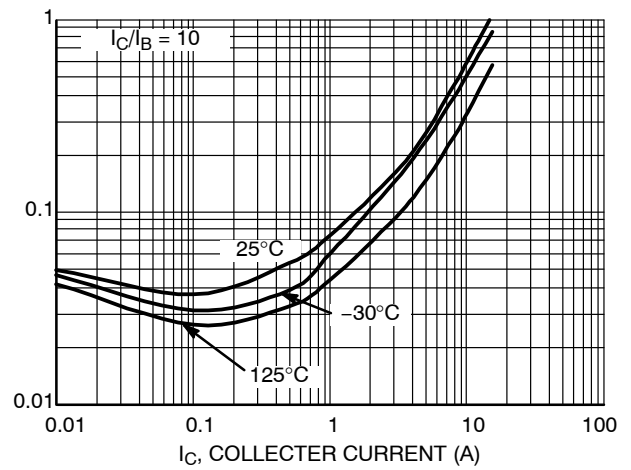


Figure 10.  $V_{CE(sat)}$ , Collector-Emitter Saturation Voltage

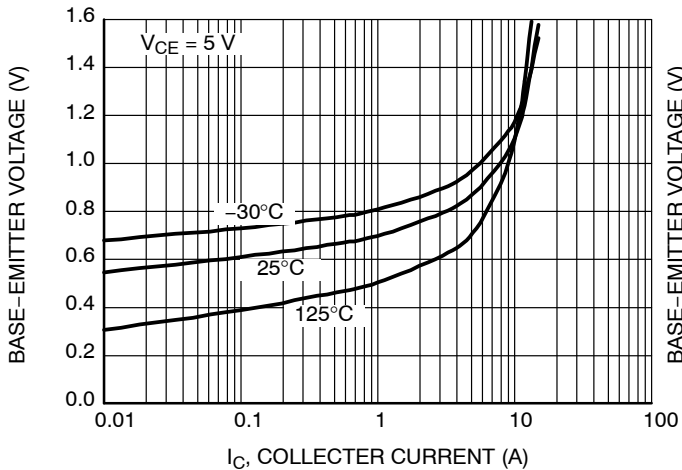


Figure 11.  $V_{BE(on)}$ , Base-Emitter Voltage

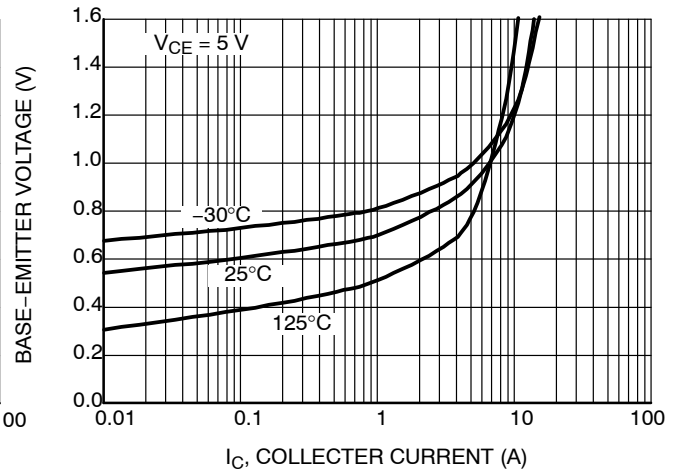
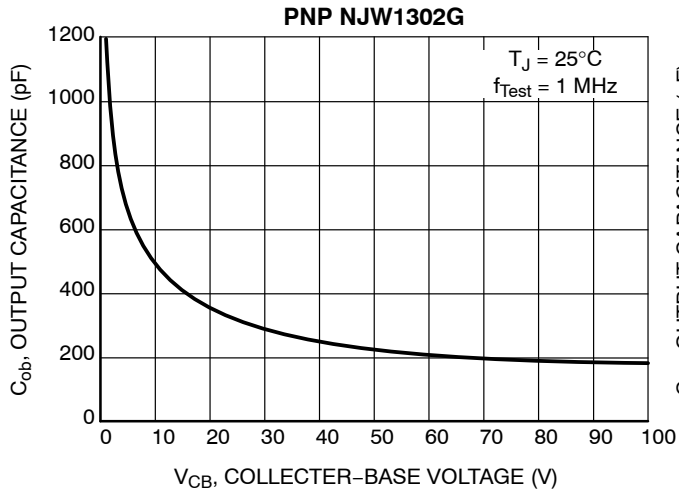


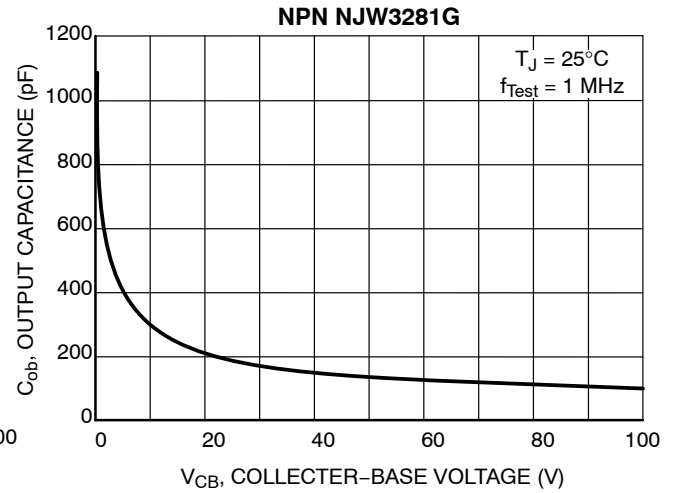
Figure 12.  $V_{BE(on)}$ , Base-Emitter Voltage

# NJW3281G (NPN) NJW1302G (PNP)

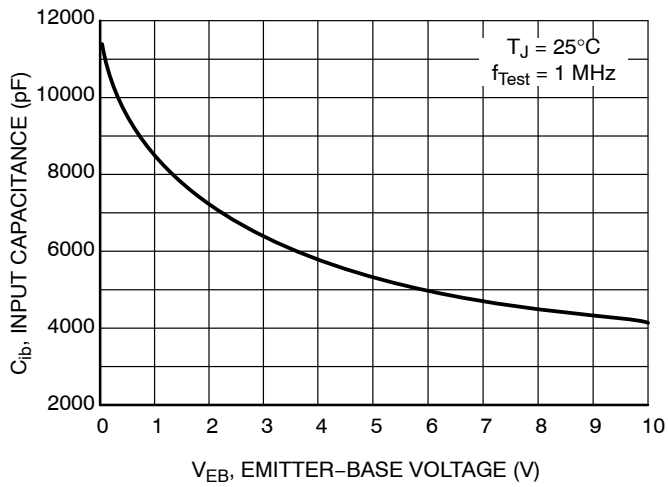
## TYPICAL CHARACTERISTICS



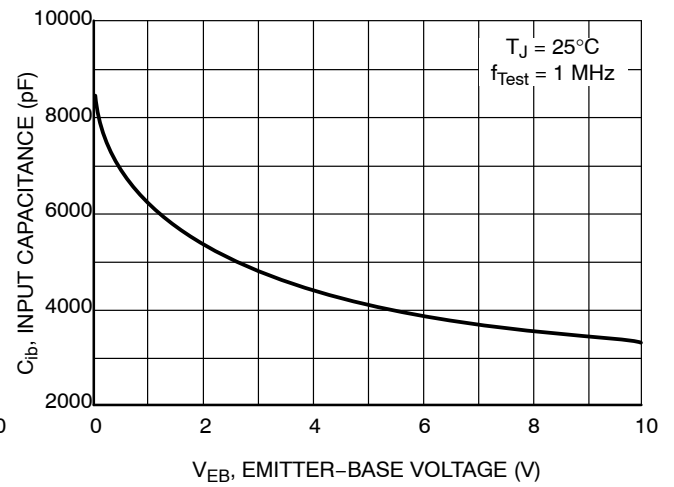
**Figure 13. Output Capacitance**



**Figure 14. Output Capacitance**

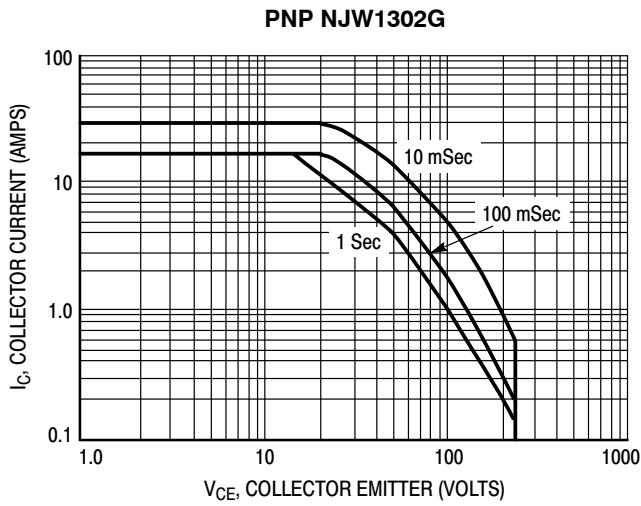


**Figure 15. Input Capacitance**



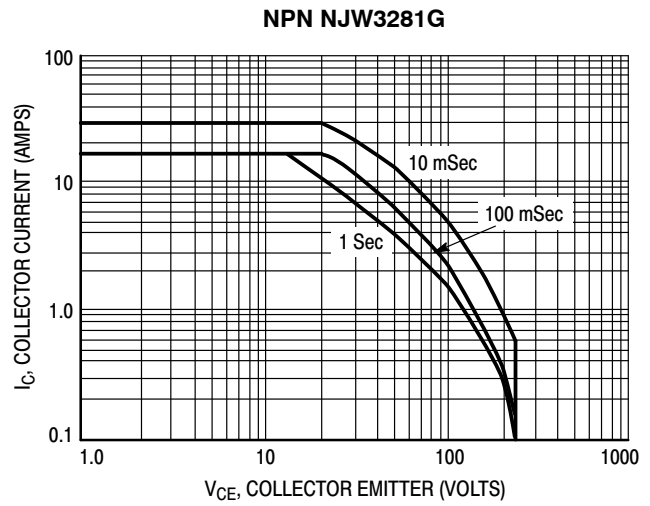
**Figure 16. Input Capacitance**

## NJW3281G (NPN) NJW1302G (PNP)



**Figure 17. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.



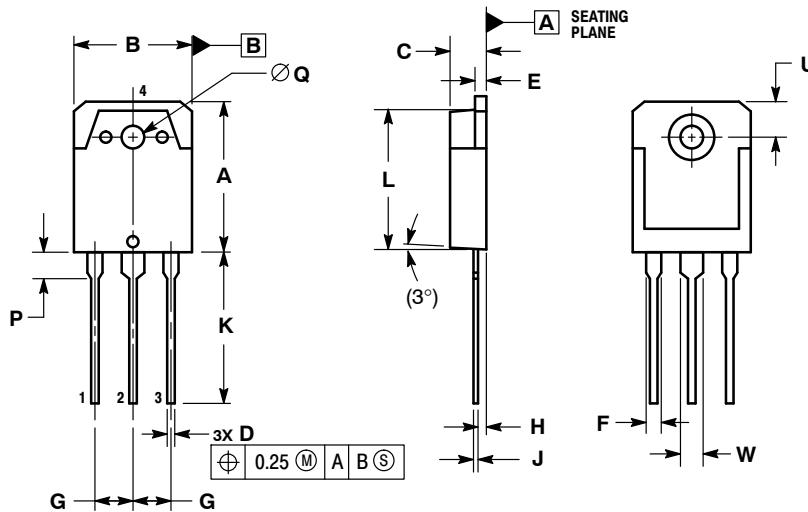
**Figure 18. Active Region Safe Operating Area**

The data of Figures 17 and 18 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

# NJW3281G (NPN) NJW1302G (PNP)

## PACKAGE DIMENSIONS

TO-3P-3LD  
CASE 340AB-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. DIMENSION A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	19.70	19.90	20.10
B	15.40	15.60	15.80
C	4.60	4.80	5.00
D	0.80	1.00	1.20
E	1.45	1.50	1.65
F	1.80	2.00	2.20
G	5.45 BSC		
H	1.20	1.40	1.60
J	0.55	0.60	0.75
K	19.80	20.00	20.20
L	18.50	18.70	18.90
P	3.30	3.50	3.70
Q	3.10	3.20	3.50
U	5.00 REF		
W	2.80	3.00	3.20

### STYLE 1:


- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

### STYLE 2:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

### STYLE 3:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5817-1050

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[NJW3281G](#) [NJW1302G](#)