

# 1.5V Drive Pch MOSFET

### RZF030P01

### Structure

Silicon P-channel MOSFET

### Features

- 1) Low on-resistance.
- 2) High power package.
- 3) Low voltage drive. (1.5V)

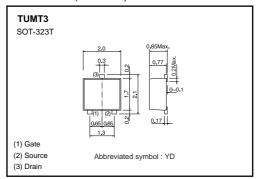
### Applications

Switching

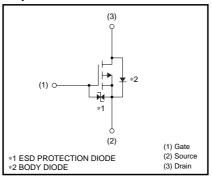
### Packaging specifications

	Package	Taping	
Type	Code	TL	
	Basic ordering unit (pieces)	3000	
RZF030P01		0	

### ●Dimensions (Unit:mm)



### ●Equivalent circuit



### ● Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		$V_{DSS}$	-12	V
Gate-source voltage		V <sub>GSS</sub>	±10	V
Drain aurrent	Continuous	I <sub>D</sub>	±3	Α
Drain current	Pulsed	I <sub>DP</sub> *1	±12	Α
Source current	Continuous	ls *1	-0.65	Α
(Body diode)	Pulsed	I <sub>SP</sub>	-12	Α
Total power dissipation		P <sub>D</sub> *2	0.8	W
Channel temperature		Tch	150	°C
Range of Storage temperature		Tstg	-55 to +150	°C
Range of Storage temperature		Tstg	-55 to +150	°C

<sup>\*1</sup> Pw≤10μs, Duty cycle≤1% \*2 Mounted on a ceramic board

### Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) *	156	°C / W

<sup>\*</sup> Mounted on a ceramic board.

RZF030P01 Data Sheet

### ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	Igss	-	ı	±10	μΑ	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V(BR) DSS	-12	-	_	V	ID= -1mA, VGS=0V
Zero gate voltage drain current	I <sub>DSS</sub>	_	-	-1	μΑ	V <sub>DS</sub> = -12V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS (th)</sub>	-0.3	_	-1.0	V	$V_{DS} = -6V$ , $I_{D} = -1mA$
Static drain-source on-state resistance	R <sub>DS (on)</sub>	_	28	39	mΩ	I <sub>D</sub> = -3A, V <sub>G</sub> S= -4.5V
		_	39	54	mΩ	Ip= -1.5A, Vgs= -2.5V
		_	51	76	mΩ	I <sub>D</sub> = -1.5A, V <sub>G</sub> S= -1.8V
		_	72	144	mΩ	I <sub>D</sub> = -0.6A, V <sub>G</sub> S= -1.5V
Forward transfer admittance	Y <sub>fs</sub>  *	5	-	_	S	V <sub>DS</sub> = -6V, I <sub>D</sub> = -3A
Input capacitance	Ciss	_	1860	_	pF	Vps= -6V
Output capacitance	Coss	_	210	_	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	Crss	_	200	_	pF	f=1MHz
Turn-on delay time	t <sub>d (on)</sub> *	_	9	_	ns	ID= -1.5A
Rise time	tr *	_	40	_	ns	V <sub>DD</sub> ≒ −6V
Turn-off delay time	td (off) *	_	210	_	ns	VGS= -4.5V RL≒4Ω
Fall time	t <sub>f</sub> *	_	120	_	ns	R <sub>G</sub> =10Ω
Total gate charge	Qg *	_	18	_	nC	V <sub>DD</sub> ≒−6V R <sub>L</sub> ≒2Ω
Gate-source charge	Q <sub>gs</sub> *	_	3.0	_	nC	$I_D = -3A$ $R_G = 10\Omega$
Gate-drain charge	Q <sub>gd</sub> *	_	2.5	_	nC	V <sub>GS</sub> = -4.5V

<sup>\*</sup>Pulsed

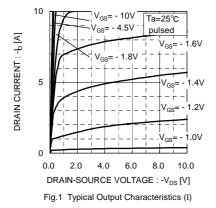
### ●Body diode characteristics (Source -drain) (Ta=25°C)

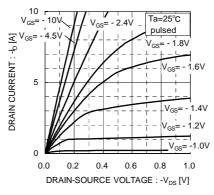
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	Vsp*	_	_	-1.2	V	I <sub>S</sub> = -3A, V <sub>GS</sub> =0V

<sup>\*</sup>Pulsed

RZF030P01 Data Sheet

### Electrical characteristic curves





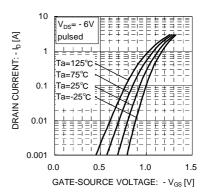


Fig.2 Typical Output Characteristics (  ${\mathbb I}$  ) Fig.3 Typical Transfer Characteristics

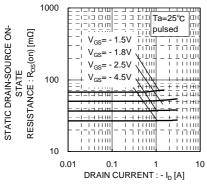


Fig.4 Static Drain-Source On-State Resistance vs.Drain Current

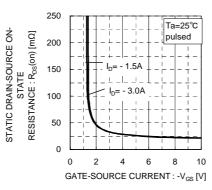


Fig.5 Static Drain-Source On-State
Resistance vs.Gate-Source Voltage

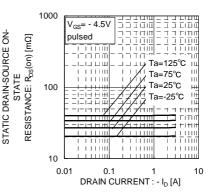


Fig.6 Static Drain-Source On-State Resistance vs.Drain Current

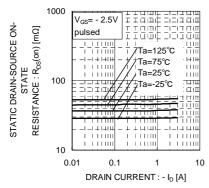


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current

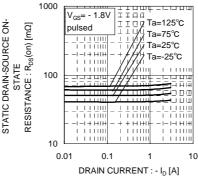


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current

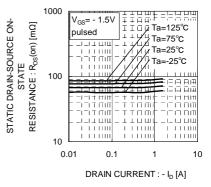


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current

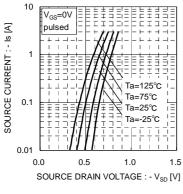


Fig.10 Source Current vs. Source-Drain Voltage

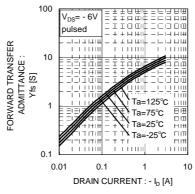


Fig.11 Forward Transfer Admittance vs. Drain Current

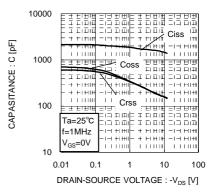


Fig.12 Typical Capacitance vs. Drain-Source Voltage

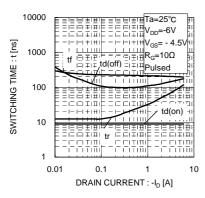


Fig.13 Switching Characteristics

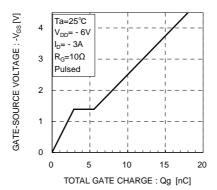


Fig.14 Dynamic Input Characteristics

RZF030P01 Data Sheet

### Measurement circuits

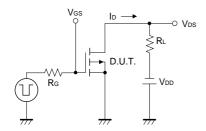


Fig.1-1 Switching Time Measurement Circuit

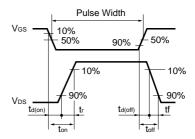


Fig.1-2 Switching Waveforms

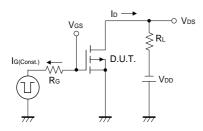


Fig.2-1 Gate Charge Measurement Circuit

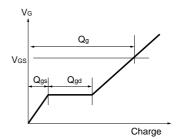


Fig.2-2 Gate Charge Waveforms

### ●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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