

4V Drive Pch+Pch MOSFET

SH8J65

●Structure

Silicon P-channel MOSFET

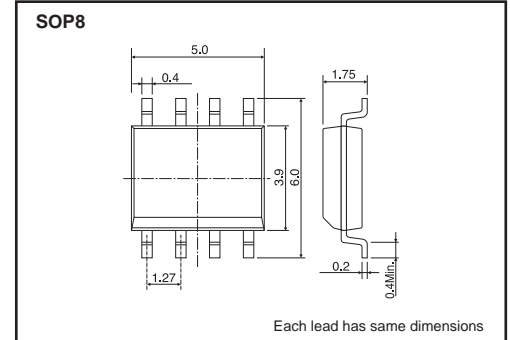
●Features

- 1) Low On-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

●Application

Switching

●Dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SH8J65		○

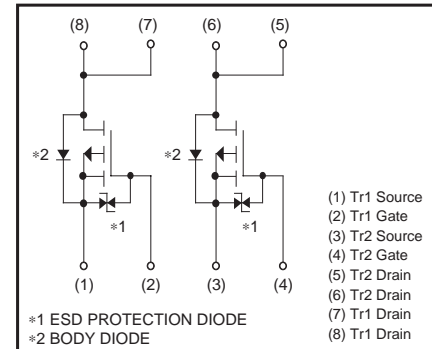
●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DS}	-30	V	
Gate-source voltage	V_{GS}	±20	V	
Drain current	Continuous	I_D	±7.0	A
	Pulsed	I_{DP} *1	±28	A
Source current (Body diode)	Continuous	I_S	-1.6	A
	Pulsed	I_{SP} *1	-28	A
Total power dissipation	P_D *2	2.0	W / TOTAL	
		1.4	W / ELEMENT	
Channel temperature	T_{ch}	150	°C	
Range of Storage temperature	T_{stg}	-55 to +150	°C	

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$
*2 Mounted on a ceramic board

●Inner circuit



●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	± 10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–30	–	–	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS}=-30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	–1.0	–	–2.5	V	$V_{DS}=-10V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	21.5	29.0	m Ω	$I_D=-7A, V_{GS}=-10V$
		–	29.0	39.0	m Ω	$I_D=-3.5A, V_{GS}=-4.5V$ *
		–	31.0	40.8	m Ω	$I_D=-3.5A, V_{GS}=-4.0V$ *
Forward transfer admittance	$ Y_{fs} $ *	6.0	–	–	S	$V_{DS}=-10V, I_D=-7A$ *
Input capacitance	C_{iss}	–	1200	–	pF	$V_{DS}=-10V$
Output capacitance	C_{oss}	–	170	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	–	170	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	12	–	ns	$V_{DD}=-15V$
Rise time	t_r *	–	40	–	ns	$I_D=-3.5A$ $V_{GS}=-10V$
Turn-off delay time	$t_{d(off)}$ *	–	80	–	ns	$R_L=4.3\Omega$
Fall time	t_f *	–	65	–	ns	$R_G=10\Omega$
Total gate charge	Q_g *	–	18	–	nC	$V_{DD}=-15V$
Gate-source charge	Q_{gs} *	–	3.5	–	nC	$I_D=-7A$ $V_{GS}=-5V$
Gate-drain charge	Q_{gd} *	–	6.5	–	nC	$R_L=2.1\Omega / R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-Drain) (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	$I_S=-7A, V_{GS}=0V$

*Pulsed

●Electrical characteristic curves

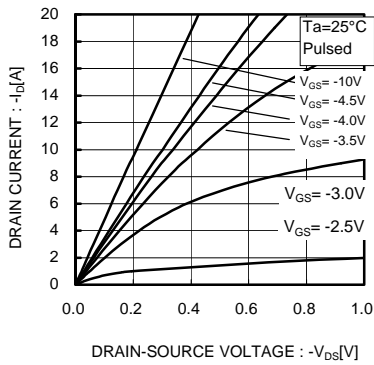


Fig.1 Typical Output Characteristics(I)

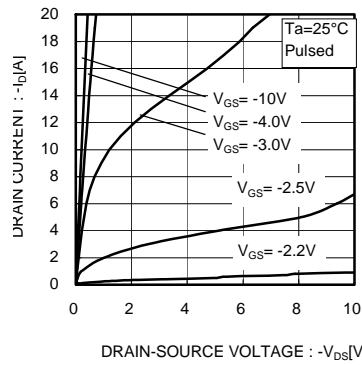


Fig.2 Typical Output Characteristics(II)

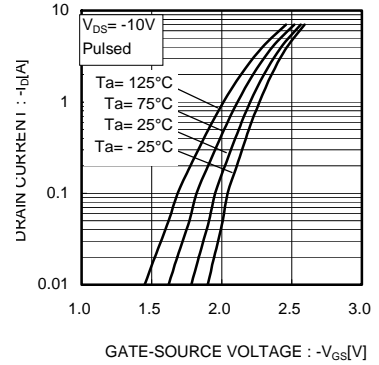


Fig.3 Typical Transfer Characteristics

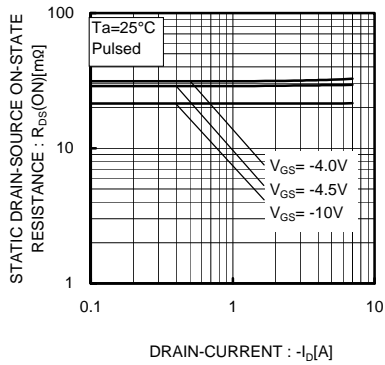


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

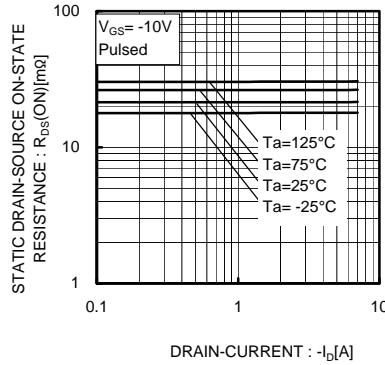


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

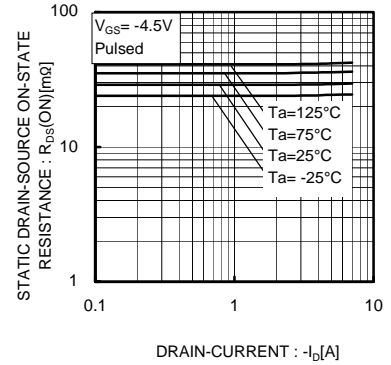


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

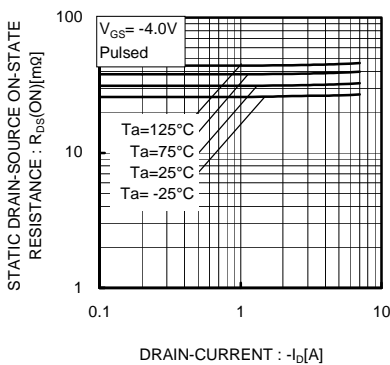


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

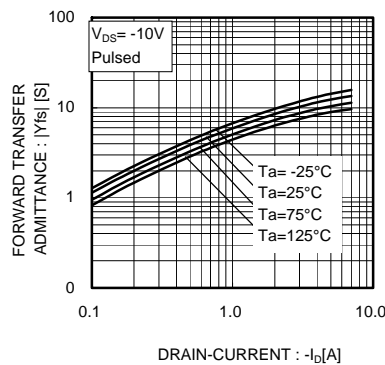


Fig.8 Forward Transfer Admittance vs. Drain Current

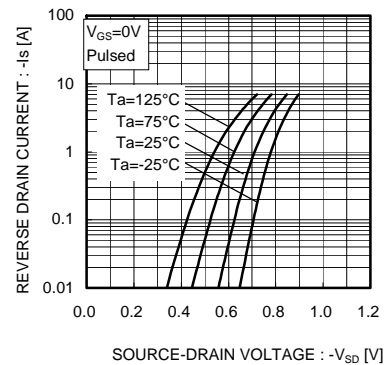


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

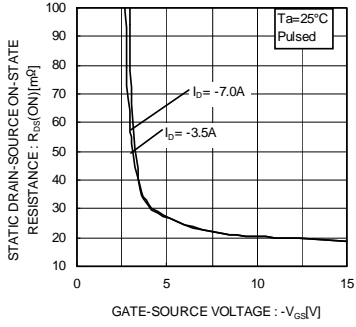


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

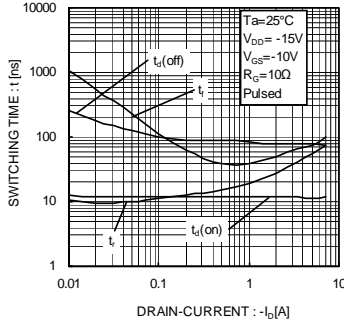


Fig.11 Switching Characteristics

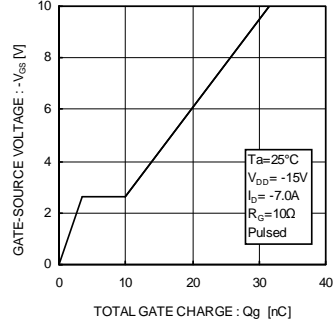


Fig.12 Dynamic Input Characteristics

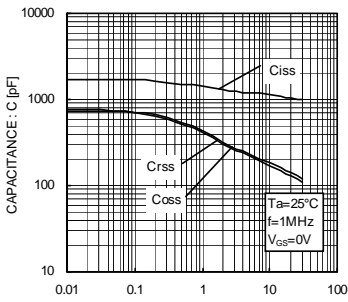


Fig.13 Typical Capacitance vs. Drain-Source Voltage

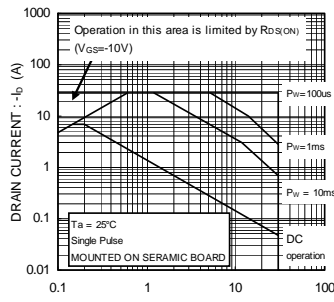


Fig.14 Maximum Safe Operating Area

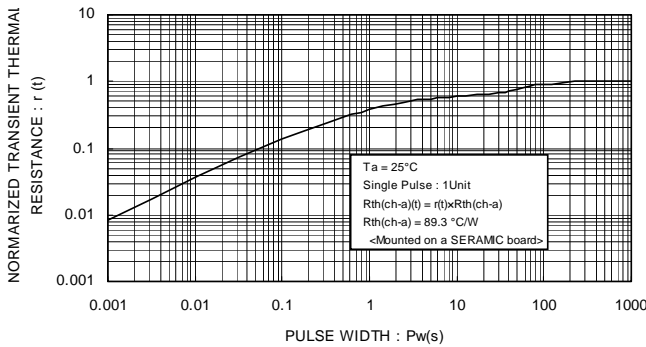


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width

●Measurement circuits

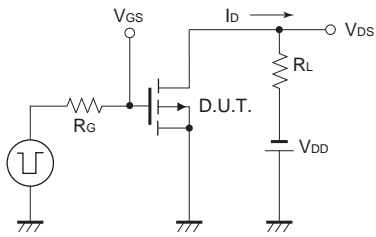


Fig.16 Switching Time Test Circuit

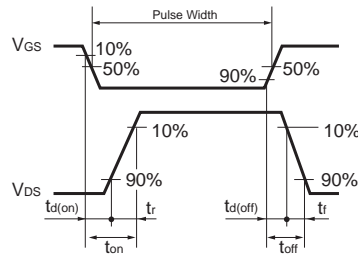


Fig.17 Switching Time Waveforms

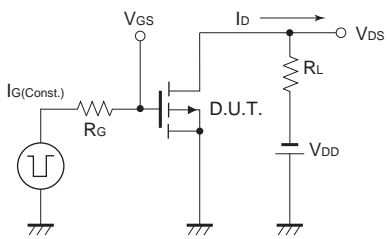


Fig.18 Gate Charge Test Circuit

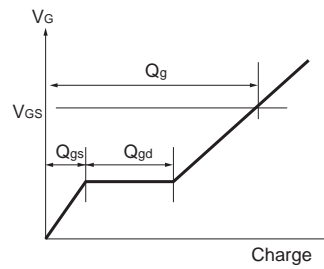


Fig.19 Gate Charge Waveform

Notes

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