

TRIUNE PRODUCTS

Features

- Supports standards (Qi®, PMA, A4WP) and proprietary wireless power applications
- Power outputs scalable based on FET size
- Support for half and full-bridge power sections
- Integrated demodulator amplifiers
- Low external component count
- Available in 28 pin 5x5 QFN

Applications

- Multi-standard compliant and non-compliant wireless chargers for:
 - Cell Phones and Smartphones
 - GPS Devices
 - Digital Cameras
 - Tablets and eReaders
- Full and half-bridge power converters
- Motor drive applications

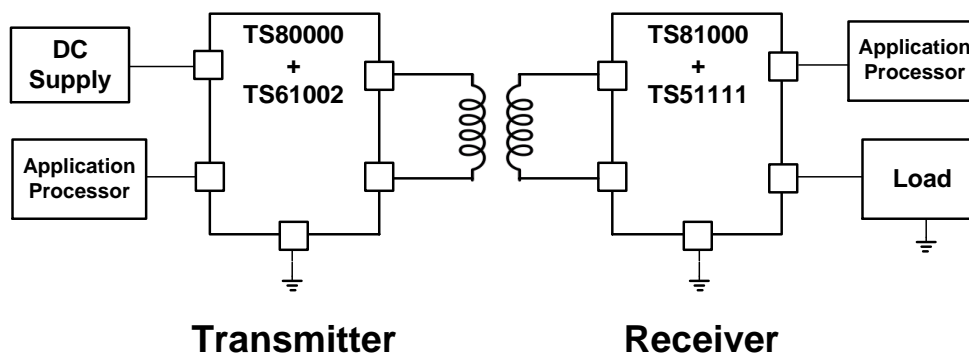
Description

TS61002 is a high-voltage FET driver that can be used to drive N-channel devices in full or half bridge configurations. TS61002 can support various power converter applications, multiple standard and proprietary wireless power applications, and motor driver systems.

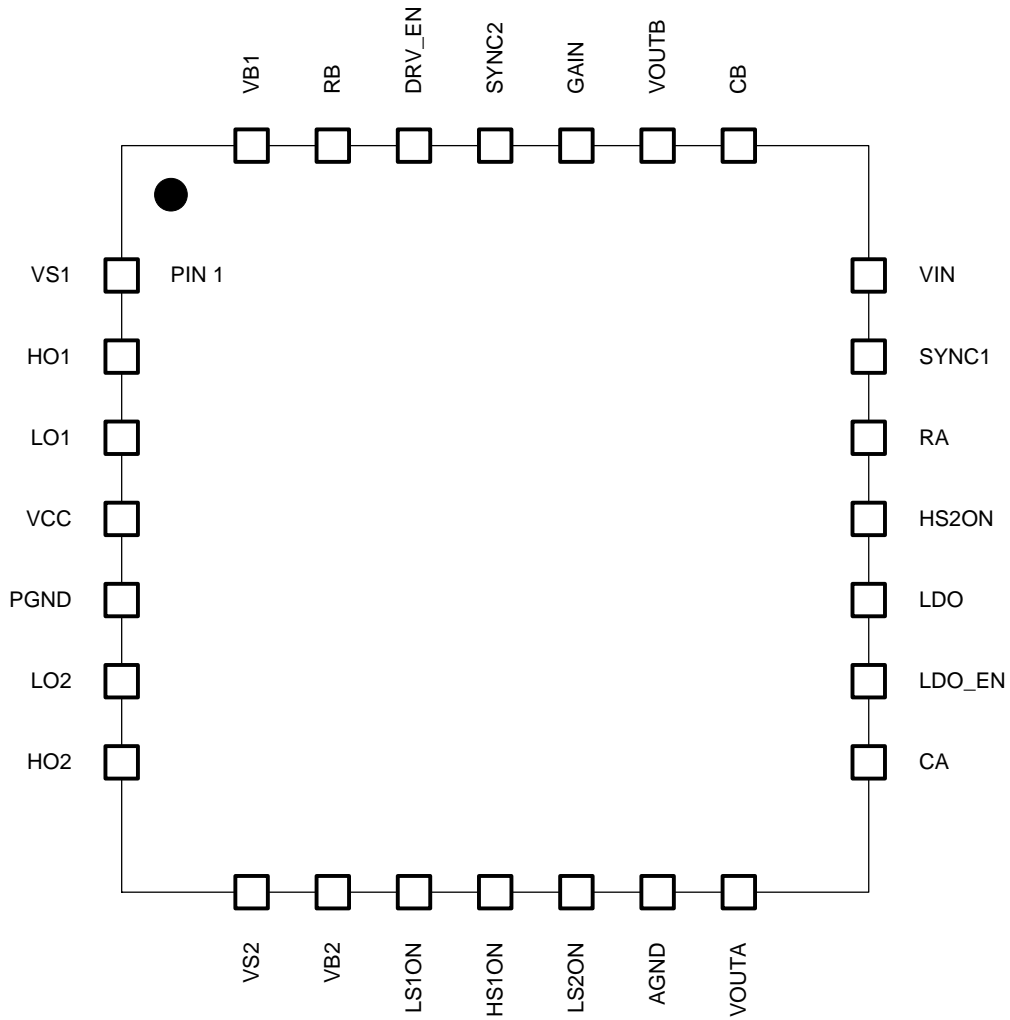
Specifications

- Drives both low side and high side N-channel MOSFETS
- 5Ω pull-up, 2Ω pull-down gate drivers
- Independent TTL compatible inputs
- Floating gate drive and bootstrap circuits for driving high side devices – up to 50V for the bridge supply voltage
- 5 V gate drive capability, down to 3.5V operation
- Fast propagation delays (<50ns~120ns typical)
- Matched channel to channel delays (<40ns mismatch typical)
- Fast rise and fall times
- Break before make detection to set minimum dead time protection
- Proprietary demodulator circuits for wireless power transmitter application
- High PSR 3.0V linear regulator (50mA capability) for supporting circuitry & external controller
- Under voltage lock out protection
- Over temperature shut down (TSD) protection

Typical Application Circuit



Pin Configuration

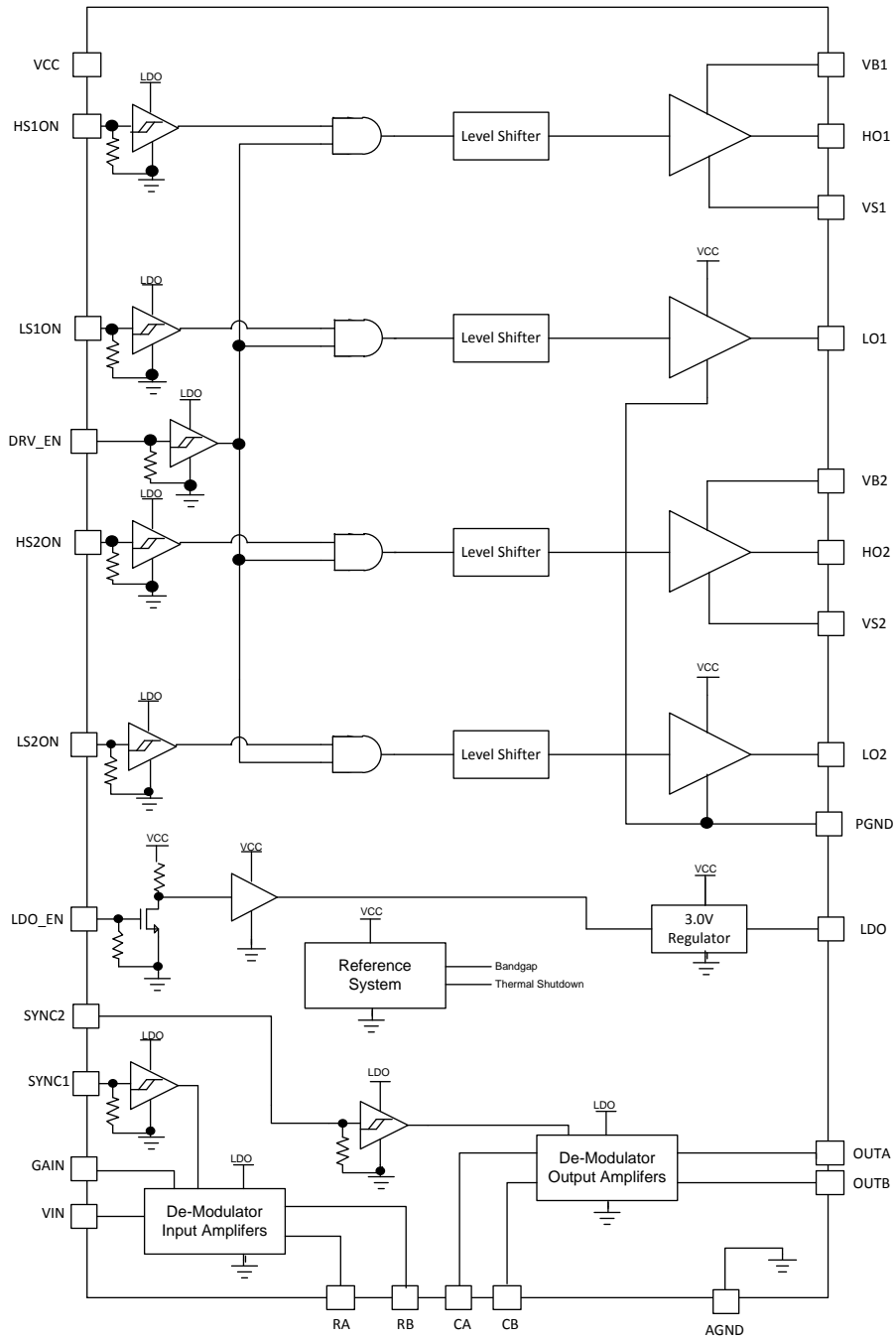


(Top View)

Pin Configuration

QFN Pin #	Pin Symbol	Function	Description
1	VS1	FET drive	High side MOSFET source #1
2	HO1	FET drive	High side MOSFET gate drive #1
3	LO1	FET drive	Low side MOSFET gate drive #1
4	VCC	Gate drive input power	Input power supply (gate drive supply)
5	PGND	Power GND	Power GND
6	LO2	FET drive	Low side MOSFET gate drive #2
7	HO2	FET drive	High side MOSFET gate drive #2
8	VS2	FET drive	High side MOSFET source #2
9	VB2	Bootstrap	Bootstrap for gate drive #2
10	LS1ON	PWM1_L	Low-side gate control #1 with 30k Ω pull-down to GND
11	HS1ON	PWM1_H	High-side gate control #1 with 30k Ω pull-down to GND
12	LS2ON	PWM2_L	Low-side gate control #2 with 30k Ω pull-down to GND
13	AGND	Analog GND	Analog GND
14	VOUTA	Demodulator	Demodulator output A
15	CA	Demodulator	Demodulator input CA
16	LDO_EN	LDO enable	LDO enable (active high) with 30k Ω pull-down to GND
17	VLDO	LDO output	3.0V regulator output and decoupling
18	HS2ON	PWM2_H	High-side gate control #2 with 30k Ω pull-down to GND
19	RA	Demodulator	Demodulator output RA
20	SYNC1	Demodulator	Demodulator SYNC1 input with 30k Ω pull-down to GND
21	VIN	Demodulator	Demodulator input
22	CB	Demodulator	Demodulator input CB
23	VOUTB	Demodulator	Demodulator output B
24	GAIN	Demodulator	Demodulator input gain setting
25	SYNC2	Demodulator	Demodulator SYNC2 input with 30k Ω pull-down to GND
26	DRV_EN	Gate drive enable	Gate drive enable (active high) with 30k Ω pull-down to GND
27	RB	Demodulator	Demodulator output RB
28	VB1	Bootstrap	Bootstrap for gate drive #1

Functional Block Diagram



Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted (1, 2)

Parameter	Value	Unit
VCC, LO1, LO2	8.0	V
VS1, VS2	50	V
VB1, VB2, HO1, HO2	8.0 (relative to VS1, VS2)	V
LDO_EN	8.0	V
LS1ON, LS2ON, HS1ON, HS2ON, DRV_EN	3.6	V
VIN, GAIN, RA, RB, CA, CB, SYNC1, SYNC2, DRV_EN, VOUTA, VOUTB	3.6	V
Electrostatic Discharge – Human Body Model (VS1, HO1, LO1, VCC, PGND, LO2, HO2, VS2, VB2, HS1ON, AGND, LDO_EN, VB1)	+/-2k	V
Electrostatic Discharge – Human Body Model (LS1ON, LS2ON, VOUTA, CA, LDO, HS2ON, RA, SYNC1, VIN, CB, VOUTB, GAIN, SYNC2, DRV_EN, RB)	+/-1k	V
Electrostatic Discharge – Charge Device Model	+/-1k	V
Lead Temperature (soldering, 10 seconds)	260	°C

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- All voltage values are with respect to AGND.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (Note 1)	25.7	°C/W
θ_{JC}	Thermal Resistance Junction to Case (Note 1)	1.84	°C/W
T _{STG}	Storage Temperature Range	-65 to 150	°C
T _{J,MAX}	Maximum Junction Temperature	150	°C
T _J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes 28LD 5x5 QFN mounted on a 4-layers FR4 2S2P JEDEC board as per JESD51-7 with 13.5 inch² of 1 oz Cu and 9 thermal vias connected to PAD.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input Operating Voltage	3.5	5	6	V
VSx	Bridge Supply Voltage	1.0	5	50	V
C _{VCCBYP}	VCC Bypass Capacitor		10		μF
C _{3P3BYP}	Internal 3.0V Bypass Capacitor		4.7		μF
C _{BST}	Bootstrap Capacitor		47		nF
f _{PWL}	Maximum Gate Drive Switching Frequency			300	kHz

Electrical Characteristics

$T^j = 25^\circ\text{C}$ for typical, $T^j = -40^\circ\text{C}$ to 125°C for min and max, $V_{CC} = 5\text{V}$, $V_S = 3.5\text{V} \sim 50\text{V}$ (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC Supply Voltage						
VCC	Input Supply Voltage		3.5	5	6	V
VS	Bridge supply Voltage		3.5	5.0	50	V
Iq_ps	Input Supply current	LDO_EN = Hi; DRV_EN=0V; No load; LDO on, Gate drivers off, demodulator off		0.42	0.75	mA
Iq_ps_drv	Input Supply current, drive mode, LDO_EN=Hi	LDO_EN & DRV_EN = Hi; LDO on, VIN=GAIN=0V, Gate driver Fs = 300KHz (no load), demodulator on		4	5.5	mA
Iq_drv	Input Supply current, drive mode LDO_EN=0	LDO_EN=VIN=GAIN=0V, external 3.0V on VLDO pin; DRV_EN=Hi; No load; Gate drivers on, demodulator on		1.8	3.0	mA
Iqq_sleep	Stand by current	LDO_EN & DRV_EN= 0V; Inputs driven Low		1	10	uA
Ron Characteristics						
Ron (pulldown)	HS,LS pull down device	VCC = 5V		1.8	4	Ω
Ron (pullup)	HS, LS pull up device	VCC = 5V		4.7	8.0	Ω
Under Voltage Lock Out						
UVLO (rise)	UV threshold (VCC)	Rising threshold measurement	3.0	3.10	3.5	V
UVLO (fall)	UV threshold (VCC)	Falling threshold measurement	2.85	2.90	3.4	V
Input Pins VIL, VIH & Pull-down Resistor						
VIH	Digital Input Pins	Gate driver inputs, DRV_EN, SYNC1, SYNC2	0.7*VLDO		VLDO	V
VIL	Digital Input Pins	Gate driver inputs, DRV_EN, SYNC1, SYNC2	0		0.3*VLDO	V
LDOEN_VIH	VIH LDO_EN	Turn on VLDO	1.5		VCC	V
LDOEN_VIL	VIL LDO_EN	Turn off VLDO	0		0.8	V
Rpd	Pull-down resistors	Gate driver inputs, DRV_EN, LDO_EN, SYNC1, SYNC2	24	30	36	k Ω
Gate Driver Power Up & Rise/Fall times						
T _{suDRV_EN}	DRV_EN power up time ¹	DRV_EN=1 to PWM gate driver ready, LDO_EN=0 mode (typical system latency = ~1ms)		20		μs
T _{r_LS}	Rise time (LS)	1nF load; 20 – 80%		12		ns
T _{f_LS}	Fall time (LS)	1nF load; 80 – 20%		12		ns
T _{r_HS}	Rise time (HS)	1nF load wrt VSx; 20 – 80%		45		ns
T _{f_HS}	Fall time (HS)	1nF load wrt VSx; 80 – 20%		10		ns
Propagation Delays, Cross Conduction Protection = ON, HSx/LSx Input Deadtime=0ns						
T _{PLShl}	Prop delay (LS) high to low	LSxON to LOx (1V), 1nF load		50		ns
T _{PLShh}	Prop delay (LS) low to high	LSxON to LOx(1V), 1nF load		100		ns
T _{PHShl}	Prop delay (HS) high to low	HSxON to HOx (HOx – VSx = 1V), 1nF load wrt VSx		60		ns
T _{PHShh}	Prop delay (HS) low to high	HSxON to HOx (HOx – VSx = 1V), 1nF load wrt VSx		120		ns
T _{PMMlshs}	Prop delay mismatch (ls to hs)	LS off to HS on mismatch, 1nF load		15		ns
T _{PMMhsls}	Prop delay mismatch (hs to ls)	HS off to LS on mismatch, 1nF load		40		ns
TPW _{min}	Minimum pulse width response ¹			80		ns
3.0V Regulator						
Vout	Nominal Output voltage		2.70	3.0	3.30	V
Iout	External loading	Output Current capability	40	50		mA
Ilimit	Current Limit ¹	VCC=3.5V, Iout when Vout shifts down10%		90		mA

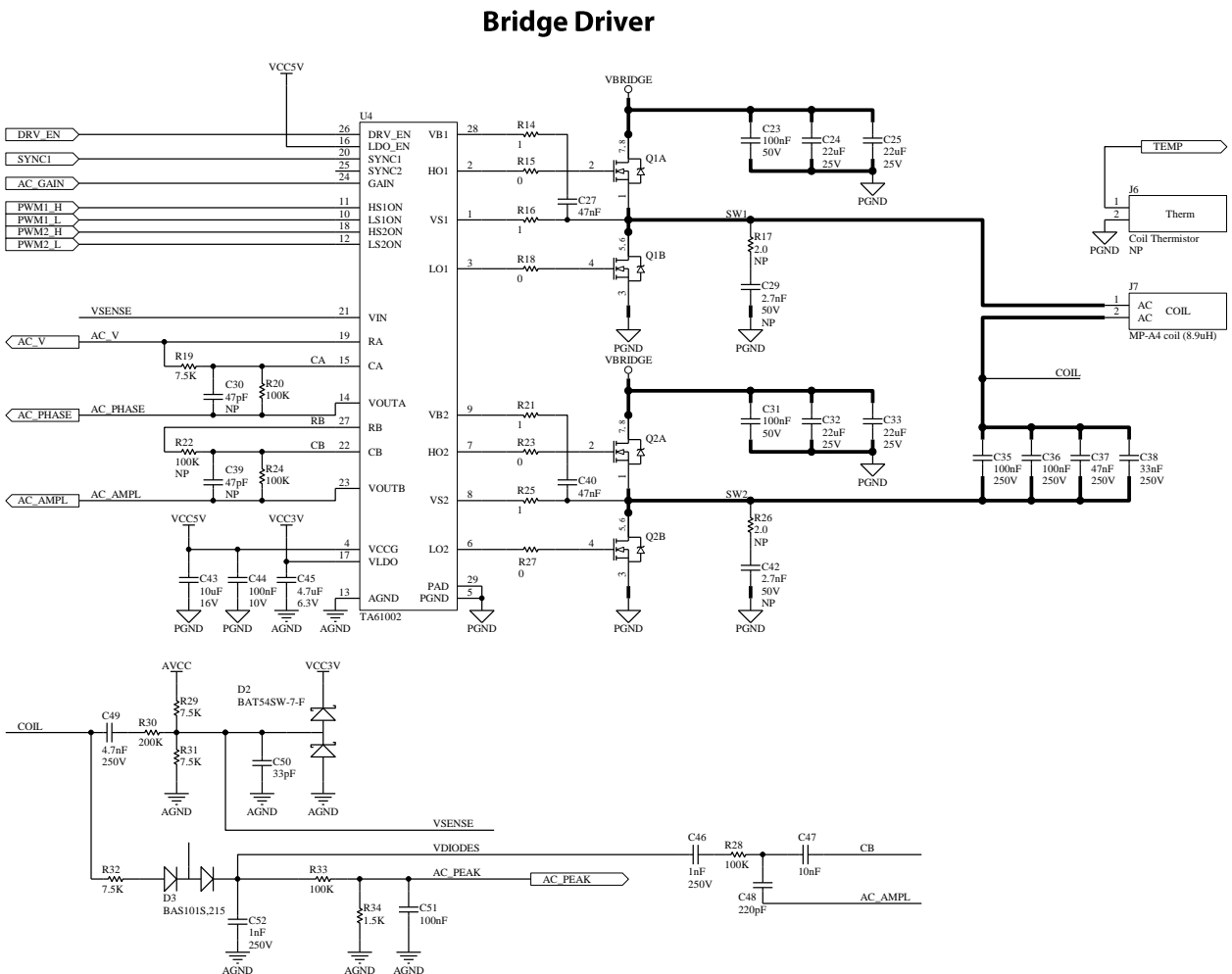
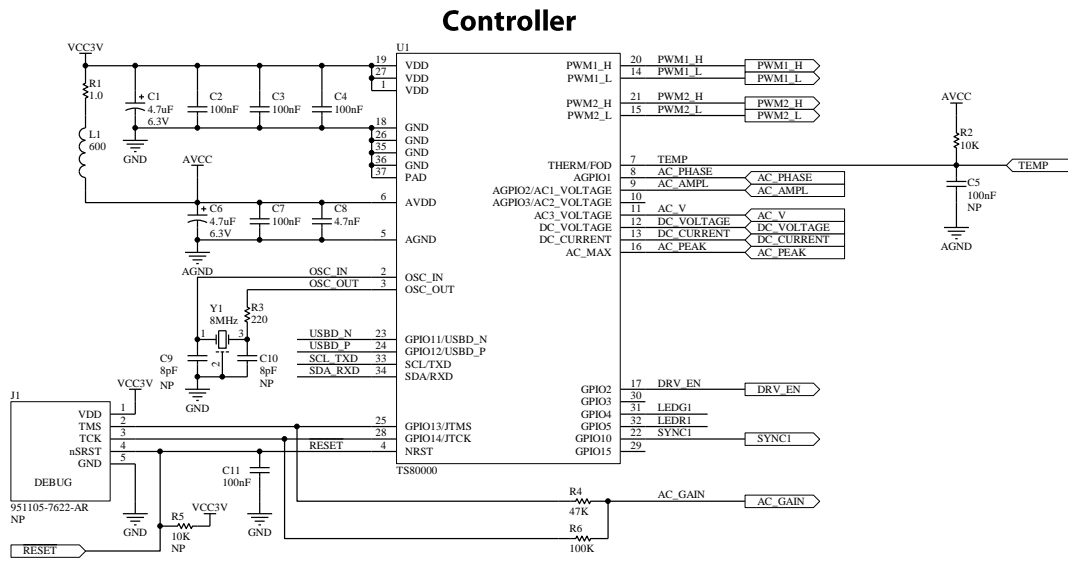
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Demodulator						
Vinput	VIN, CA, CB pin input range		0.65		2.35	V
Av_VIN	VIN Input Gain Setting	0dB		0.5		V
		6dB		1		V
		9.5dB		2		V
		12dB		2.5		V
RA_swing	RA Output Range	100kΩ load to ground, 1Vpp input	0.95	1.0	1.15	Vpp
RB_swing	RB Output Range	100kΩ load to ground, 1Vpp input	0.35	0.42	0.55	Vpp
VREF	Reference Voltage	VLDO=3.0V		1.5		V
VO	VOUTA, VOUTB Output Range		0		3.0	V
Trst	SYNC2 Reset Time ¹	Capacitor between CB and VOUTB = 2.2nF		1.0		μs

Note 1. Not tested in production

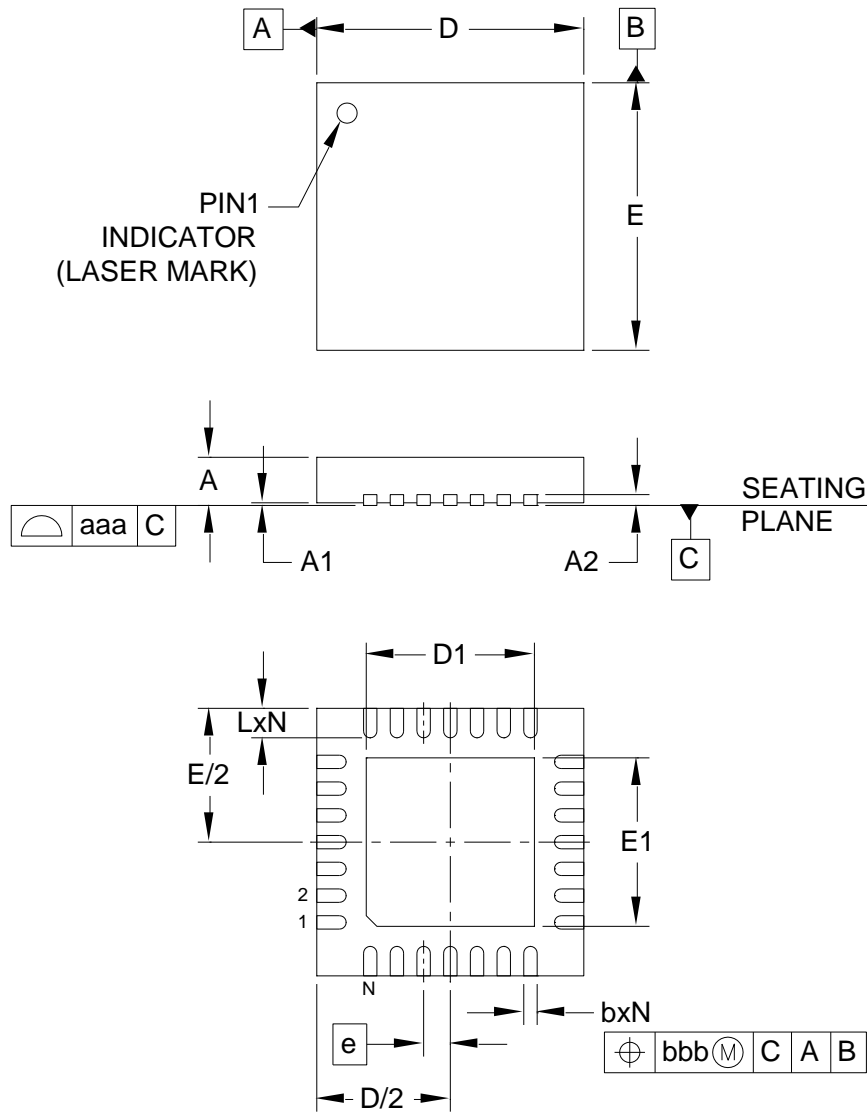
Operational Modes

LDO_EN	DRV_EN	Operational Mode	Gate Drivers	Demodulator	LDO
0	0	LDO=off, Idle	off	off	off
0	1	LDO=off, Drive	on	on	off
1	0	LDO=on, Idle	off	off	on
1	1	LDO=on, Drive	on	on	on

Application Schematic



Package Drawing



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	-	1.00
A1	0.00	-	0.05
A2	(0.20)		
b	0.18	0.25	0.30
D	4.90	5.00	5.10
D1	3.00	3.15	3.25
E	4.90	5.00	5.10
E1	3.00	3.15	3.25
e	0.50 BSC		
L	0.45	0.55	0.65
N	28		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Ordering Information

Device Part Number	Description
TS61002-QFNR	Full-bridge FET Driver



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Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

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