



STB18N65M5, STD18N65M5

N-channel 650 V, 0.198 Ω typ., 15 A MDmesh™ V Power MOSFET in D²PAK and DPAK packages

Datasheet — production data

Features

Order codes	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STB18N65M5	710 V	< 0.22 Ω	15 A
STD18N65M5			

- Worldwide best R_{DS(on)} * area
- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

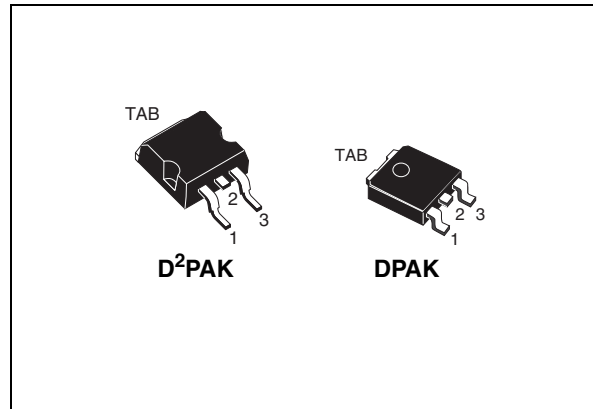


Figure 1. Internal schematic diagram

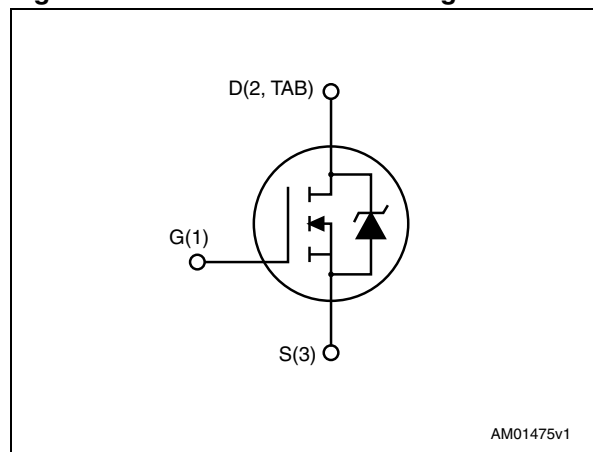


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB18N65M5	18N65M5	D ² PAK	Tape and reel
STD18N65M5		DPAK	

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	9
4	Package mechanical data	10
5	Packaging mechanical data	14
6	Revision history	17



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
V _{GS}	Gate-source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	15		A
I _D	Drain current (continuous) at T _C = 100 °C	9.4		A
I _{DM} ⁽¹⁾	Drain current (pulsed)	60		A
P _{TOT}	Total dissipation at T _C = 25 °C	110		W
dv/dt ⁽¹⁾	Peak diode recovery voltage slope	15		V/ns
T _{stg}	Storage temperature	- 55 to 150		°C
T _j	Max. operating junction temperature	150		°C

1. I_{SD} ≤ 15 A, di/dt ≤ 400 A/μs; V_{DSPeak} < V_{(BR)DSS}, V_{DD} = 400 V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
R _{thj-case}	Thermal resistance junction-case max	1.14		°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	30	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	4	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} ; V _{DD} = 50 V)	210	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$		0.198	0.22	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1240 32 3.2	-	pF pF pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0$	-	99	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	30	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	3	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 520\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 10\text{ V}$ (see Figure 18)	-	31 8 14	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t_d (V)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 9.5$ A,		36		ns
t_r (V)	Voltage rise time	$R_G = 4.7$ Ω , $V_{GS} = 10$ V	-	7	-	ns
$t_{f(i)}$	Current fall time	(see Figure 19 and		9		ns
$t_{c(off)}$	Crossing time	Figure 22)		11		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15$ A, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 15$ A, $di/dt = 100$ A/ μ s	-	290		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100$ V (see Figure 22)	-	3.4		μ C
I_{RRM}	Reverse recovery current			23.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 15$ A, $di/dt = 100$ A/ μ s	-	352		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100$ V, $T_j = 150$ °C	-	4		μ C
I_{RRM}	Reverse recovery current	(see Figure 22)		24		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

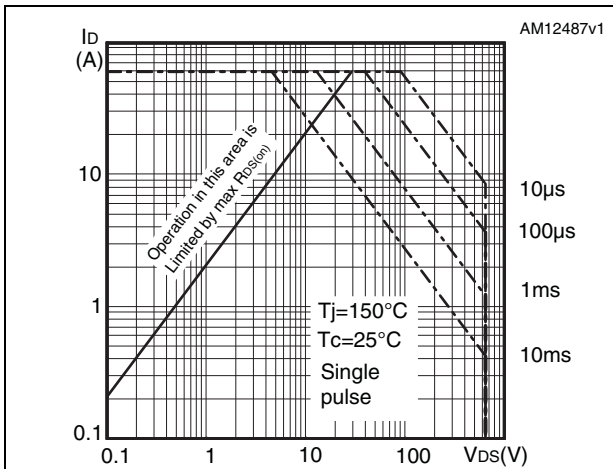


Figure 3. Thermal impedance for D²PAK

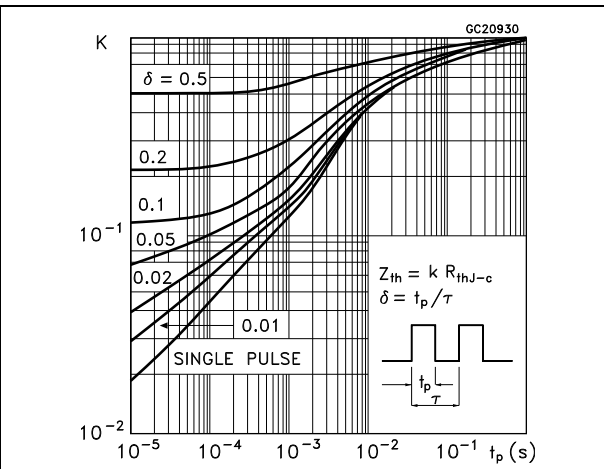


Figure 4. Safe operating area for DPAK

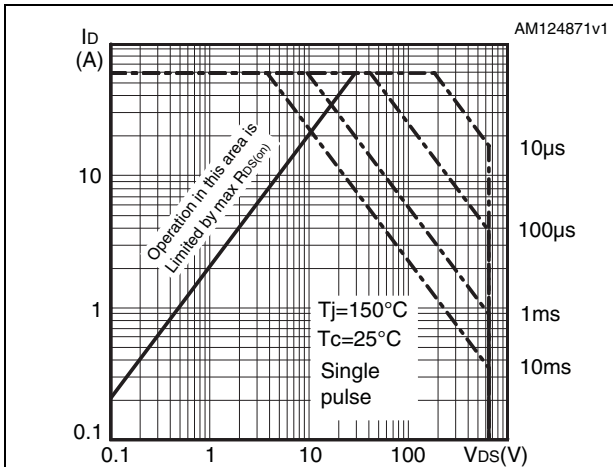


Figure 5. Thermal impedance for DPAK

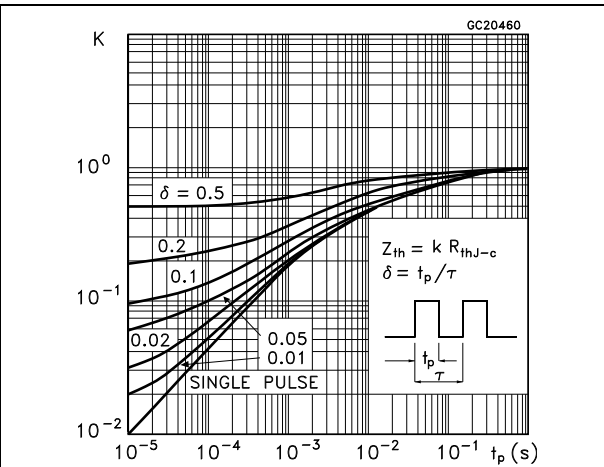


Figure 6. Output characteristics

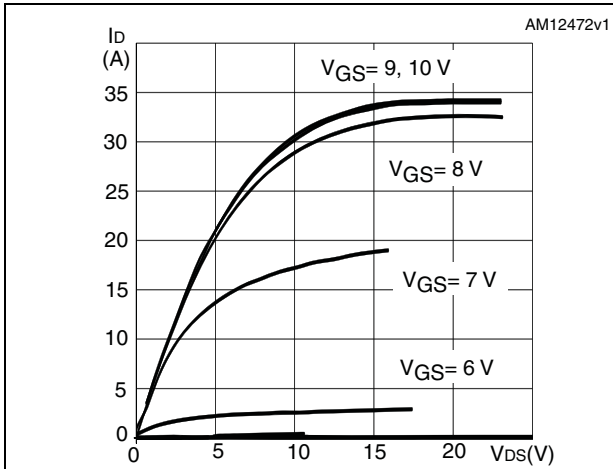


Figure 7. Transfer characteristics

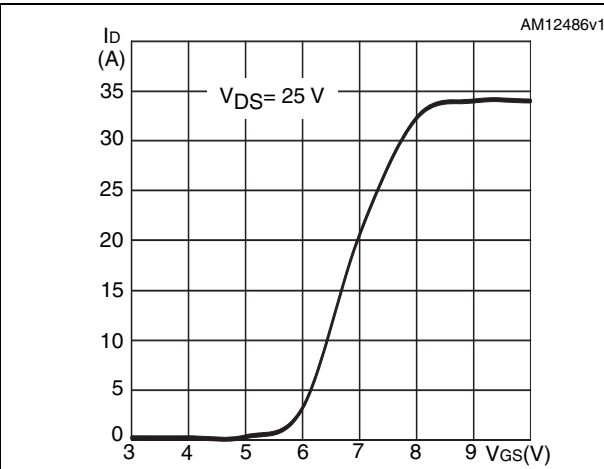


Figure 8. Gate charge vs gate-source voltage Figure 9. Static drain-source on-resistance

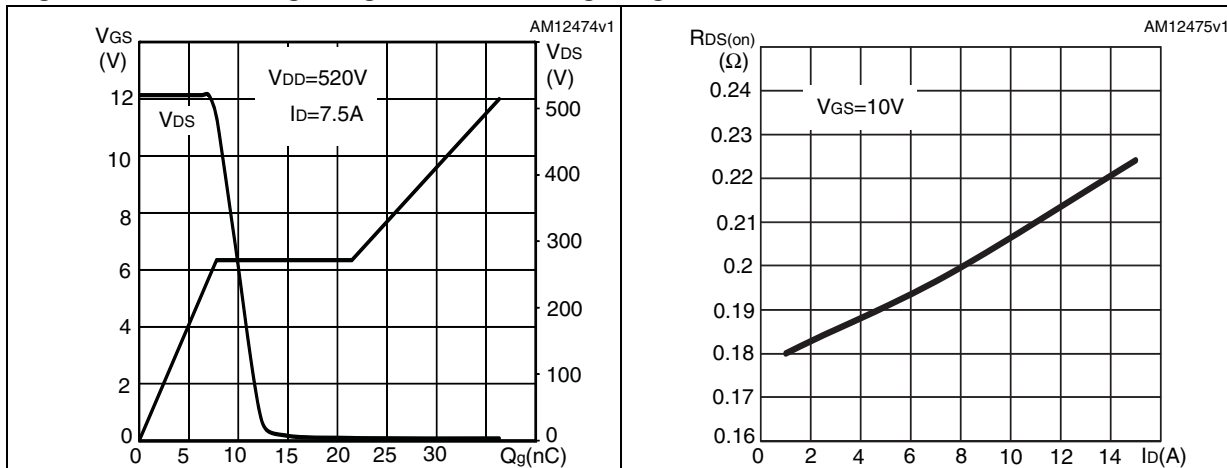


Figure 10. Capacitance variations Figure 11. Output capacitance stored energy

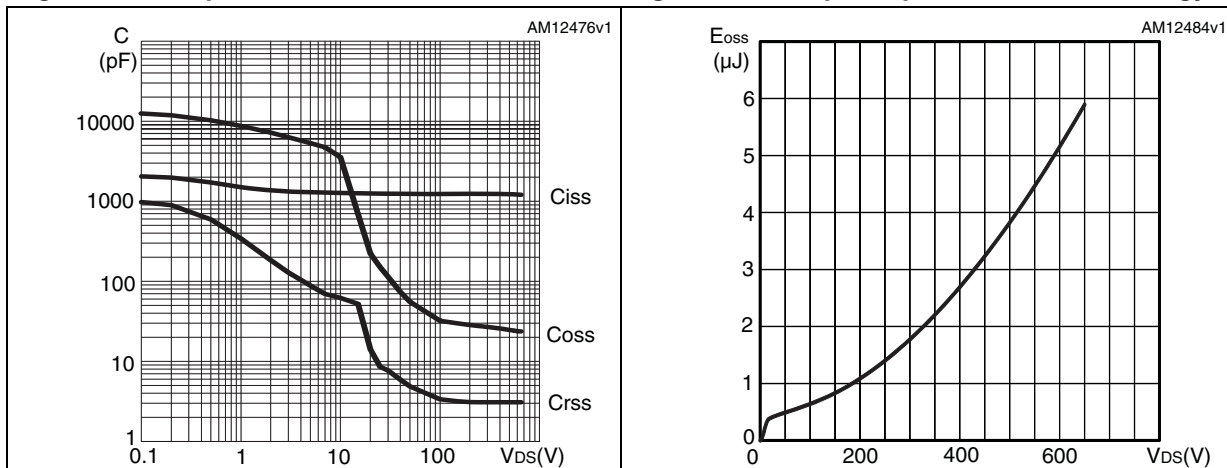


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on-resistance vs temperature

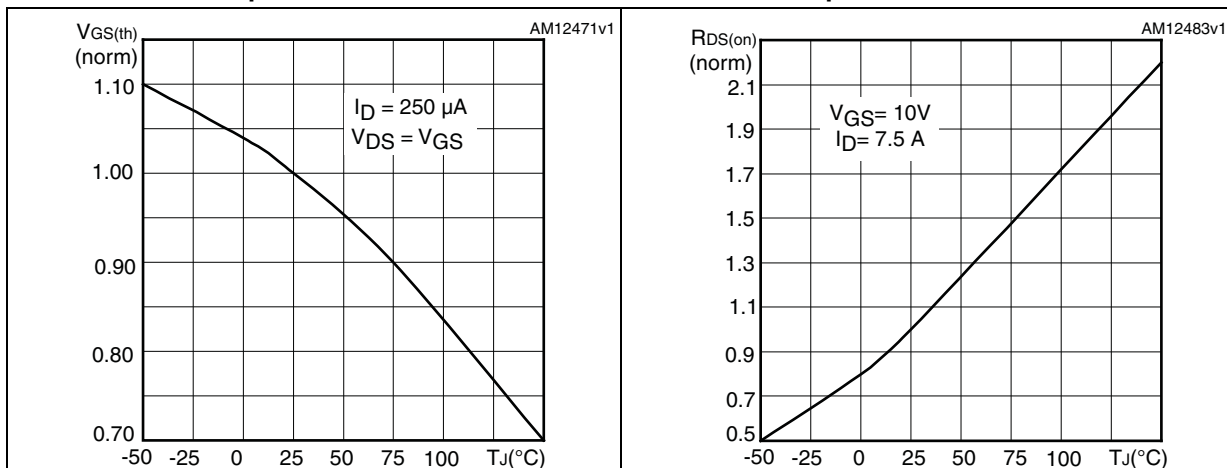


Figure 14. Drain-source diode forward characteristics

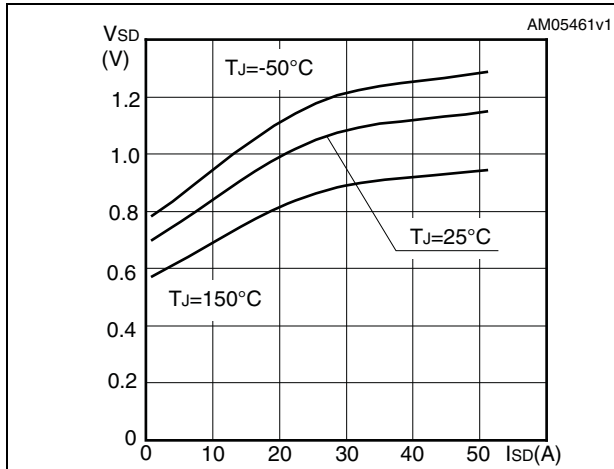


Figure 15. Normalized B_{VDSS} vs temperature

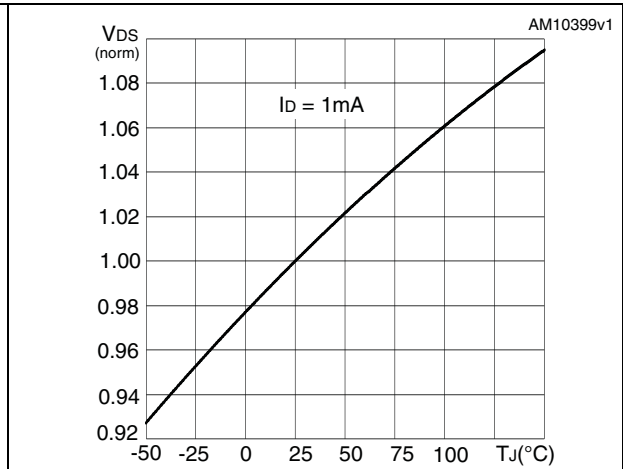
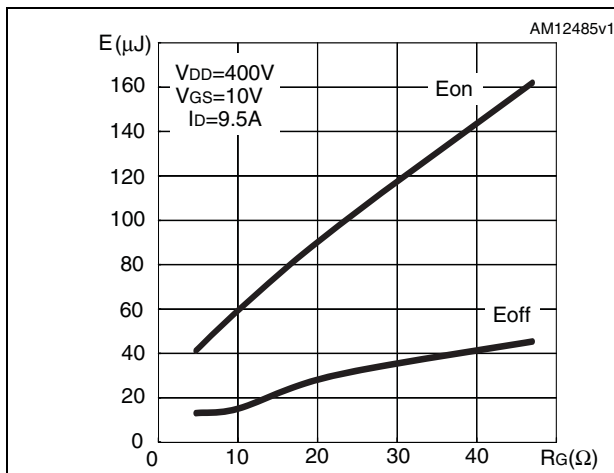


Figure 16. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 17. Switching times test circuit for resistive load

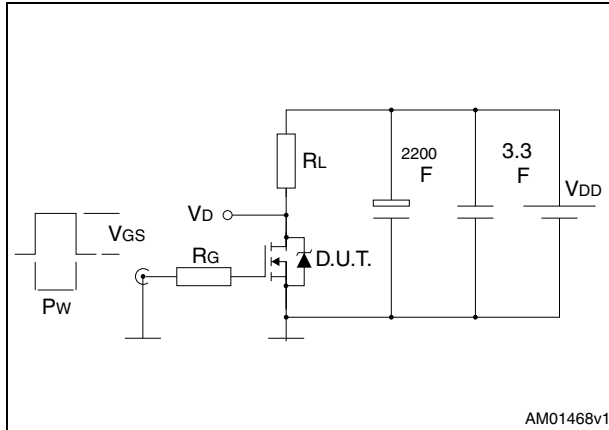


Figure 18. Gate charge test circuit

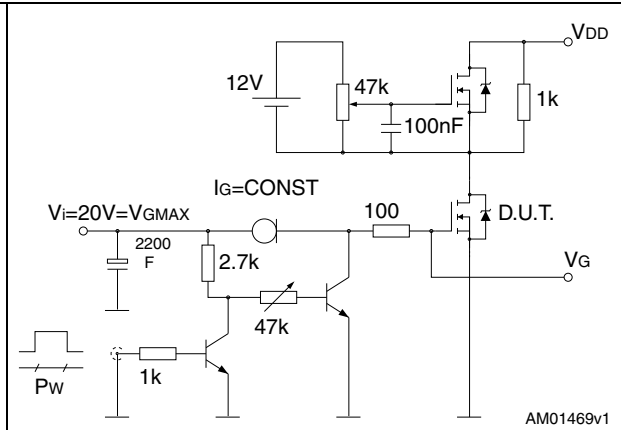


Figure 19. Test circuit for inductive load switching and diode recovery times

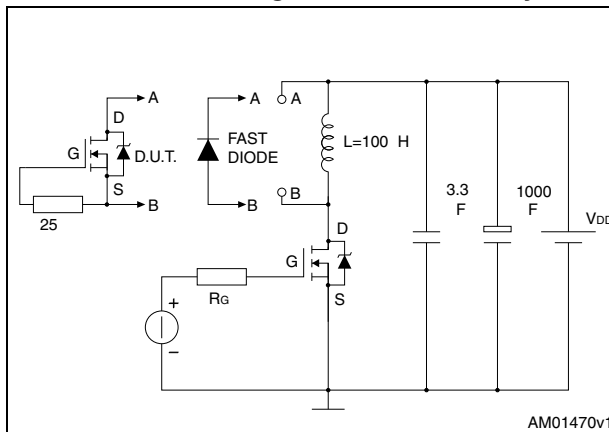


Figure 20. Unclamped inductive load test circuit

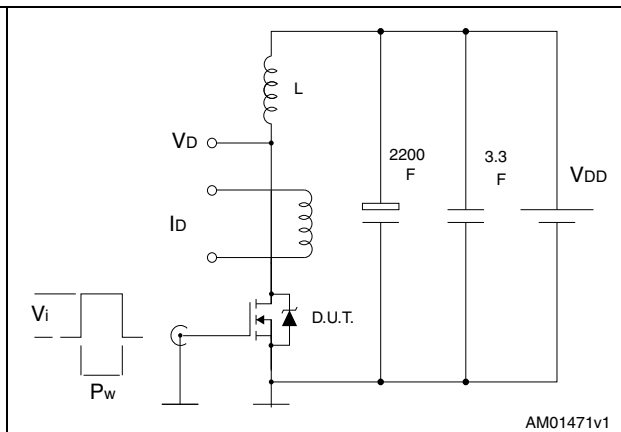


Figure 21. Unclamped inductive waveform

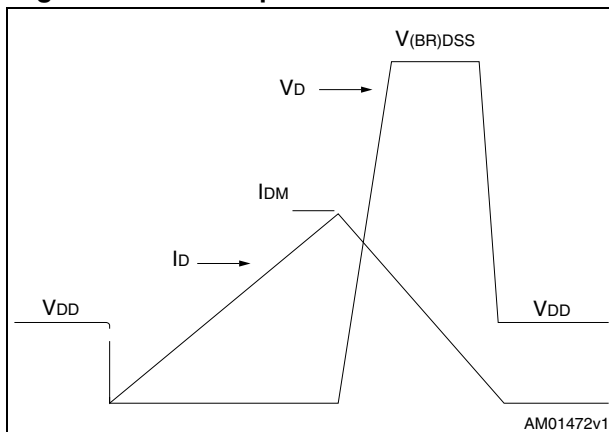
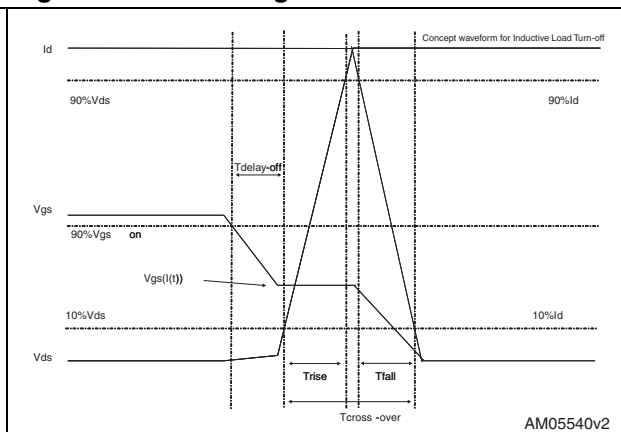


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK (TO-263) drawing



Figure 24. D²PAK footprint^(a)



a. All dimensions are in millimeters

Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

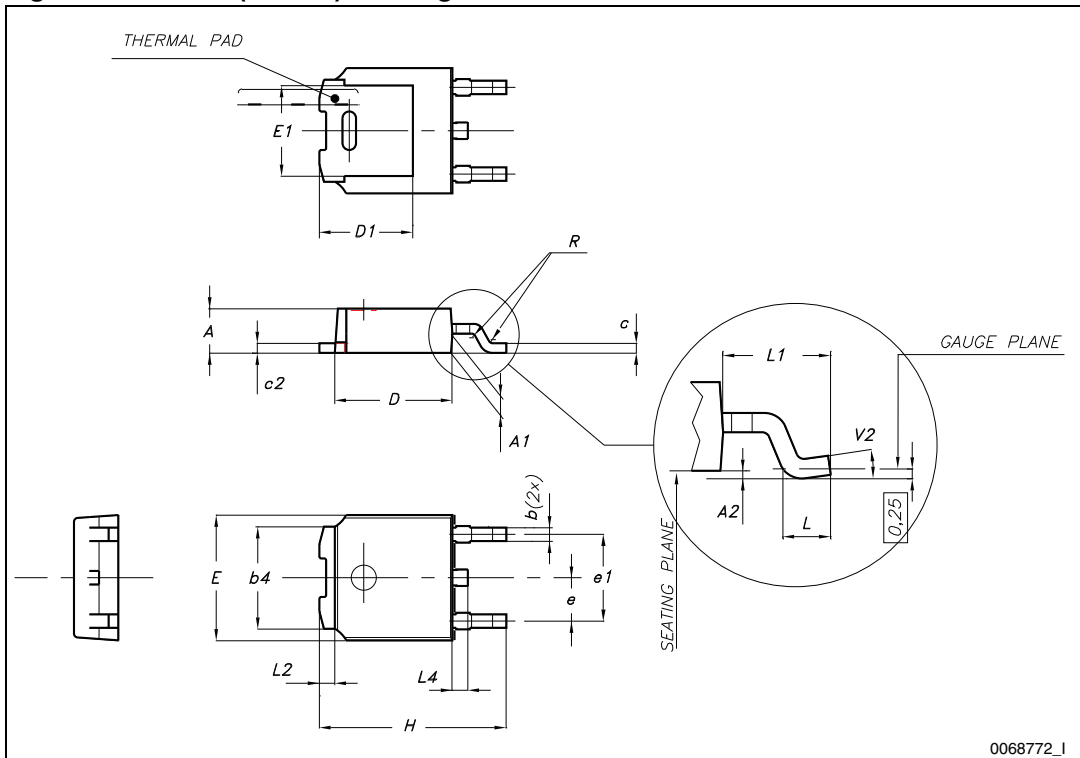
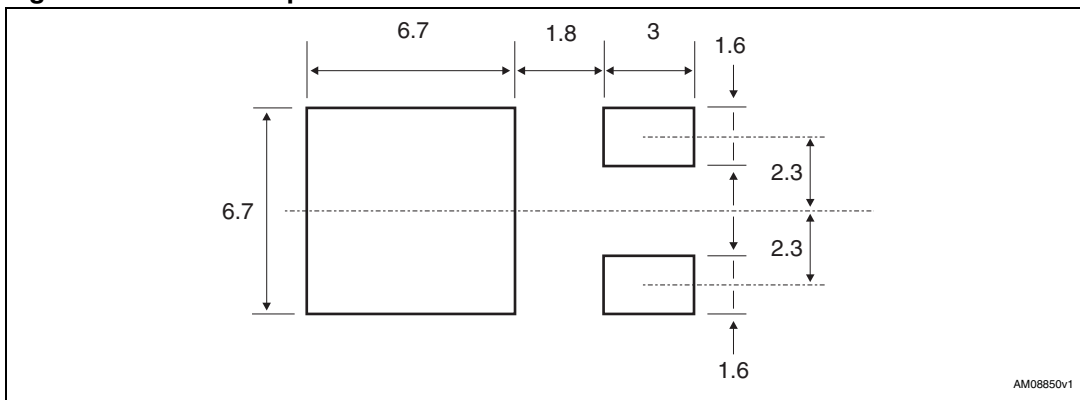


Figure 26. DPAK footprint^(b)



b. All dimensions are in millimeters

5 Packaging mechanical data

Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Table 12. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000

Table 12. D²PAK (TO-263) tape and reel mechanical data (continued)

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 27. Tape for D²PAK (TO-263) and DPAK (TO-252)

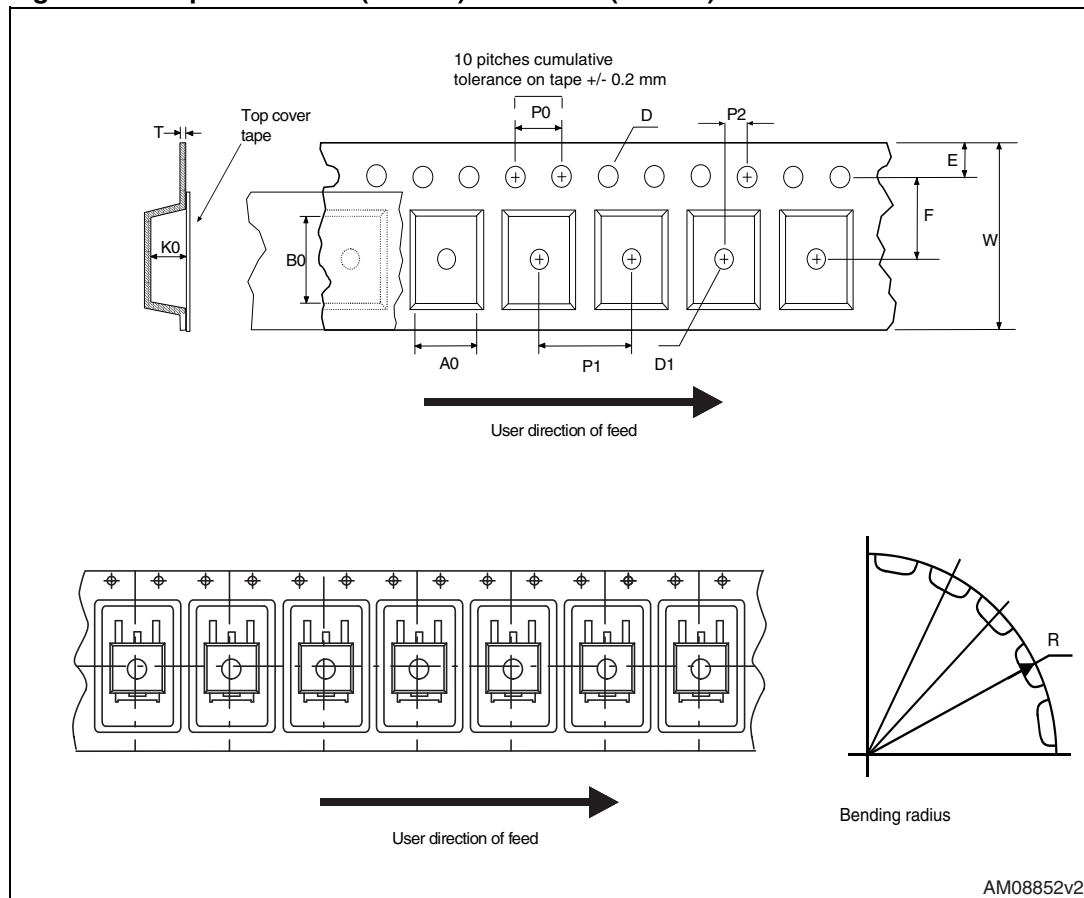
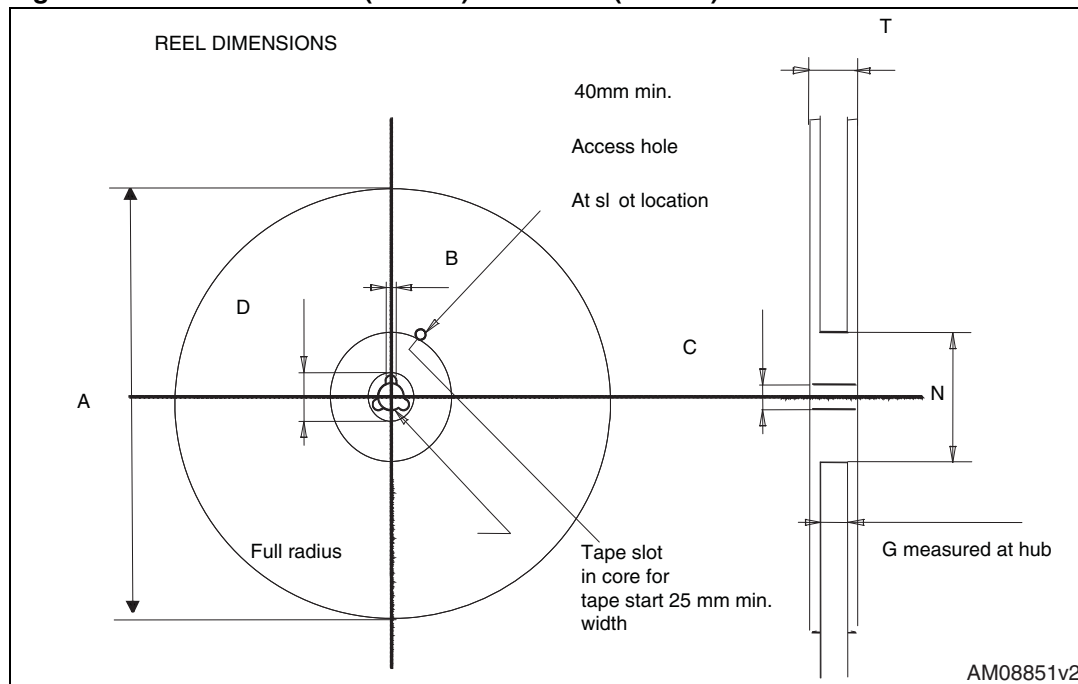


Figure 28. Reel for D²PAK (TO-263) and DPAK (TO-252)



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
18-Jul-2012	1	First release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[STB18N65M5](#) [STD18N65M5](#)